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# HM62A16100I Series

Wide Temperature Range Version  
16 M SRAM (1-Mword × 16-bit)

REJ03C0053-0001Z  
Preliminary  
Rev. 0.01  
Jun.02.2003

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## Description

The Renesas HM62A16100I Series is 16-Mbit static RAM organized 1-Mword × 16-bit. HM62A16100I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has the package variations of 48-bump chip size package with 0.75 mm bump pitch for high density surface mounting.

## Features

- Single 1.8 V supply: 1.65 V to 2.2 V
- Fast access time: 70 ns (max)
- Power dissipation:
  - Active: 3.6 mW/MHz (typ)
  - Standby: 0.9 μW (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
  - 2 chip selection for battery backup
- Temperature range: -40 to +85°C

Preliminary: The specification of this device are subject to change without notice. Please contact your nearest Renesas Technology's Sales Dept. regarding specification.

## HM62A16100I Series

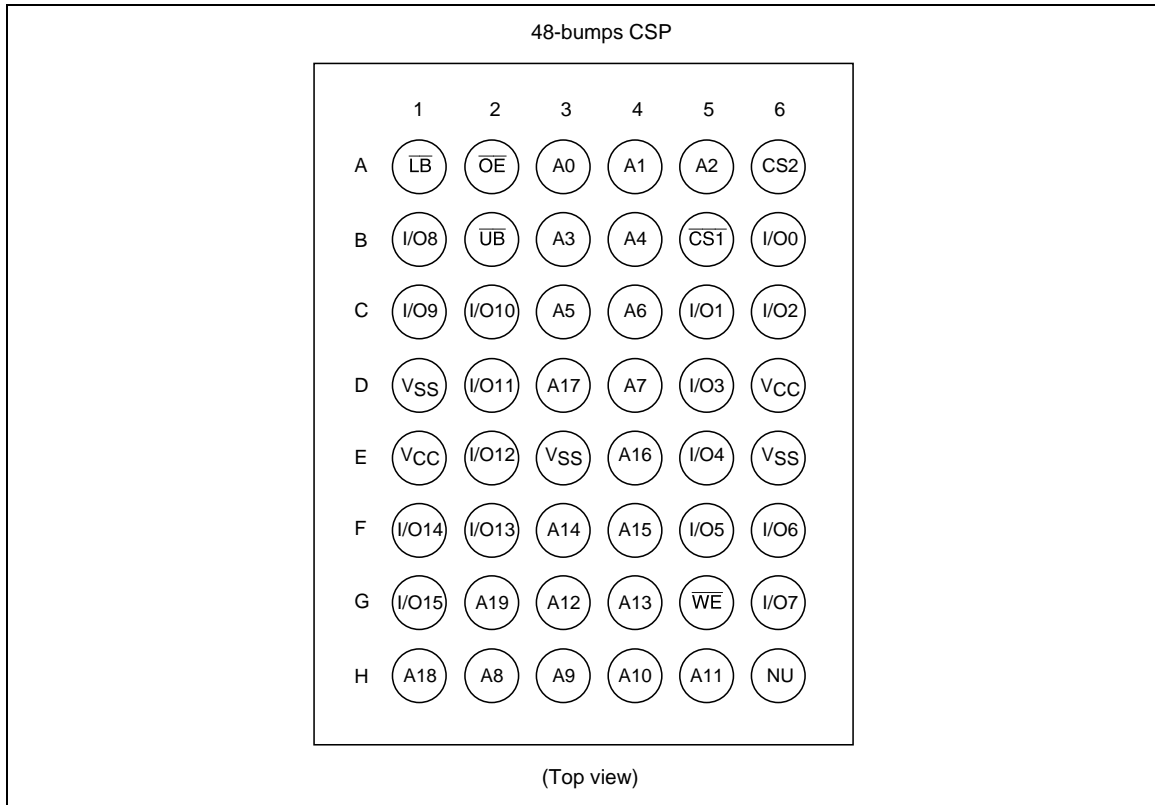
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### Ordering Information

| Type No.           | Access time | Package                                       |
|--------------------|-------------|---|
| HM62A16100LBPI-7   | 70 ns       | 48-bump CSP with 0.75 mm bump pitch (TBP-48F) |
| HM62A16100LBPI-7SL | 70 ns       |   |

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**Pin Arrangement**

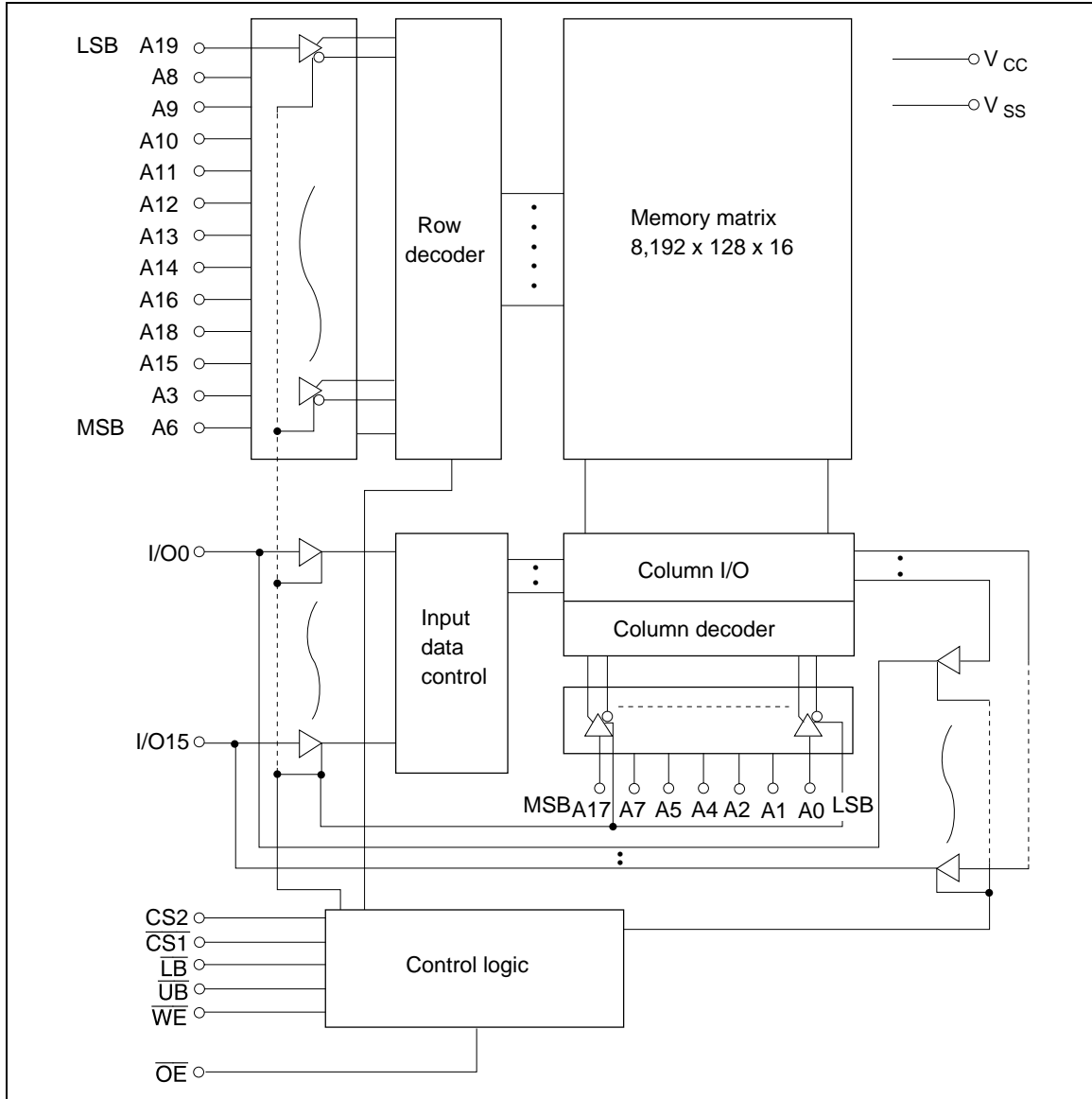


**Pin Description**

| Pin name         | Function                 |
|------------------|--------------------------|
| A0 to A19        | Address input            |
| I/O0 to I/O15    | Data input/output        |
| CS1              | Chip select 1            |
| CS2              | Chip select 2            |
| WE               | Write enable             |
| OE               | Output enable            |
| LB               | Lower byte select        |
| UB               | Upper byte select        |
| V <sub>cc</sub>  | Power supply             |
| V <sub>ss</sub>  | Ground                   |
| NU* <sup>1</sup> | Not used (test mode pin) |

Note: 1. This pin should be connected to a ground (V<sub>ss</sub>), or not be connected (open).

Block Diagram



## HM62A16100I Series

### Operation Table

| CS1 | CS2 | WE | OE | UB | LB | I/O0 to I/O7 | I/O8 to I/O15 | Operation        |
|-----|-----|----|----|----|----|--------------|---------------|------------------|
| H   | ×   | ×  | ×  | ×  | ×  | High-Z       | High-Z        | Standby          |
| ×   | L   | ×  | ×  | ×  | ×  | High-Z       | High-Z        | Standby          |
| ×   | ×   | ×  | ×  | H  | H  | High-Z       | High-Z        | Standby          |
| L   | H   | H  | L  | L  | L  | Dout         | Dout          | Read             |
| L   | H   | H  | L  | H  | L  | Dout         | High-Z        | Lower byte read  |
| L   | H   | H  | L  | L  | H  | High-Z       | Dout          | Upper byte read  |
| L   | H   | L  | ×  | L  | L  | Din          | Din           | Write            |
| L   | H   | L  | ×  | H  | L  | Din          | High-Z        | Lower byte write |
| L   | H   | L  | ×  | L  | H  | High-Z       | Din           | Upper byte write |
| L   | H   | H  | H  | ×  | ×  | High-Z       | High-Z        | Output disable   |

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , ×:  $V_{IH}$  or  $V_{IL}$

### Absolute Maximum Ratings

| Parameter  | Symbol   | Value   | Unit |
|--|----------|---|------|
| Power supply voltage relative to $V_{SS}$        | $V_{CC}$ | -0.3 to +2.6  | V    |
| Terminal voltage on any pin relative to $V_{SS}$ | $V_T$    | -0.3* <sup>1</sup> to $V_{CC} + 0.3$ * <sup>2</sup> | V    |
| Power dissipation                                | $P_T$    | 1.0   | W    |
| Storage temperature range                        | Tstg     | -55 to +125   | °C   |
| Storage temperature range under bias             | Tbias    | -40 to +85  | °C   |

Notes: 1.  $V_T$  min: -2.0 V for pulse half-width ≤ 10 ns.

2. Maximum voltage is +2.6 V.

### DC Operating Conditions

| Parameter                 | Symbol   | Min                  | Typ | Max                  | Unit | Note |
|---------------------------|----------|----------------------|-----|----------------------|------|------|
| Supply voltage            | $V_{CC}$ | 1.65                 | 1.8 | 2.2                  | V    |      |
|                           | $V_{SS}$ | 0                    | 0   | 0                    | V    |      |
| Input high voltage        | $V_{IH}$ | $0.75 \times V_{CC}$ | —   | $V_{CC} + 0.3$       | V    |      |
| Input low voltage         | $V_{IL}$ | -0.3                 | —   | $0.25 \times V_{CC}$ | V    | 1    |
| Ambient temperature range | Ta       | -40                  | —   | 85                   | °C   |      |

Note: 1.  $V_{IL}$  min: -2.0 V for pulse half-width ≤ 10 ns.

## HM62A16100I Series

### DC Characteristics

| Parameter                 | Symbol                  | Min            | Typ* <sup>1</sup> | Max | Unit          | Test conditions  |
|---------------------------|-------------------------|----------------|-------------------|-----|---------------|--|
| Input leakage current     | $ I_{LI} $              | —              | —                 | 1   | $\mu\text{A}$ | $V_{in} = V_{SS}$ to $V_{CC}$  |
| Output leakage current    | $ I_{LO} $              | —              | —                 | 1   | $\mu\text{A}$ | CS1 = $V_{IH}$ or CS2 = $V_{IL}$ or<br>OE = $V_{IH}$ or WE = $V_{IL}$ or<br>LB = UB = $V_{IH}$ , $V_{IO} = V_{SS}$ to $V_{CC}$   |
| Operating current         | $I_{CC}$                | —              | —                 | 8   | mA            | CS1 = $V_{IL}$ , CS2 = $V_{IH}$ ,<br>Others = $V_{IH}/V_{IL}$ , $I_{IO} = 0$ mA  |
| Average operating current | $I_{CC1}$               | —              | 20                | 30  | mA            | Min. cycle, duty = 100%,<br>$I_{IO} = 0$ mA, CS1 = $V_{IL}$ , CS2 = $V_{IH}$ ,<br>Others = $V_{IH}/V_{IL}$   |
|                           | $I_{CC2}$               | —              | 2                 | 5   | mA            | Cycle time = 1 $\mu\text{s}$ , duty = 100%,<br>$I_{IO} = 0$ mA, CS1 $\leq 0.2$ V,<br>CS2 $\geq V_{CC} - 0.2$ V<br>$V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V  |
| Standby current           | $I_{SB}$                | —              | 0.1               | 0.5 | mA            | CS2 = $V_{IL}$   |
| Standby current           | $I_{SB1}$ <sup>*2</sup> | —              | 0.5               | 25  | $\mu\text{A}$ | 0 V $\leq V_{in}$<br>(1) 0 V $\leq$ CS2 $\leq 0.2$ V or<br>(2) CS1 $\geq V_{CC} - 0.2$ V,<br>CS2 $\geq V_{CC} - 0.2$ V or<br>(3) LB = UB $\geq V_{CC} - 0.2$ V,<br>CS2 $\geq V_{CC} - 0.2$ V,<br>CS1 $\leq 0.2$ V<br>Average value |
|                           | $I_{SB1}$ <sup>*3</sup> | —              | 0.5               | 8   | $\mu\text{A}$ |  |
| Output high voltage       | $V_{OH}$                | $V_{CC} - 0.2$ | —                 | —   | V             | $I_{OH} = -100$ $\mu\text{A}$  |
| Output low voltage        | $V_{OL}$                | —              | —                 | 0.2 | V             | $I_{OL} = 100$ $\mu\text{A}$   |

Notes: 1. Typical values are at  $V_{CC} = 1.8$  V,  $T_a = +25^\circ\text{C}$  and not guaranteed.

2. This characteristic is guaranteed only for L-version.

3. This characteristic is guaranteed only for L-SL version.

### Capacitance

( $T_a = +25^\circ\text{C}$ ,  $f = 1.0$  MHz)

| Parameter                | Symbol   | Min | Typ | Max | Unit | Test conditions | Note |
|--------------------------|----------|-----|-----|-----|------|-----------------|------|
| Input capacitance        | $C_{in}$ | —   | —   | 8   | pF   | $V_{in} = 0$ V  | 1    |
| Input/output capacitance | $C_{IO}$ | —   | —   | 10  | pF   | $V_{IO} = 0$ V  | 1    |

Note: 1. This parameter is sampled and not 100% tested.

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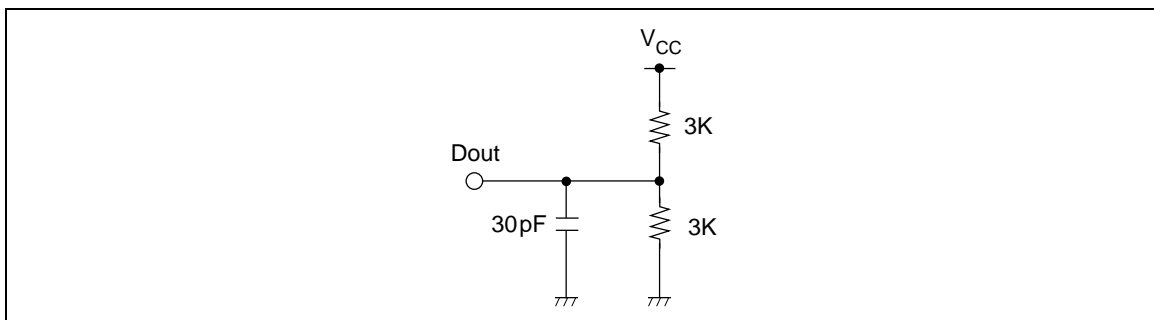
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### AC Characteristics

( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 1.65$  V to  $2.2$  V, unless otherwise noted.)

#### Test Conditions

- Input pulse levels:  $V_{IL} = 0.2$  V,  $V_{IH} = V_{CC} - 0.2$  V
- Input rise and fall time: 3 ns
- Input and output timing reference levels:  $0.5 \times V_{CC}$
- Output load: See figures (Including scope and jig)



## HM62A16100I Series

### Read Cycle

| Parameter                          | Symbol     | HM62A16100I |     | Unit | Notes   |
|------------------------------------|------------|-------------|-----|------|---------|
|                                    |            | -7          |     |      |         |
|                                    |            | Min         | Max |      |         |
| Read cycle time                    | $t_{RC}$   | 70          | —   | ns   |         |
| Address access time                | $t_{AA}$   | —           | 70  | ns   |         |
| Chip select access time            | $t_{ACS1}$ | —           | 70  | ns   |         |
|                                    | $t_{ACS2}$ | —           | 70  | ns   |         |
| Output enable to output valid      | $t_{OE}$   | —           | 35  | ns   |         |
| Output hold from address change    | $t_{OH}$   | 10          | —   | ns   |         |
| LB, UB access time                 | $t_{BA}$   | —           | 70  | ns   |         |
| Chip select to output in low-Z     | $t_{CLZ1}$ | 10          | —   | ns   | 2, 3    |
|                                    | $t_{CLZ2}$ | 10          | —   | ns   | 2, 3    |
| LB, UB enable to low-Z             | $t_{BLZ}$  | 5           | —   | ns   | 2, 3    |
| Output enable to output in low-Z   | $t_{OLZ}$  | 5           | —   | ns   | 2, 3    |
| Chip deselect to output in high-Z  | $t_{CHZ1}$ | 0           | 25  | ns   | 1, 2, 3 |
|                                    | $t_{CHZ2}$ | 0           | 25  | ns   | 1, 2, 3 |
| LB, UB disable to high-Z           | $t_{BHZ}$  | 0           | 25  | ns   | 1, 2, 3 |
| Output disable to output in high-Z | $t_{OHZ}$  | 0           | 25  | ns   | 1, 2, 3 |

### Write Cycle

| Parameter                          | Symbol    | HM62A16100I |     | Unit | Notes |
|------------------------------------|-----------|-------------|-----|------|-------|
|                                    |           | -7          |     |      |       |
|                                    |           | Min         | Max |      |       |
| Write cycle time                   | $t_{WC}$  | 70          | —   | ns   |       |
| Address valid to end of write      | $t_{AW}$  | 60          | —   | ns   |       |
| Chip selection to end of write     | $t_{CW}$  | 60          | —   | ns   | 5     |
| Write pulse width                  | $t_{WIP}$ | 50          | —   | ns   | 4     |
| LB, UB valid to end of write       | $t_{BW}$  | 60          | —   | ns   |       |
| Address setup time                 | $t_{AS}$  | 0           | —   | ns   | 6     |
| Write recovery time                | $t_{WR}$  | 0           | —   | ns   | 7     |
| Data to write time overlap         | $t_{DW}$  | 30          | —   | ns   |       |
| Data hold from write time          | $t_{DH}$  | 0           | —   | ns   |       |
| Output active from end of write    | $t_{OW}$  | 5           | —   | ns   | 2     |
| Output disable to output in high-Z | $t_{OHZ}$ | 0           | 25  | ns   | 1, 2  |
| Write to output in high-Z          | $t_{WHZ}$ | 0           | 25  | ns   | 1, 2  |



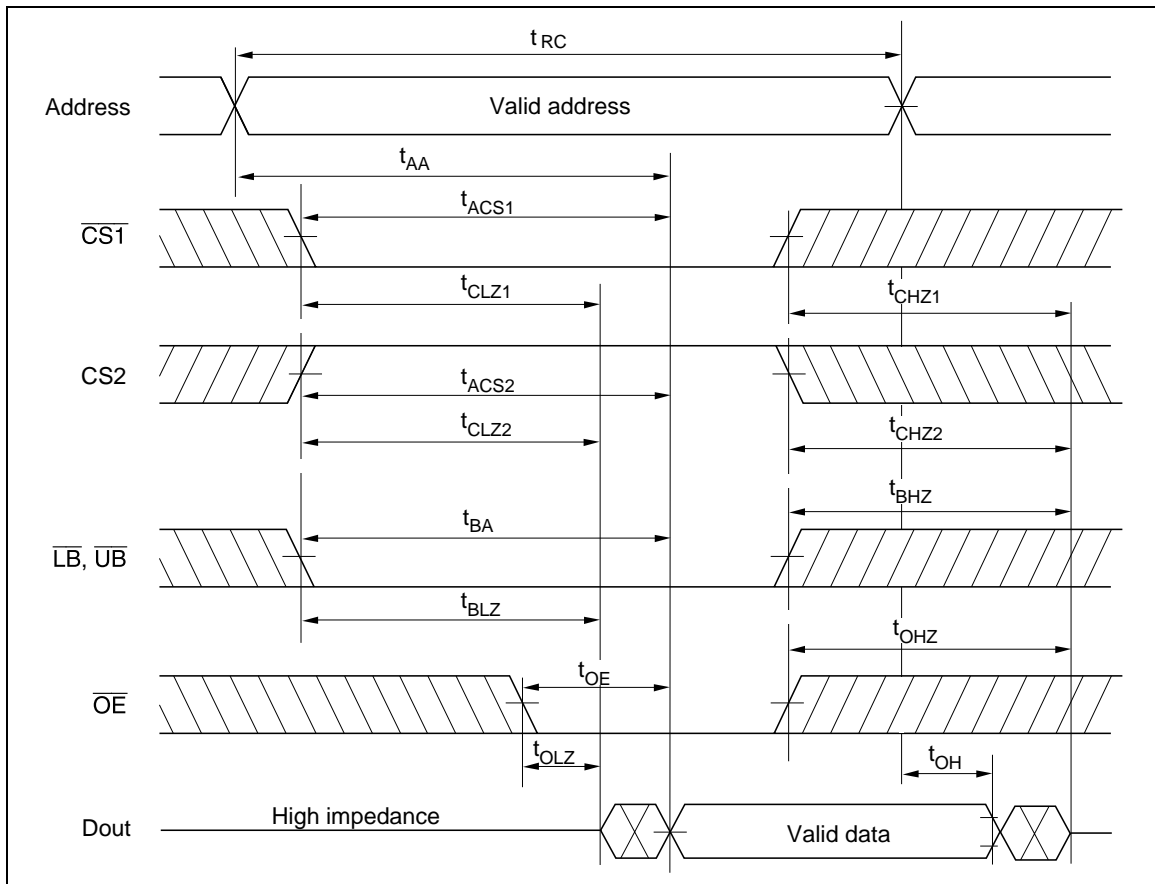
## HM62A16100I Series

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- Notes:
1.  $t_{\text{CHZ}}$ ,  $t_{\text{OHZ}}$ ,  $t_{\text{WHZ}}$  and  $t_{\text{BHZ}}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  2. This parameter is sampled and not 100% tested.
  3. At any given temperature and voltage condition,  $t_{\text{HZ}}$  max is less than  $t_{\text{LZ}}$  min both for a given device and from device to device.
  4. A write occurs during the overlap of a low CS1, a high CS2, a low WE and a low LB or a low UB. A write begins at the latest transition among CS1 going low, CS2 going high, WE going low and LB going low or UB going low. A write ends at the earliest transition among CS1 going high, CS2 going low, WE going high and LB going high or UB going high.  $t_{\text{WP}}$  is measured from the beginning of write to the end of write.
  5.  $t_{\text{CW}}$  is measured from the later of CS1 going low or CS2 going high to the end of write.
  6.  $t_{\text{AS}}$  is measured from the address valid to the beginning of write.
  7.  $t_{\text{WR}}$  is measured from the earliest of CS1 or WE going high or CS2 going low to the end of write cycle.

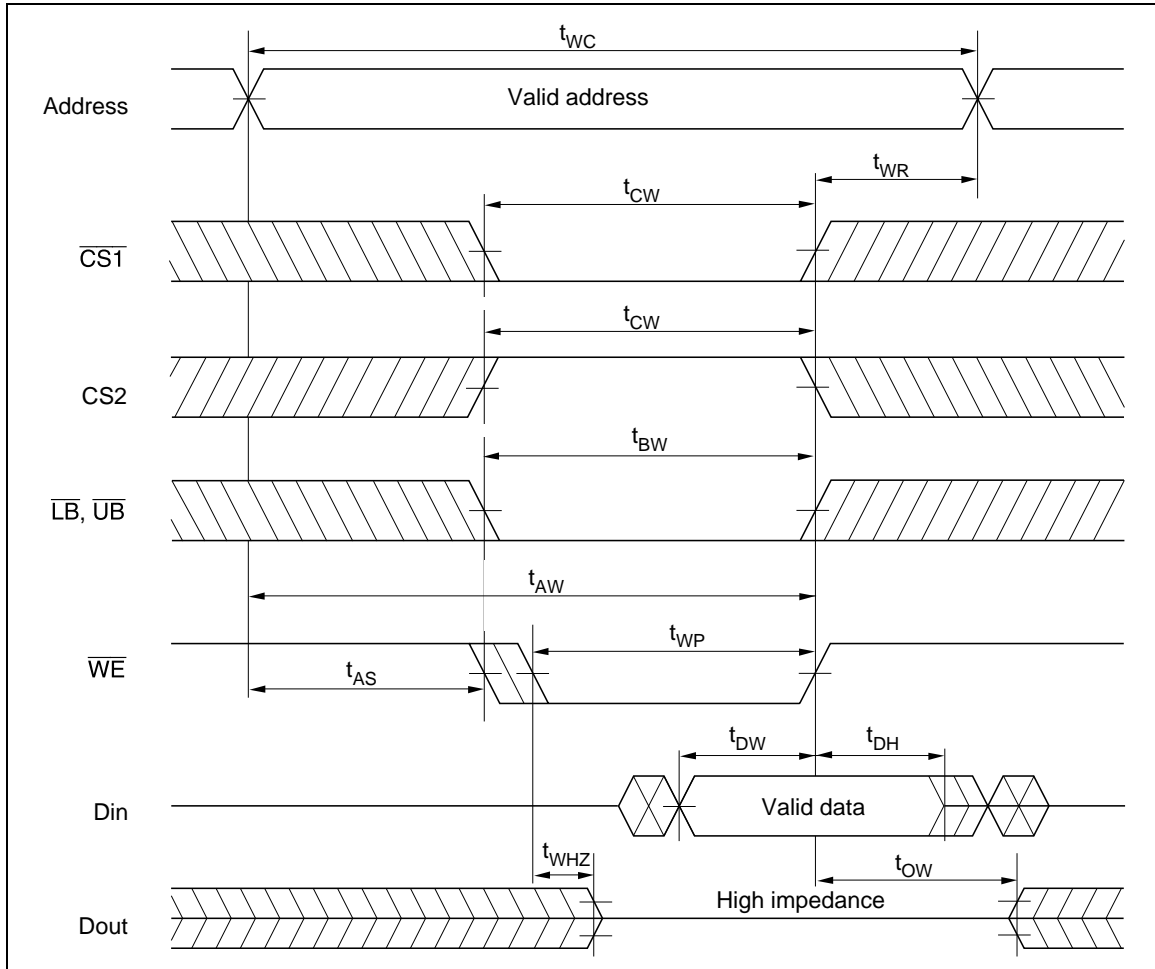
Timing Waveform

Read Cycle



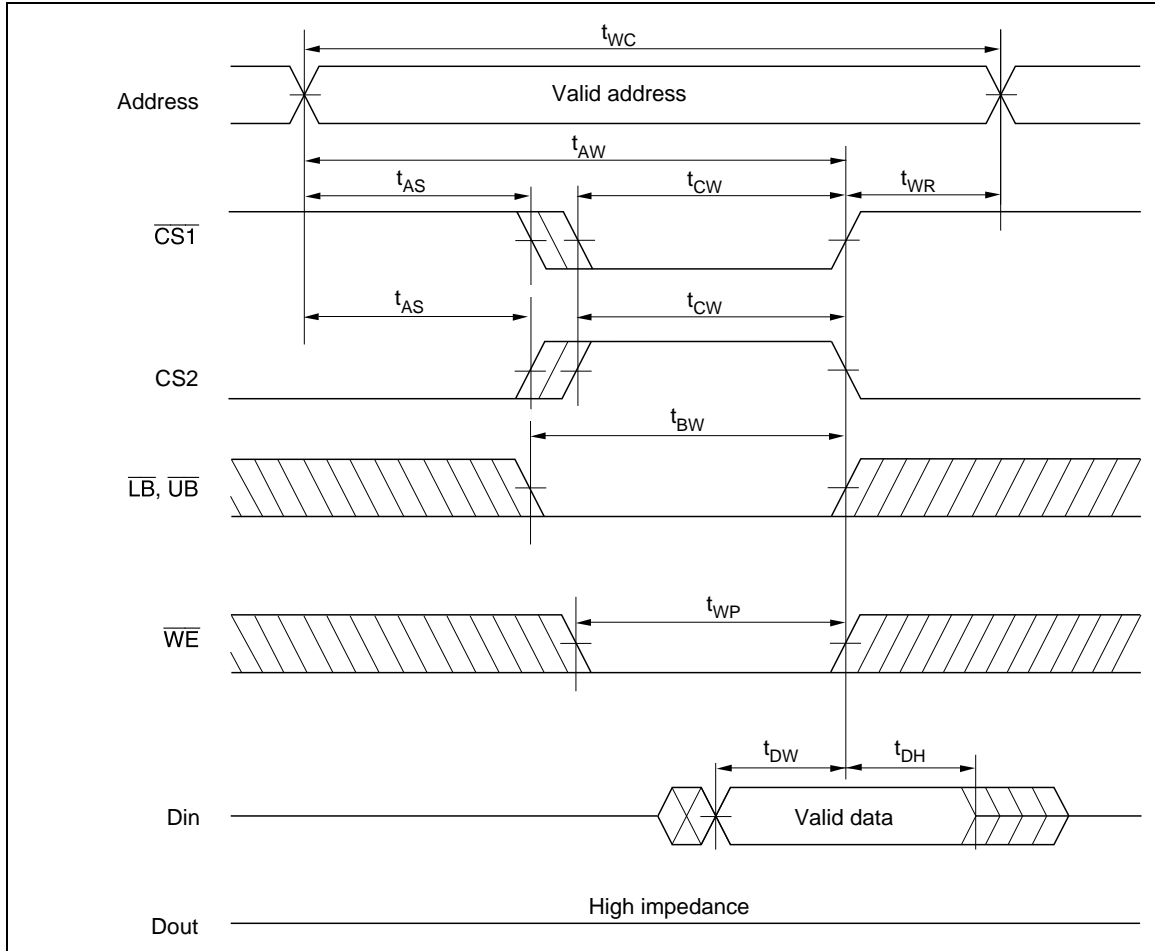
**HM62A16100I Series**

**Write Cycle (1) (WE Clock)**



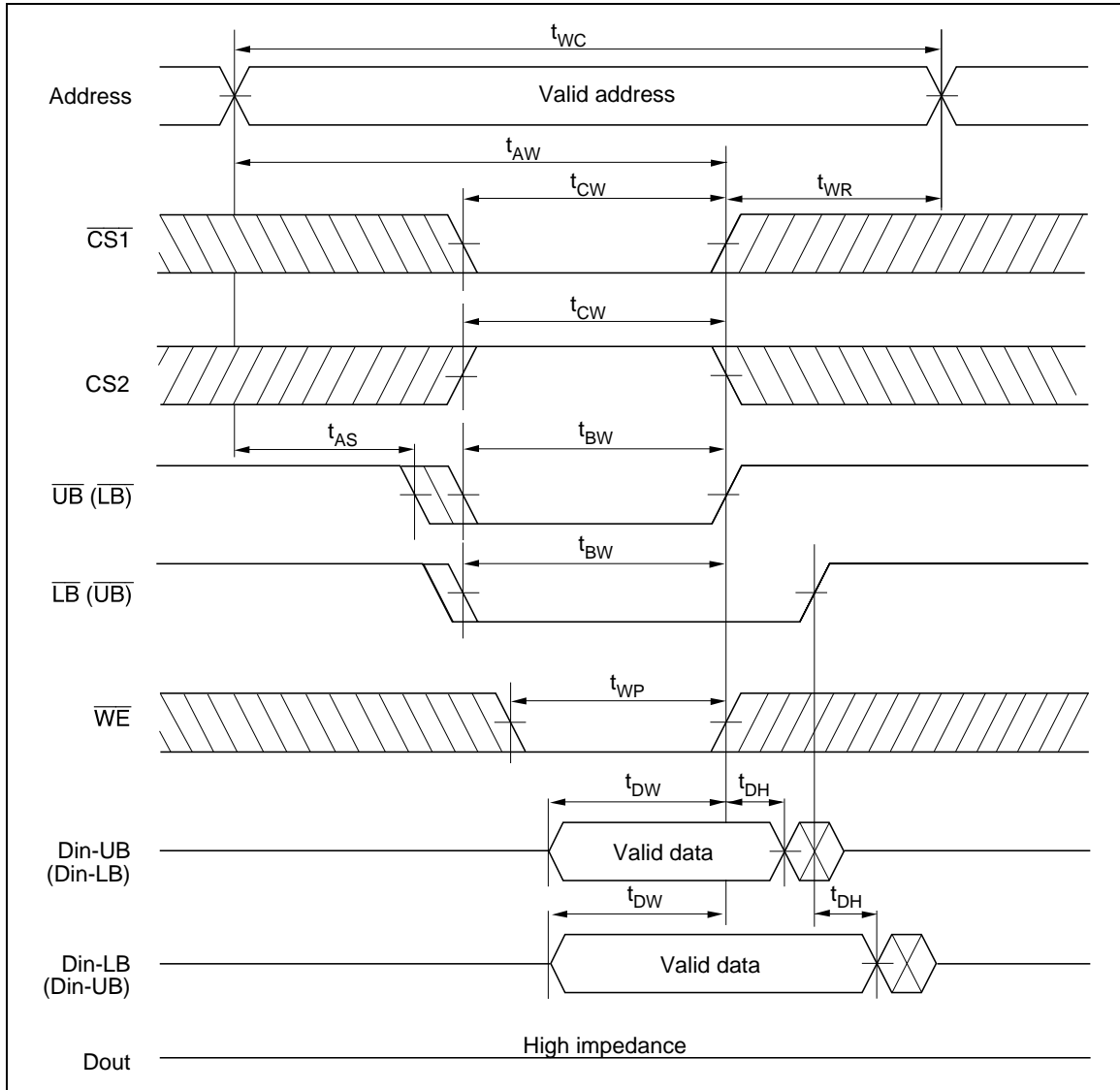
**HM62A16100I Series**

**Write Cycle (2) (CS1, CS2 Clock, OE = V<sub>IH</sub>)**



**HM62A16100I Series**

**Write Cycle (3) (LB, UB Clock, OE = V<sub>IH</sub>)**



## HM62A16100I Series

### Low $V_{CC}$ Data Retention Characteristics

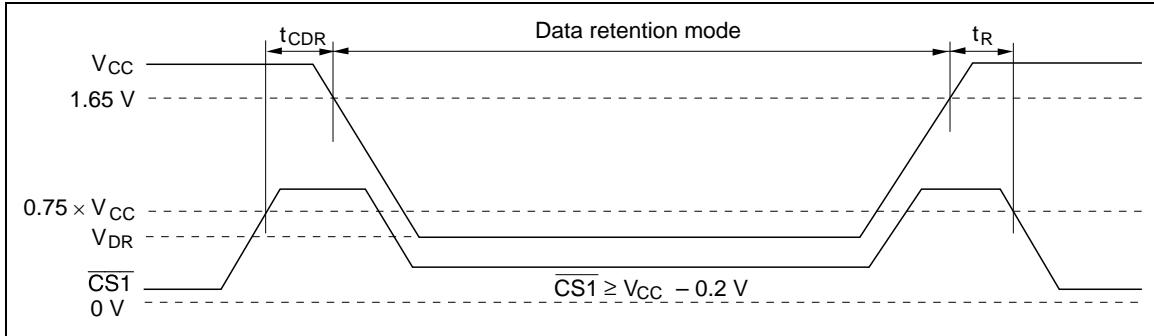
( $T_a = -40$  to  $+85^\circ\text{C}$ )

| Parameter                            | Symbol          | Min | Typ* <sup>4</sup> | Max | Unit          | Test conditions* <sup>3</sup>   |
|--------------------------------------|-----------------|-----|-------------------|-----|---------------|---|
| $V_{CC}$ for data retention          | $V_{DR}$        | 1.0 | —                 | 2.2 | V             | $V_{in} \geq 0$ V<br>(1) $0 \text{ V} \leq \text{CS2} \leq 0.2 \text{ V}$ or<br>(2) $\text{CS2} \geq V_{CC} - 0.2 \text{ V}$ ,<br>$\text{CS1} \geq V_{CC} - 0.2 \text{ V}$ or<br>(3) $\text{LB} = \text{UB} \geq V_{CC} - 0.2 \text{ V}$ ,<br>$\text{CS2} \geq V_{CC} - 0.2 \text{ V}$ ,<br>$\text{CS1} \leq 0.2 \text{ V}$   |
| Data retention current               | $I_{CCDR}^{*1}$ | —   | 0.5               | 25  | $\mu\text{A}$ | $V_{CC} = 1.5 \text{ V}$ , $V_{in} \geq 0 \text{ V}$<br>(1) $0 \text{ V} \leq \text{CS2} \leq 0.2 \text{ V}$ or<br>(2) $\text{CS2} \geq V_{CC} - 0.2 \text{ V}$ ,<br>$\text{CS1} \geq V_{CC} - 0.2 \text{ V}$ or<br>(3) $\text{LB} = \text{UB} \geq V_{CC} - 0.2 \text{ V}$ ,<br>$\text{CS2} \geq V_{CC} - 0.2 \text{ V}$ ,<br>$\text{CS1} \leq 0.2 \text{ V}$<br>Average value |
|                                      | $I_{CCDR}^{*2}$ | —   | 0.5               | 8   | $\mu\text{A}$ |   |
| Chip deselect to data retention time | $t_{CDR}$       | 0   | —                 | —   | ns            | See retention waveforms   |
| Operation recovery time              | $t_R$           | 5   | —                 | —   | ms            |   |

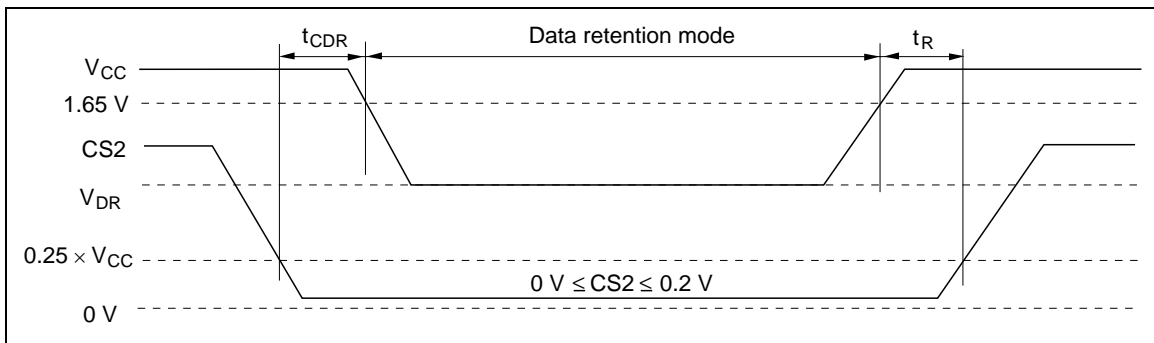
- Notes:
1. This characteristic is guaranteed only for L-version.
  2. This characteristic is guaranteed only for L-SL version.
  3. CS2 controls address buffer, WE buffer, CS1 buffer, OE buffer, LB, UB buffer and Din buffer. If CS2 controls data retention mode,  $V_{in}$  levels (address, WE, OE, CS1, LB, UB, I/O) can be in the high impedance state. If CS1 controls data retention mode, CS2 must be  $\text{CS2} \geq V_{CC} - 0.2 \text{ V}$  or  $0 \text{ V} \leq \text{CS2} \leq 0.2 \text{ V}$ . The other input levels (address, WE, OE, LB, UB, I/O) can be in the high impedance state.
  4. Typical values are at  $V_{CC} = 1.5 \text{ V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.

**HM62A16100I Series**

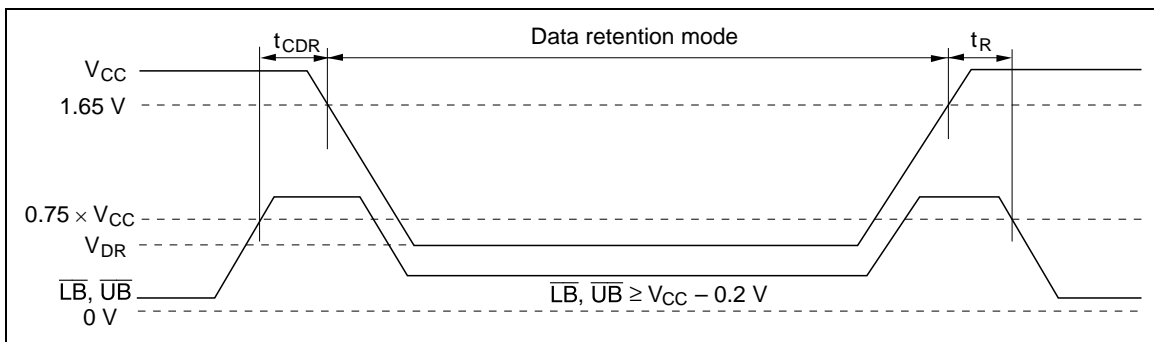
**Low  $V_{CC}$  Data Retention Timing Waveform (1) (CS1 Controlled)**



**Low  $V_{CC}$  Data Retention Timing Waveform (2) (CS2 Controlled)**



**Low  $V_{CC}$  Data Retention Timing Waveform (3) (LB, UB Controlled)**

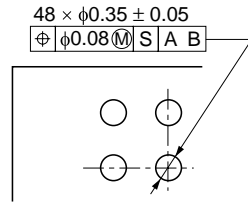
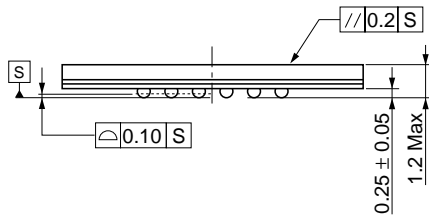
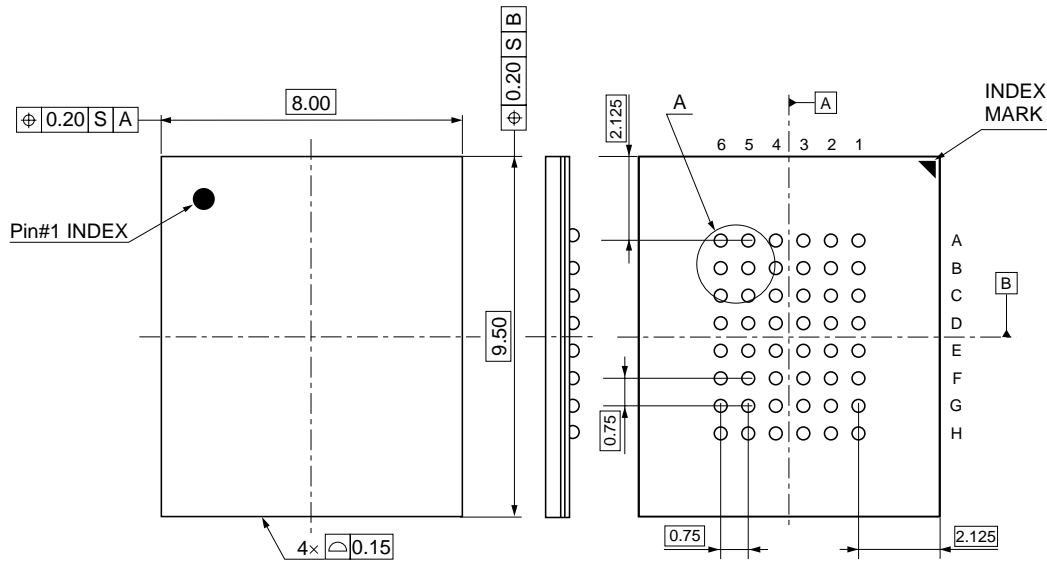


HM62A16100I Series

Package Dimensions

HM62A16100LBPI Series (TBP-48F)

As of January, 2003  
Unit: mm



Details of the part A

|                        |         |
|------------------------|---------|
| Package Code           | TBP-48F |
| JEDEC                  | -       |
| JEITA                  | -       |
| Mass (reference value) | 0.15 g  |



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