R1LV0408C-C Series

4 M SRAM (512-kword × 8-bit)

REJ03C0099-0100Z
Rev. 1.00
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Description

The R1LV0408C-C is a 4-Mbit static RAM organized 512-kword × 8-bit. R1LV0408C-C Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). The R1LV0408C-C Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has packaged in 32-pin SOP, 32-pin TSOP II and 32-pin STSOP.

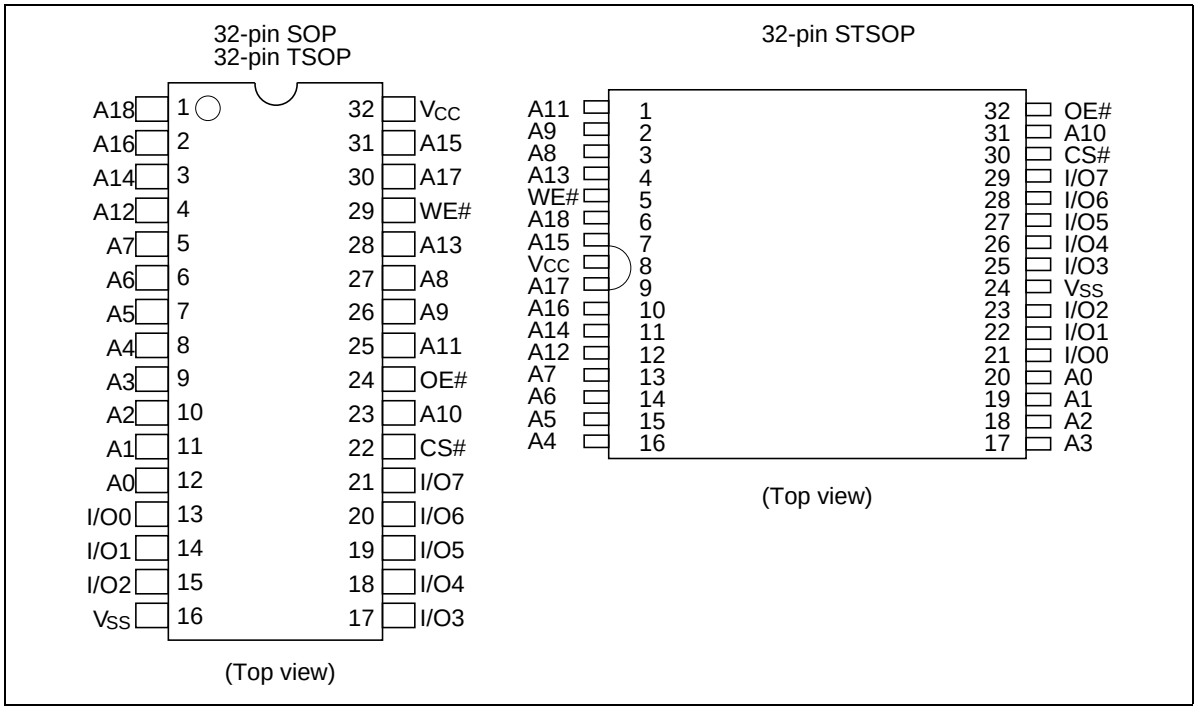
Features

- Single 3 V supply: 2.7 V to 3.6 V
- Access time: 55/70 ns (max)
- Power dissipation:
  - Active: 6 mW/MHz (typ)
  - Standby: 2.4 μW (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Directly TTL compatible.
  - All inputs and outputs
- Battery backup operation.
- Operating temperature: −20 to +70°C

Ordering Information

Type No.	Access time	Package
R1LV0408CSP-5SC	55 ns	525-mil 32-pin plastic SOP (32P2M-A)
R1LV0408CSP-7LC	70 ns	
R1LV0408CSB-5SC	55 ns	400-mil 32-pin plastic TSOP II (32P3Y-H)
R1LV0408CSB-7LC	70 ns	
R1LV0408CSA-5SC	55 ns	8mm × 13.4mm STSOP (32P3K-B)
R1LV0408CSA-7LC	70 ns	

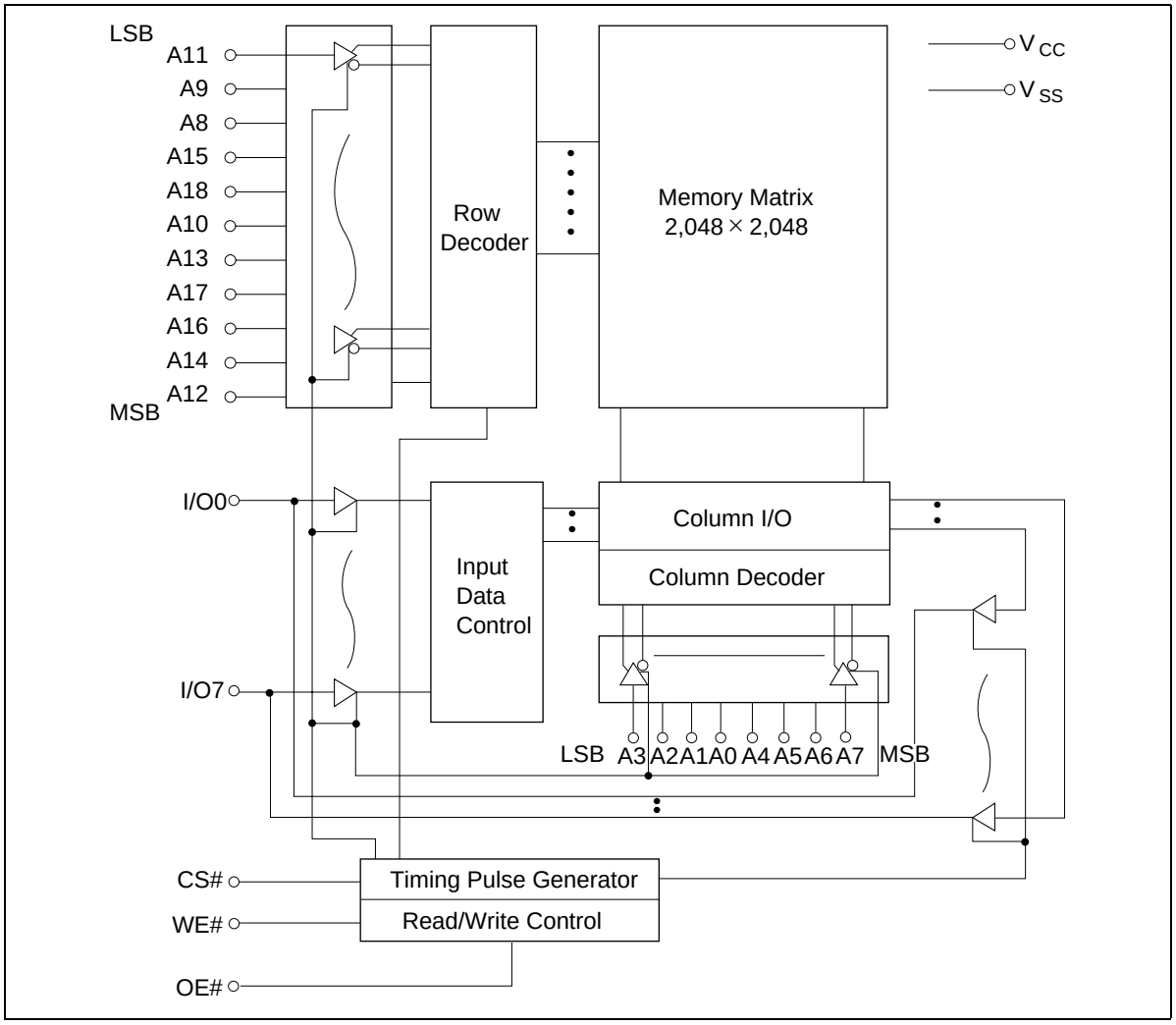
Pin Arrangement



Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CS# ($\overline{CS}$)	Chip select
OE# ($\overline{OE}$)	Output enable
WE# ($\overline{WE}$)	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Operation Table

WE#	CS#	OE#	Mode	V_{CC} current	I/O0 to I/O7	Ref. cycle
×	H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5*[1] to V_{CC} + 0.5*[2]	V
Power dissipation	P_T	0.7	W
Operating temperature	Topr	–20 to +70	°C
Storage temperature range	Tstg	–65 to +150	°C
Storage temperature range under bias	Tbias	–20 to +85	°C

Notes: 1. V_T min: –3.0 V for pulse half-width ≤ 30 ns.
2. Maximum voltage is +7.0 V.

DC Operating Conditions

(Ta = –20 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	–0.3*[1]	—	0.8	V

Note: 1. V_{IL} min: –3.0 V for pulse half-width ≤ 30 ns.

DC Characteristics

Parameter		Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current		$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current		$\|I_{LO}\|$	—	—	1	µA	CS# = V_{IH} or OE# = V_{IH} or WE# = V_{IL} or $V_{I/O}$ = V_{SS} to V_{CC}
Operating current		I_{CC}	—	5	10	mA	CS# = V_{IL}, Others = V_{IH}/ V_{IL}, $I_{I/O}$ = 0 mA
Average operating current		I_{CC1}	—	8	25	mA	Min. cycle, duty = 100%, CS# = V_{IL}, Others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
		I_{CC2}	—	2	5	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, CS# ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby current		I_{SB}	—	0.1	0.3	mA	CS# = V_{IH}
Standby current	to +70°C	I_{SB1}	—	—	16*2	µA	Vin ≥ 0 V, CS# ≥ V_{CC} – 0.2 V
			—	—	8*3	µA	
	to +40°C	I_{SB1}	—	0.7*2	10*2	µA	
			—	0.7*3	3*3	µA	
	–20°C to +25°C	I_{SB1}	—	0.5*2	10*2	µA	
			—	0.5*3	3*3	µA	
Output low voltage		V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
		V_{OL2}	—	—	0.2	V	I_{OL} = 100 µA
Output high voltage		V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA
		V_{OH2}	V_{CC} – 0.2	—	—	V	I_{OH} = –0.1 mA

Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.
2. L version. (–7LC)
3. SL version. (–5SC)

Capacitance

(Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	—	8	pF	Vin = 0 V	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

(Ta = –20 to +70°C, V_{CC} = 2.7 V to 3.6 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{IL} = 0.4 V, V_{IH} = 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C_L (50 pF) (R1LV0408C-5C)
  1 TTL Gate + C_L (100 pF) (R1LV0408C-7C)
  (Including scope and jig)

Read Cycle

		R1LV0408C-C					
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	55	—	70	—	ns	
Address access time	t_{AA}	—	55	—	70	ns	
Chip select access time	t_{CO}	—	55	—	70	ns	
Output enable to output valid	t_{OE}	—	30	—	35	ns	
Chip select to output in low-Z	t_{LZ}	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2
Chip deselect to output in high-Z	t_{HZ}	0	20	0	25	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1, 2
Output hold from address change	t_{OH}	10	—	10	—	ns	

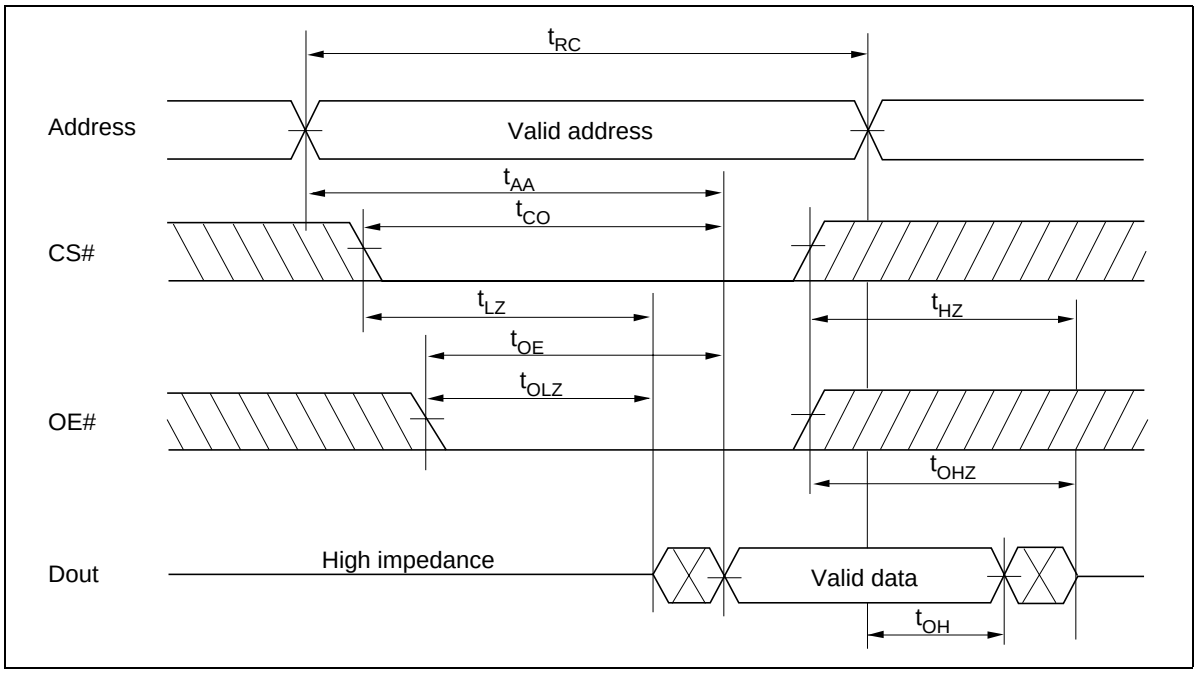
Write Cycle

		R1LV0408C-C					
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	55	—	70	—	ns	
Chip selection to end of write	t_{CW}	50	—	60	—	ns	4
Address setup time	t_{AS}	0	—	0	—	ns	5
Address valid to end of write	t_{AW}	50	—	60	—	ns	
Write pulse width	t_{WP}	40	—	50	—	ns	3, 12
Write recovery time	t_{WR}	0	—	0	—	ns	6
Write to output in high-Z	t_{WHZ}	0	20	0	25	ns	1, 2, 7
Data to write time overlap	t_{DW}	25	—	30	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1, 2, 7

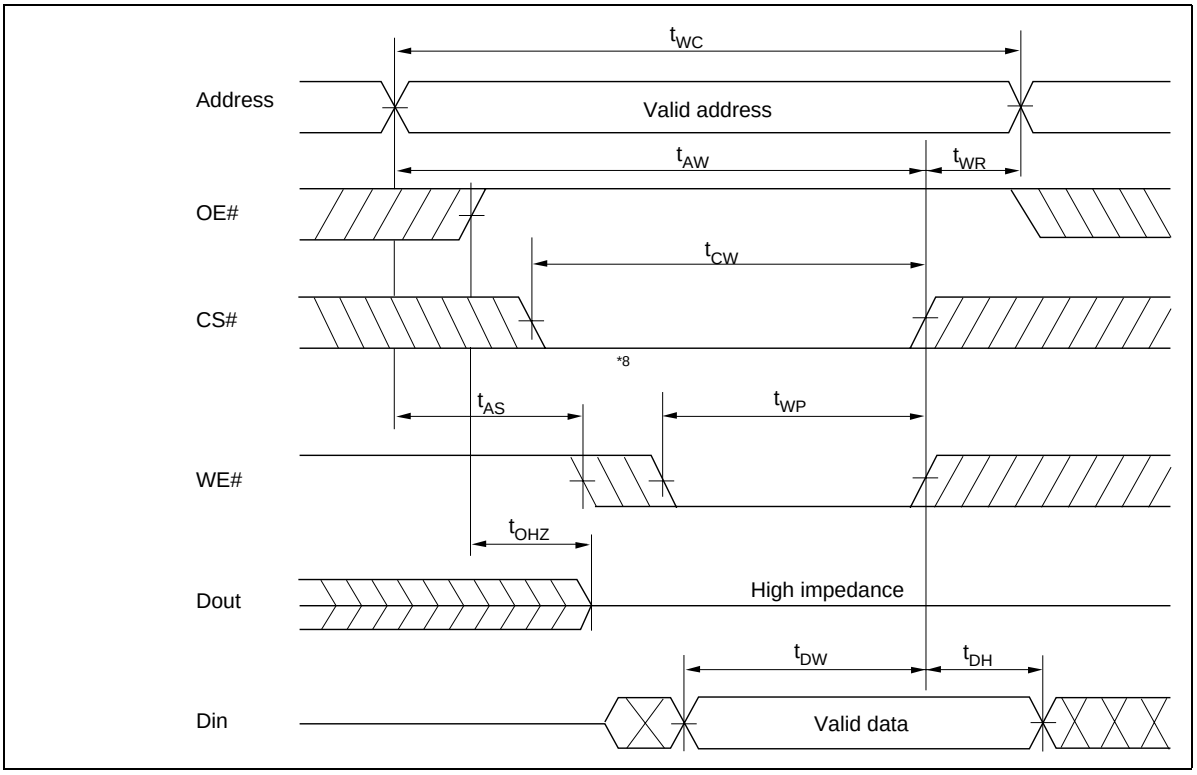
Notes:
1. t_{HZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. A write occurs during the overlap (t_{WP}) of a low CS# and a low WE#. A write begins at the later transition of CS# going low or WE# going low. A write ends at the earlier transition of CS# going high or WE# going high. t_{WP} is measured from the beginning of write to the end of write.
4. t_{CW} is measured from CS# going low to the end of write.
5. t_{AS} is measured from the address valid to the beginning of write.
6. t_{WR} is measured from the earlier of WE# or CS# going high to the end of write cycle.
7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
8. If the CS# low transition occurs simultaneously with the WE# low transition or after the WE# transition, the output remain in a high impedance state.
9. Dout is the same phase of the write data of this write cycle.
10. Dout is the read data of next address.
11. If CS# is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
12. In the write cycle with OE# low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW}$ min + t_{WHZ} max

Timing Waveform

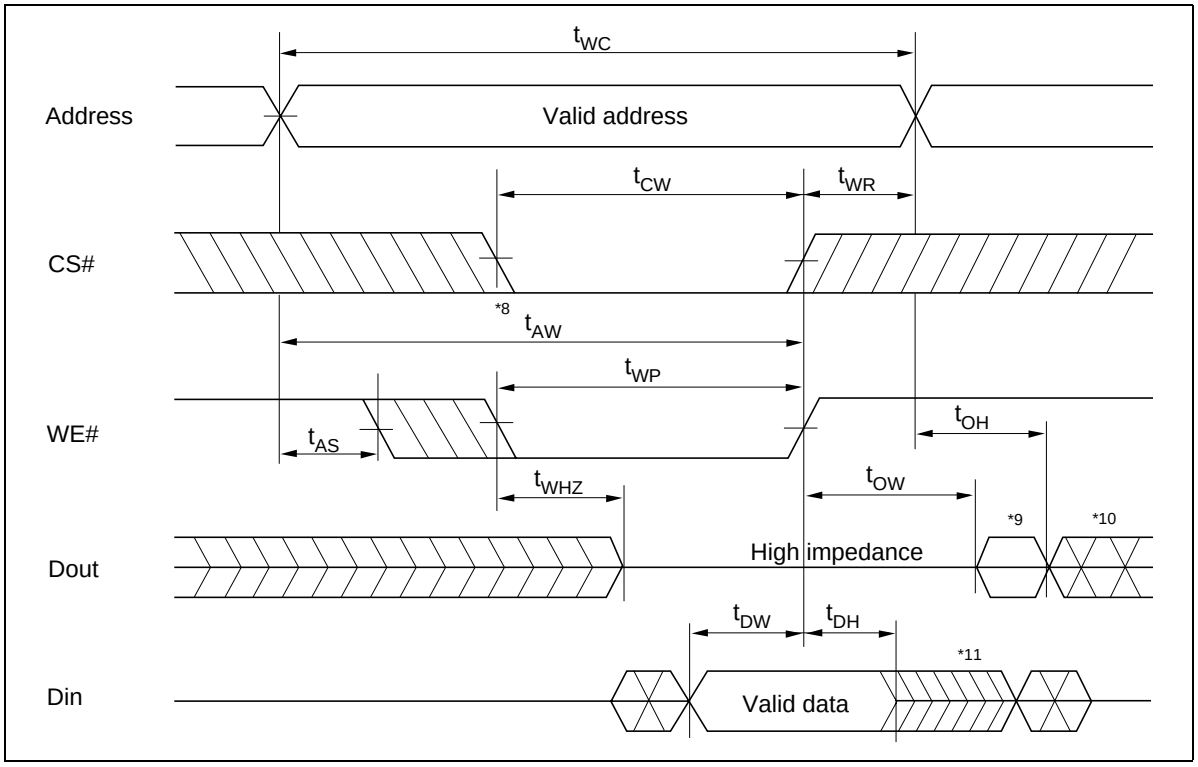
Read Timing Waveform (WE# = V_{IH})



Write Timing Waveform (1) (OE# Clock)



Write Timing Waveform (2) (OE# Low Fixed)



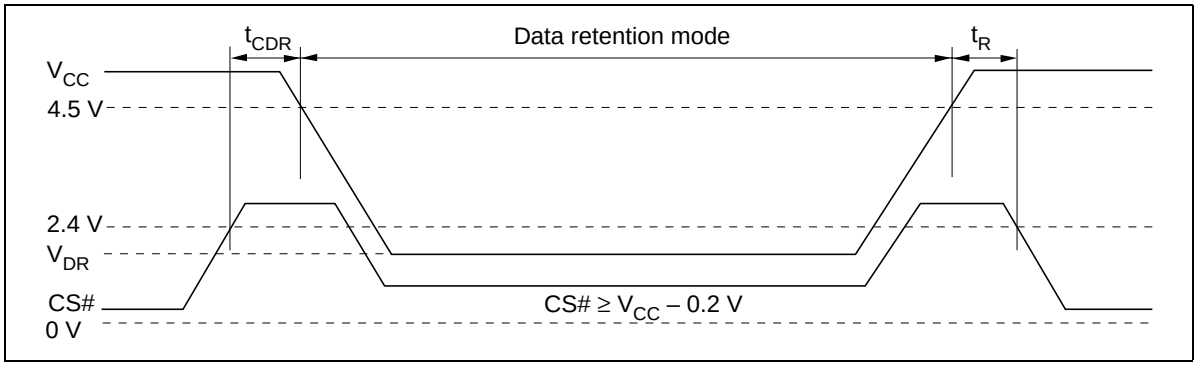
Low V_{CC} Data Retention Characteristics

(Ta = –20 to +70°C)

Parameter		Symbol	Min	Typ*4	Max	Unit	Test conditions*3
V_{CC} for data retention		V_{DR}	2	—	—	V	CS# ≥ V_{CC} – 0.2 V, Vin ≥ 0 V
Data retention current	to +70°C	I_{CCDR}*1	—	—	16	µA	V_{CC} = 3.0 V, Vin ≥ 0 V
		I_{CCDR}*2	—	—	8		CS# ≥ V_{CC} – 0.2 V
	to +40°C	I_{CCDR}*1	—	0.7	10	µA	
		I_{CCDR}*2	—	0.7	3		
	–20°C to +25°C	I_{CCDR}*1	—	0.5	10	µA	
		I_{CCDR}*2	—	0.5	3		
Chip deselect to data retention time		t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time		t_R	t_{RC}*5	—	—	ns	

Notes: 1. This characteristic is guaranteed only for L version.
2. This characteristic is guaranteed only for SL version.
3. CS# controls address buffer, WE# buffer, OE# buffer, and Din buffer. In data retention mode, Vin levels (address, WE#, OE#, I/O) can be in the high impedance state.
4. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.
5. t_{RC} = read cycle time.

Low V_{CC} Data Retention Timing Waveform (CS# Controlled)



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.00	Jul. 24, 2003	Initial issue		