

To all our customers

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## **Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.**

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The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**MITSUBISHI MICROCOMPUTERS**  
**M37920S4CGP**

16-BIT CMOS MICROCOMPUTER

**DESCRIPTION**

The M37920S4CGP is a single-chip microcomputers designed with high-performance CMOS silicon gate technology. These are housed in 100-pin plastic molded QFP. This microcomputer supports the 7900 Series instruction set, which are enhanced and expanded instruction set and are upper-compatible with the 7700/7751 Series instruction set.

The CPU of this microcomputer is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. Also, the bus interface unit of this microcomputer enhance the memory access efficiency to execute instructions fast. This microcomputer include the 4-channel DMA controller and the DRAM controller with enhanced fast page mode. Therefore, this microcomputer are suitable for office, business, and industrial equipment controller that require fast processing of large data.

- Instruction execution time
  - The fastest instruction at 20 MHz frequency ..... 50 ns
- Single power supply ..... 5 V ± 0.5 V
- Interrupts ..... 6 external sources, 17 internal sources, 7 levels
- Multi-functional 16-bit timer ..... 5 + 3
- Serial I/O (UART or Clock synchronous) ..... 2
- 10-bit A-D converter ..... 4-channel inputs
- DMA controller ..... 4-channels
- DRAM controller
- Real-time output
  - .... 4 bits × 2 channels, or 6 bits × 1 channel + 2 bits × 1 channel
- 12-bit watchdog timer
- Programmable input/output (ports P2–P9, P12) ..... 49

**DISTINCTIVE FEATURES**

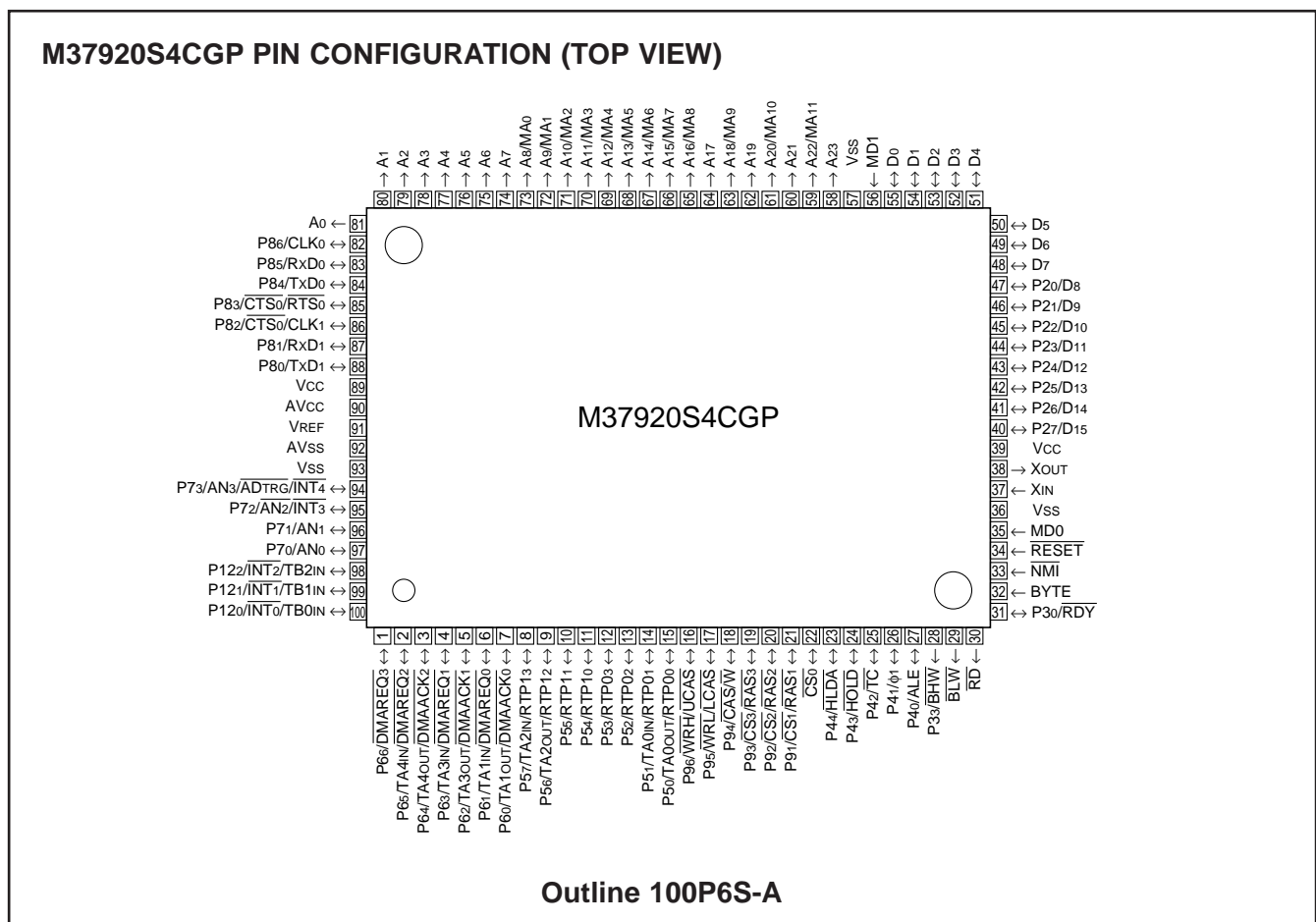
<Microcomputer mode>

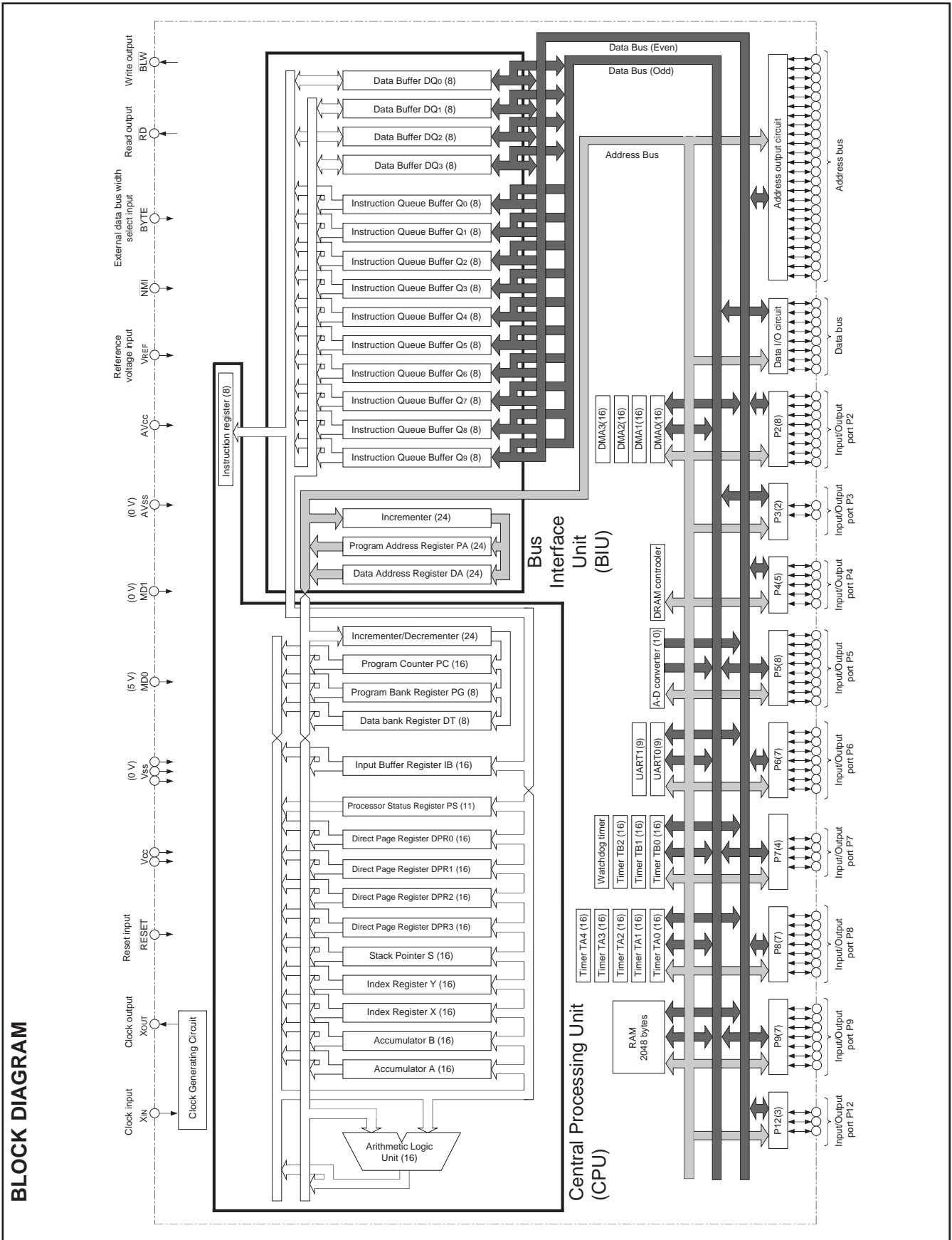
- Number of basic machine instructions ..... 203
- Memory
  - RAM ..... 2048 bytes
  - ROM ..... External

**APPLICATION**

Telecommunications equipment such as copiers, printers, typewriters, facsimiles, optical disk drives, HDD, mobile radio communication equipment, ISDN terminals

Control devices for office automation equipment such as personal computers





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**FUNCTIONS (Microcomputer mode)**

Parameter		Functions
Number of basic machine instructions		203
Instruction execution time		50 ns (the fastest instruction at $f(X_{IN}) = 20$ MHz)
External clock input frequency $f(X_{IN})$		20 MHz (Max.)
Memory size	ROM	External
	RAM	2048 bytes
Programmable input/output ports	P2, P5	8-bit X 2
	P3	2-bit X 1
	P4	5-bit X 1
	P6, P8	7-bit X 2
	P7	4-bit X 1
	P9	6-bit X 1
	P12	3-bit X 1
Multi-functional timers	TA0–TA4	16-bit X 5
	TB0–TB2	16-bit X 3
Serial I/O	UART0 and UART1	(UART or Clock synchronous serial I/O) X 2
A-D converter		10-bit successive approximation method X 1 (4 channels)
Watchdog timer		12-bit X 1
DMA controller		4 channels Maximum transfer rate    20 Mbytes/sec. (at $f(X_{IN}) = 20$ MHz, 0 wait, 1-bus cycle transfer) 10 Mbytes/sec. (at $f(X_{IN}) = 20$ MHz, 0 wait, 2-bus cycles transfer)
DRAM controller		1 channel Supports fast page access mode. Incorporates 8-bit refresh timer. Supports CAS before RAS refresh method or self refresh method.
Chip-select wait control		Chip select area X 4 ( $\overline{CS}_0$ – $\overline{CS}_3$ ). A wait number and bus width can be set for each chip select area.
Real-time output		4 bits X 2 channels; or 6 bits X 1 channel + 2 bits X 1 channel
Interrupts		6 external types, 17 internal types. Each interrupt except $\overline{NMI}$ can be set to a priority level within the range of 0–7 by software.
Clock generating circuit		Built-in (externally connected to a ceramic resonator or quartz crystal resonator).
Power supply voltage		5 V $\pm$ 10 %
Power dissipation		135 mW (at $f(X_{IN}) = 20$ MHz, typ.)
Ports' input/output characteristics	Input/Output withstand voltage	5 V
	Output current	5 mA
Memory expansion		Up to 16 Mbytes. Note that bank FF16 is a reserved area.
Operating temperature range		–20 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		100-pin plastic molded QFP

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**PIN DESCRIPTION (Microcomputer mode)**

Pin	Name	Input/ Output	Functions
Vcc, Vss	Power supply input	—	Apply 5 V±10 % to Vcc, and 0 V to Vss.
MD0	MD0	Input	This pin controls the processor mode. Connect this pin to Vcc.
MD1	MD1	Input	Connect this pin to Vss.
$\overline{\text{RESET}}$	Reset input	Input	The microcomputer is reset when “L” level is applies to this pin.
XIN	Clock input	Input	These are input and output pins of the internal clock generating circuit. Connect a ceramic or quartz- crystal resonator between the XIN and XOUT pins. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.
XOUT	Clock output	Output	
BYTE	External data bus width select input	Input	This pin determines whether the external data bus has an 8-bit width or 16-bit width for the memory expansion mode or microprocessor mode. The width is 16 bits when “L” signal is input, and 8 bits when “H” signal is input.
AVcc, AVss	Analog power supply input	—	Power supply input pin for the A-D converter. Connect AVcc to Vcc, and AVss to Vss externally.
VREF	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter.
A0–A7	Low-order address	Output	The low-order 8 bits of address (A0–A7) are output.
A8–A15/ MA0–MA7	Middle-order address/ DRAM address	Output	The middle-order 8 bits of address (A8–A15) are input/output. While DRAM space is accessed, multiplexed address (MA0–MA7) is output.
A16–A23/ MA8–MA11	High-order address/ DRAM address	Output	The high-order 8 bits of address (A16–A23) are output. While DRAM space is accessed, multiplexed address (MA8–MA11) is output.
D0–D7	Low-order data	I/O	The low-order 8 bits of data (D0–D7) are input/output.
P20/D8– P27/D15	I/O port P2/ High-order data	I/O	<ul style="list-style-type: none"> <li>■ When 8-bit external data bus is used (BYTE = “H” level) Port P2 is an 8-bit I/O port.</li> <li>■ When 16-bit external data bus is used (BYTE = “L” level) The high-order 8 bits (D8–D15) are input/output.</li> </ul>
P30/ $\overline{\text{RDY}}$ , $\overline{\text{RD}}$ , $\overline{\text{BLW}}$ , P33/ $\overline{\text{BHW}}$	Memory control signal I/O	Input Output Output Output	<p>While the input level at pin <math>\overline{\text{RDY}}</math> is “L”, the microcomputer is placed in the ready state. While pin <math>\overline{\text{RD}}</math> is at “L” level, the microcomputer reads out data and instruction codes. Also, pin <math>\overline{\text{RDY}}</math> can function as a programmable I/O port pin (P30) by software.</p> <ul style="list-style-type: none"> <li>■ When 8-bit external data bus is used (BYTE = “H” level) While pin <math>\overline{\text{BLW}}</math> is at “L” level, the microcomputer writes data.</li> <li>■ When 16-bit external data bus is used (BYTE = “L” level) While pin <math>\overline{\text{BLW}}</math> is at “L” level, the microcomputer writes data into an even-numbered address. While pin <math>\overline{\text{BHW}}</math> is at “L” level, the microcomputer writes data into an odd-numbered address.</li> </ul>
P40/ALE, P41/ $\phi_1$ , P42/ $\overline{\text{TC}}$ , P43/ $\overline{\text{HOLD}}$ , P44/ $\overline{\text{HLDA}}$	I/O port P4	Output Output I/O Input Output	Signal ALE is used to latch an address. $\phi_1$ has the same period as internal clock $\phi$ . Pin P42 functions as a programmable I/O port pin. While the input level at pin $\overline{\text{HOLD}}$ is at “L” level, the microcomputer is placed in the hold state. Signal $\overline{\text{HLDA}}$ is used to inform the external that the microcomputer enters the hold state. By software, pin ALE, clock $\phi_1$ output pin, and pins $\overline{\text{HOLD}}$ , $\overline{\text{HLDA}}$ function as programmable I/O port pins (P40, P41, P43, P44). Pin P42 also functions as pin TC.
P50–P57	I/O port P5	I/O	Port P5 is an 8-bit I/O port. These pins also function as I/O pins for timers A0, A2, and pulse output pins for the real-time output.
P60–P66	I/O port P6	I/O	Port P6 is a 7-bit I/O port. These pins also function as I/O pins for timers A1, A3, A4, input pins for DMA requests, and output pins for DMA acknowledge signals.

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Pin	Name	Input/ Output	Functions
P70–P73	I/O port P7	I/O	Port P7 is a 4-bit I/O port. P72 and P73 also function as input pins for $\overline{INT3}$ and $\overline{INT4}$ . According to the software setting, these pins also function as input pins for the A-D converter.
P80–P86	I/O port P8	I/O	Port P8 is a 7-bit I/O port. These pins also function as I/O pins for UART0, UART1.
$\overline{CS0}$	Chip-select output	Output	This is an output pin for $\overline{CS0}$ .
P91–P96	I/O port P9	I/O	Port P9 is a 6-bit I/O port. According to the software setting, P91–P93 also function as chip select output pins. While DRAM space is selected, P94–P96 function as output pins for DRAM control signals.
P120–P122	I/O port P12	I/O	Port P12 is a 3-bit I/O port. These pins also function as input pins for $\overline{INT0}$ , $\overline{INT1}$ , $\overline{INT2}$ . According to software setting, these pins also function as input pins for timers B0–B2.
$\overline{NMI}$	Non-maskable interrupt	Input	This pin is for a non-maskable interrupt.

**BASIC FUNCTION BLOCKS**

The M37920S4CGP is the same functions as the M37920F8CGP except for the following.

Therefore, refer to the datasheet of the M37920F8CGP.

- The M37920S4CGP does not include the internal flash memory.
- The M37920S4CGP operates only in the microprocessor mode.
- The M37920S4CGP does not have the flash memory control register (address 9E16).
- Some of programmable I/O ports of the M37920S4CGP differ from those of the M37920FGCGP.

**MEMORY**

Figure 1 shows the memory map.

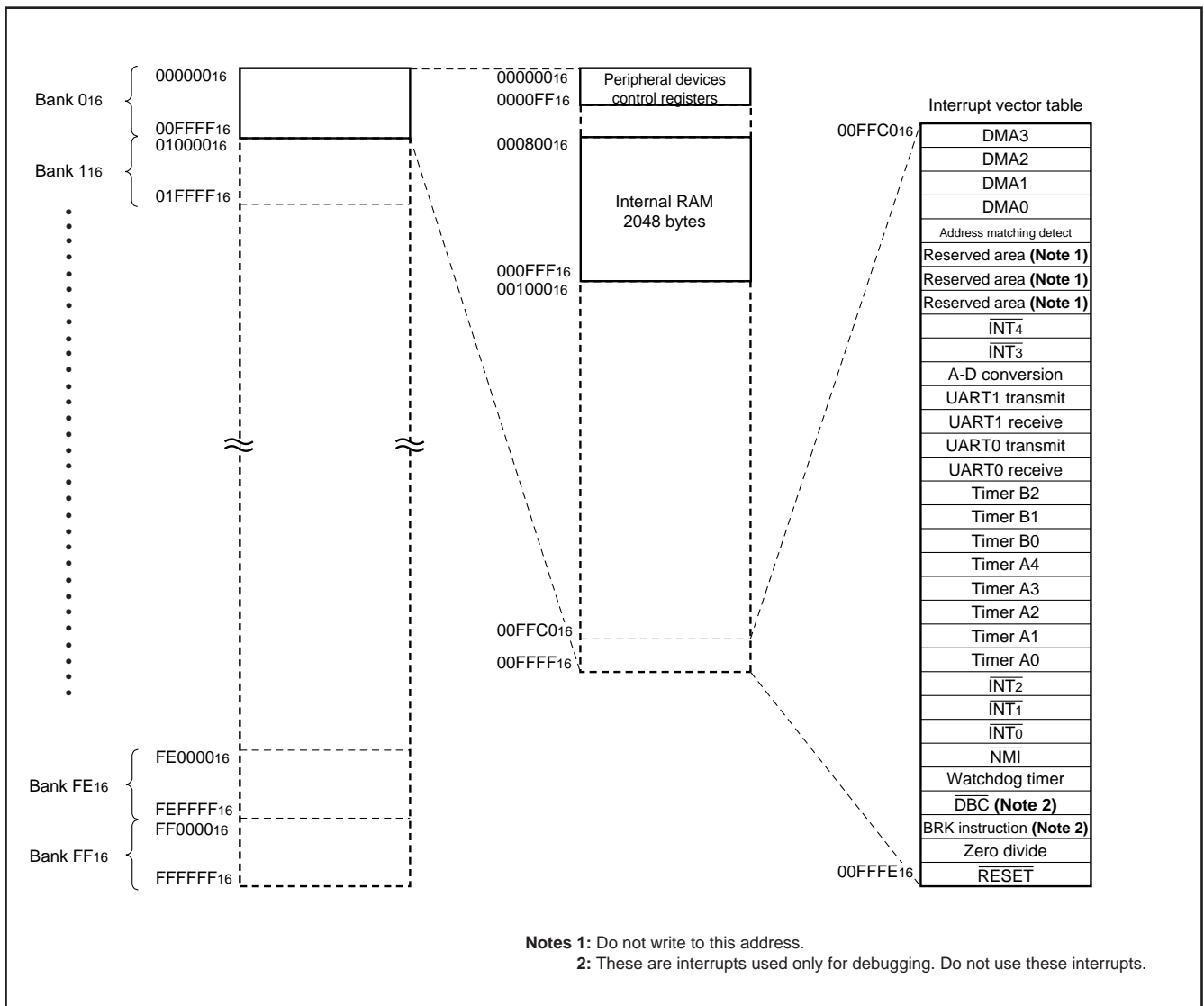


Fig. 1 Memory map

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Address (Hexadecimal notation)		Address (Hexadecimal notation)	
000000 <sub>16</sub>	Reserved area (Note 1)	000040 <sub>16</sub>	Count start register
000001 <sub>16</sub>	Reserved area (Note 1)	000041 <sub>16</sub>	
000002 <sub>16</sub>	[Port P0 register] (Note 2)	000042 <sub>16</sub>	One-shot start register
000003 <sub>16</sub>	[Port P1 register] (Note 2)	000043 <sub>16</sub>	
000004 <sub>16</sub>	[Port P0 direction register] (Note 2)	000044 <sub>16</sub>	Up-down register
000005 <sub>16</sub>	[Port P1 direction register] (Note 2)	000045 <sub>16</sub>	Timer A clock division select register
000006 <sub>16</sub>	Port P2 register	000046 <sub>16</sub>	Timer A0 register
000007 <sub>16</sub>	Port P3 register	000047 <sub>16</sub>	
000008 <sub>16</sub>	Port P2 direction register	000048 <sub>16</sub>	Timer A1 register
000009 <sub>16</sub>	Port P3 direction register	000049 <sub>16</sub>	
00000A <sub>16</sub>	Port P4 register	00004A <sub>16</sub>	Timer A2 register
00000B <sub>16</sub>	Port P5 register	00004B <sub>16</sub>	
00000C <sub>16</sub>	Port P4 direction register	00004C <sub>16</sub>	Timer A3 register
00000D <sub>16</sub>	Port P5 direction register	00004D <sub>16</sub>	
00000E <sub>16</sub>	Port P6 register	00004E <sub>16</sub>	Timer A4 register
00000F <sub>16</sub>	Port P7 register	00004F <sub>16</sub>	
000010 <sub>16</sub>	Port P6 direction register	000050 <sub>16</sub>	Timer B0 register
000011 <sub>16</sub>	Port P7 direction register	000051 <sub>16</sub>	
000012 <sub>16</sub>	Port P8 register	000052 <sub>16</sub>	Timer B1 register
000013 <sub>16</sub>	Port P9 register	000053 <sub>16</sub>	
000014 <sub>16</sub>	Port P8 direction register	000054 <sub>16</sub>	Timer B2 register
000015 <sub>16</sub>	Port P9 direction register	000055 <sub>16</sub>	
000016 <sub>16</sub>	[Port P10 register] (Note 2)	000056 <sub>16</sub>	Timer A0 mode register
000017 <sub>16</sub>	[Port P11 register] (Note 2)	000057 <sub>16</sub>	Timer A1 mode register
000018 <sub>16</sub>	[Port P10 direction register] (Note 2)	000058 <sub>16</sub>	Timer A2 mode register
000019 <sub>16</sub>	[Port P11 direction register] (Note 2)	000059 <sub>16</sub>	Timer A3 mode register
00001A <sub>16</sub>	Port P12 register	00005A <sub>16</sub>	Timer A4 mode register
00001B <sub>16</sub>		00005B <sub>16</sub>	Timer B0 mode register
00001C <sub>16</sub>	Port P12 direction register	00005C <sub>16</sub>	Timer B1 mode register
00001D <sub>16</sub>		00005D <sub>16</sub>	Timer B2 mode register
00001E <sub>16</sub>	A-D control register 0	00005E <sub>16</sub>	Processor mode register 0
00001F <sub>16</sub>	A-D control register 1	00005F <sub>16</sub>	Processor mode register 1
000020 <sub>16</sub>	A-D register 0	000060 <sub>16</sub>	Watchdog timer register
000021 <sub>16</sub>		000061 <sub>16</sub>	Watchdog timer frequency select register
000022 <sub>16</sub>	A-D register 1	000062 <sub>16</sub>	Particular function select register 0
000023 <sub>16</sub>		000063 <sub>16</sub>	Particular function select register 1
000024 <sub>16</sub>	A-D register 2	000064 <sub>16</sub>	Particular function select register 2
000025 <sub>16</sub>		000065 <sub>16</sub>	Reserved area (Note 1)
000026 <sub>16</sub>	A-D register 3	000066 <sub>16</sub>	Debug control register 0
000027 <sub>16</sub>		000067 <sub>16</sub>	Debug control register 1
000028 <sub>16</sub>		000068 <sub>16</sub>	
000029 <sub>16</sub>		000069 <sub>16</sub>	Address comparison register 0
00002A <sub>16</sub>		00006A <sub>16</sub>	
00002B <sub>16</sub>		00006B <sub>16</sub>	
00002C <sub>16</sub>		00006C <sub>16</sub>	Address comparison register 1
00002D <sub>16</sub>		00006D <sub>16</sub>	
00002E <sub>16</sub>		00006E <sub>16</sub>	INT <sub>3</sub> interrupt control register
00002F <sub>16</sub>		00006F <sub>16</sub>	INT <sub>4</sub> interrupt control register
000030 <sub>16</sub>	UART0 transmit/receive mode register	000070 <sub>16</sub>	A-D conversion interrupt control register
000031 <sub>16</sub>	UART0 baud rate register (BRG0)	000071 <sub>16</sub>	UART0 transmit interrupt control register
000032 <sub>16</sub>	UART0 transmit buffer register	000072 <sub>16</sub>	UART0 receive interrupt control register
000033 <sub>16</sub>		000073 <sub>16</sub>	UART1 transmit interrupt control register
000034 <sub>16</sub>	UART0 transmit/receive control register 0	000074 <sub>16</sub>	UART1 receive interrupt control register
000035 <sub>16</sub>	UART0 transmit/receive control register 1	000075 <sub>16</sub>	Timer A0 interrupt control register
000036 <sub>16</sub>		000076 <sub>16</sub>	Timer A1 interrupt control register
000037 <sub>16</sub>	UART0 receive buffer register	000077 <sub>16</sub>	Timer A2 interrupt control register
000038 <sub>16</sub>	UART1 transmit/receive mode register	000078 <sub>16</sub>	Timer A3 interrupt control register
000039 <sub>16</sub>	UART1 baud rate register (BRG1)	000079 <sub>16</sub>	Timer A4 interrupt control register
00003A <sub>16</sub>		00007A <sub>16</sub>	Timer B0 interrupt control register
00003B <sub>16</sub>	UART1 transmit buffer register	00007B <sub>16</sub>	Timer B1 interrupt control register
00003C <sub>16</sub>	UART1 transmit/receive control register 0	00007C <sub>16</sub>	Timer B2 interrupt control register
00003D <sub>16</sub>	UART1 transmit/receive control register 1	00007D <sub>16</sub>	INT <sub>0</sub> interrupt control register
00003E <sub>16</sub>		00007E <sub>16</sub>	INT <sub>1</sub> interrupt control register
00003F <sub>16</sub>	UART1 receive buffer register	00007F <sub>16</sub>	INT <sub>2</sub> interrupt control register

**Notes 1:** Do not read/write to this address.  
**2:** These registers are used in the bus fixation of the power saving function. For details, refer to the section on the power saving function of the M37920F8CGP datasheet.

Fig. 2 Location of peripheral devices' control registers (1)



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Address (Hexadecimal notation)		Address (Hexadecimal notation)	
000080 <sup>16</sup>	CS <sub>0</sub> control register L	0000C0 <sup>16</sup>	Source address register 0 L
000081 <sup>16</sup>	CS <sub>0</sub> control register H	0000C1 <sup>16</sup>	Source address register 0 M
000082 <sup>16</sup>	CS <sub>1</sub> control register L	0000C2 <sup>16</sup>	Source address register 0 H
000083 <sup>16</sup>	CS <sub>1</sub> control register H	0000C3 <sup>16</sup>	
000084 <sup>16</sup>	CS <sub>2</sub> control register L	0000C4 <sup>16</sup>	Destination address register 0 L
000085 <sup>16</sup>	CS <sub>2</sub> control register H	0000C5 <sup>16</sup>	Destination address register 0 M
000086 <sup>16</sup>	CS <sub>3</sub> control register L	0000C6 <sup>16</sup>	Destination address register 0 H
000087 <sup>16</sup>	CS <sub>3</sub> control register H	0000C7 <sup>16</sup>	
000088 <sup>16</sup>		0000C8 <sup>16</sup>	Transfer counter register 0 L
000089 <sup>16</sup>		0000C9 <sup>16</sup>	Transfer counter register 0 M
00008A <sup>16</sup>	Area CS <sub>0</sub> start address register	0000CA <sup>16</sup>	Transfer counter register 0 H
00008B <sup>16</sup>		0000CB <sup>16</sup>	
00008C <sup>16</sup>	Area CS <sub>1</sub> start address register	0000CC <sup>16</sup>	DMA0 mode register L
00008D <sup>16</sup>		0000CD <sup>16</sup>	DMA0 mode register H
00008E <sup>16</sup>	Area CS <sub>2</sub> start address register	0000CE <sup>16</sup>	DMA0 control register
00008F <sup>16</sup>		0000CF <sup>16</sup>	
000090 <sup>16</sup>	Area CS <sub>3</sub> start address register	0000D0 <sup>16</sup>	Source address register 1 L
000091 <sup>16</sup>		0000D1 <sup>16</sup>	Source address register 1 M
000092 <sup>16</sup>		0000D2 <sup>16</sup>	Source address register 1 H
000093 <sup>16</sup>		0000D3 <sup>16</sup>	
000094 <sup>16</sup>		0000D4 <sup>16</sup>	Destination address register 1 L
000095 <sup>16</sup>		0000D5 <sup>16</sup>	Destination address register 1 M
000096 <sup>16</sup>		0000D6 <sup>16</sup>	Destination address register 1 H
000097 <sup>16</sup>		0000D7 <sup>16</sup>	
000098 <sup>16</sup>		0000D8 <sup>16</sup>	Transfer counter register 1 L
000099 <sup>16</sup>		0000D9 <sup>16</sup>	Transfer counter register 1 M
00009A <sup>16</sup>		0000DA <sup>16</sup>	Transfer counter register 1 H
00009B <sup>16</sup>		0000DB <sup>16</sup>	
00009C <sup>16</sup>	Reserved area (Note 1)	0000DC <sup>16</sup>	DMA1 mode register L
00009D <sup>16</sup>	Reserved area (Note 1)	0000DD <sup>16</sup>	DMA1 mode register H
00009E <sup>16</sup>	Reserved area (Note 1)	0000DE <sup>16</sup>	DMA1 control register
00009F <sup>16</sup>		0000DF <sup>16</sup>	
0000A0 <sup>16</sup>	Real-time output control register	0000E0 <sup>16</sup>	Source address register 2 L
0000A1 <sup>16</sup>		0000E1 <sup>16</sup>	Source address register 2 M
0000A2 <sup>16</sup>	Pulse output data register 0	0000E2 <sup>16</sup>	Source address register 2 H
0000A3 <sup>16</sup>		0000E3 <sup>16</sup>	
0000A4 <sup>16</sup>	Pulse output data register 1	0000E4 <sup>16</sup>	Destination address register 2 L
0000A5 <sup>16</sup>		0000E5 <sup>16</sup>	Destination address register 2 M
0000A6 <sup>16</sup>	Reserved area (Note 1)	0000E6 <sup>16</sup>	Destination address register 2 H
0000A7 <sup>16</sup>		0000E7 <sup>16</sup>	
0000A8 <sup>16</sup>	DRAM control register	0000E8 <sup>16</sup>	Transfer counter register 2 L
0000A9 <sup>16</sup>	Refresh timer	0000E9 <sup>16</sup>	Transfer counter register 2 M
0000AA <sup>16</sup>		0000EA <sup>16</sup>	Transfer counter register 2 H
0000AB <sup>16</sup>		0000EB <sup>16</sup>	
0000AC <sup>16</sup>	CTS/RTS separate select register	0000EC <sup>16</sup>	DMA2 mode register L
0000AD <sup>16</sup>		0000ED <sup>16</sup>	DMA2 mode register H
0000AE <sup>16</sup>		0000EE <sup>16</sup>	DMA2 control register
0000AF <sup>16</sup>		0000EF <sup>16</sup>	
0000B0 <sup>16</sup>	DMAC control register L	0000F0 <sup>16</sup>	Source address register 3 L
0000B1 <sup>16</sup>	DMAC control register H	0000F1 <sup>16</sup>	Source address register 3 M
0000B2 <sup>16</sup>	DMA0 interrupt control register	0000F2 <sup>16</sup>	Source address register 3 H
0000B3 <sup>16</sup>	DMA1 interrupt control register	0000F3 <sup>16</sup>	
0000B4 <sup>16</sup>	DMA2 interrupt control register	0000F4 <sup>16</sup>	Destination address register 3 L
0000B5 <sup>16</sup>	DMA3 interrupt control register	0000F5 <sup>16</sup>	Destination address register 3 M
0000B6 <sup>16</sup>		0000F6 <sup>16</sup>	Destination address register 3 H
0000B7 <sup>16</sup>		0000F7 <sup>16</sup>	
0000B8 <sup>16</sup>		0000F8 <sup>16</sup>	Transfer counter register 3 L
0000B9 <sup>16</sup>		0000F9 <sup>16</sup>	Transfer counter register 3 M
0000BA <sup>16</sup>		0000FA <sup>16</sup>	Transfer counter register 3 H
0000BB <sup>16</sup>		0000FB <sup>16</sup>	
0000BC <sup>16</sup>	Reserved area (Note 1)	0000FC <sup>16</sup>	DMA3 mode register L
0000BD <sup>16</sup>	Reserved area (Note 1)	0000FD <sup>16</sup>	DMA3 mode register H
0000BE <sup>16</sup>	Reserved area (Note 1)	0000FE <sup>16</sup>	DMA3 control register
0000BF <sup>16</sup>	Reserved area (Note 1)	0000FF <sup>16</sup>	

**Note 1:** Do not read/write to this address.

Fig. 3 Location of peripheral devices' control registers (2)

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### Processor mode

The M37920S4CGP operates only in the microprocessor mode exclusive for the external ROM. Be sure to fix the level at pin MD0 to Vcc and the level at pin MD1 to Vss. Also, be sure to fix bits 1, 0 at address 5E16 (the processor mode register 0) to "1" and "0", respectively.

### Microprocessor mode

When the microcomputer starts its operation after reset with the level at pin MD0 = Vcc level (5 V), the microcomputer is placed in the microprocessor mode.

Table 1. Relationship between pins MD0, MD1 and processor mode

Pin MD0	Pin MD1	Processor mode
Vcc level (5 V)	Vss level (5 V)	After reset, the microcomputer starts its operation in the microprocessor mode. (Be sure to pin MD0 to Vcc level.)

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

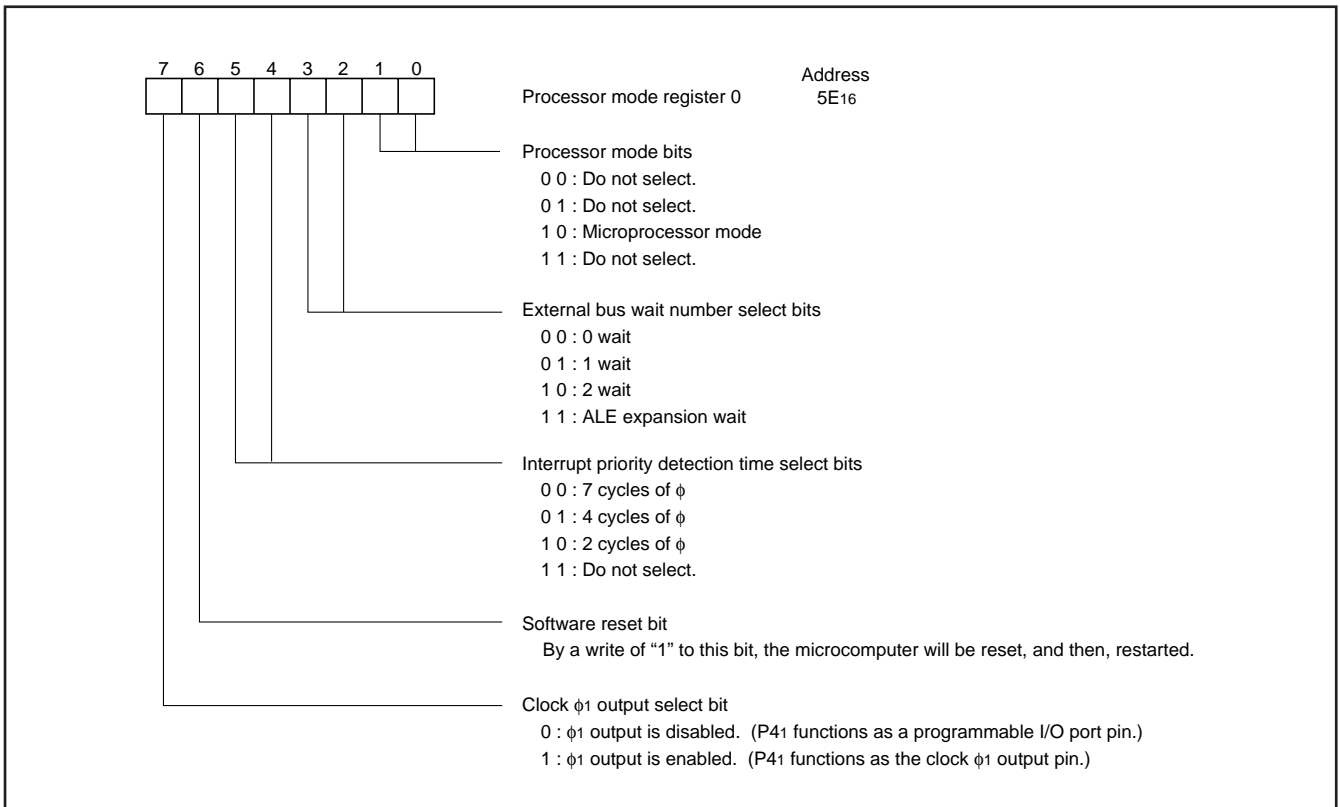


Fig. 4 Processor mode register 0's bit configuration

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

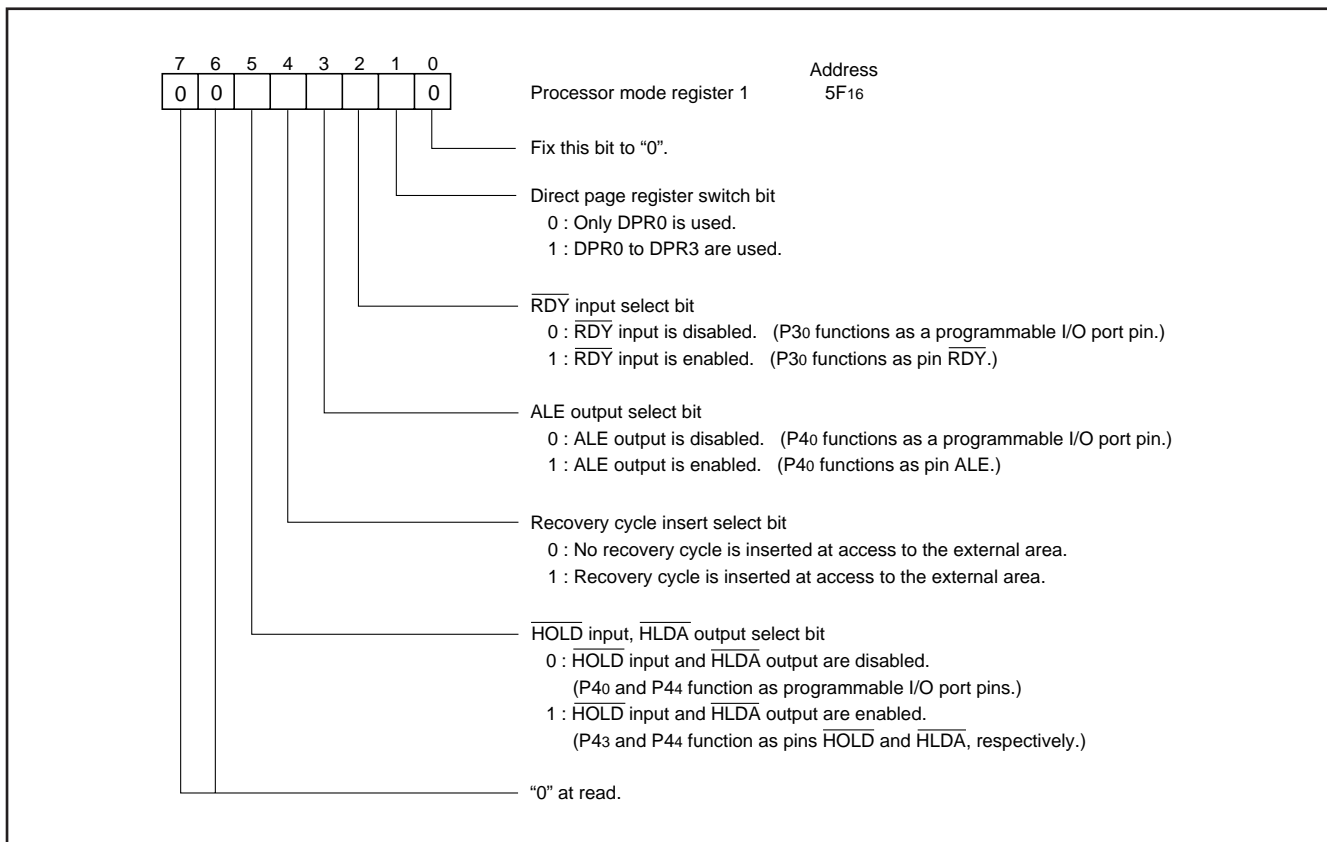


Fig. 5 Processor mode register 1's bit configuration

	Address		Address																					
Port P0 direction register	(04 <sub>16</sub> )...	00 <sub>16</sub>	Processor mode register 0	(5E <sub>16</sub> )... <table border="1"><tr><td>Note 2</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Note 2</td><td>0</td></tr></table>	Note 2	0	0	0	1	0	Note 2	0												
Note 2	0	0	0	1	0	Note 2	0																	
Port P1 direction register	(05 <sub>16</sub> )...	00 <sub>16</sub>	Processor mode register 1	(5F <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>(Note 2)</td><td>0</td><td>0</td></tr></table>	0	0	(Note 2)	0	0															
0	0	(Note 2)	0	0																				
Port P2 direction register	(08 <sub>16</sub> )...	00 <sub>16</sub>	Watchdog timer	(60 <sub>16</sub> )... FFF <sub>16</sub>																				
Port P3 direction register	(09 <sub>16</sub> )...	<table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	0	0	0	0	Watchdog timer frequency select register	(61 <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	⊗	0				
⊗	⊗	⊗	⊗	0	0	0	0																	
⊗	⊗	⊗	⊗	⊗	⊗	⊗	0																	
Port P4 direction register	(0C <sub>16</sub> )...	<table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	0	0	0	0	Particular function select register 0	(62 <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	⊗	0	0			
⊗	⊗	⊗	⊗	0	0	0	0																	
⊗	⊗	⊗	⊗	⊗	⊗	⊗	0	0																
Port P5 direction register	(0D <sub>16</sub> )...	00 <sub>16</sub>	Particular function select register 1	(63 <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>(Note 3)</td></tr></table>	⊗	⊗	⊗	⊗	⊗	0	0	(Note 3)												
⊗	⊗	⊗	⊗	⊗	0	0	(Note 3)																	
Port P6 direction register	(10 <sub>16</sub> )...	<table border="1"><tr><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	0	0	0	0	0	0	0	Debug control register 0	(66 <sub>16</sub> )... <table border="1"><tr><td>1</td><td>(Note 3)</td></tr></table>	1	(Note 3)										
⊗	0	0	0	0	0	0	0																	
1	(Note 3)																							
Port P7 direction register	(11 <sub>16</sub> )...	<table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	0	0	0	0	Debug control register 1	(67 <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>Note 3</td><td>0</td><td>0</td><td>0</td><td>Note 3</td></tr></table>	0	0	0	Note 3	0	0	0	Note 3			
⊗	⊗	⊗	⊗	⊗	0	0	0	0																
0	0	0	Note 3	0	0	0	Note 3																	
Port P8 direction register	(14 <sub>16</sub> )...	<table border="1"><tr><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	0	0	0	0	0	0	0	$\overline{\text{INT}}_3$ interrupt control register	(6E <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0		
⊗	0	0	0	0	0	0	0																	
⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0															
Port P9 direction register	(15 <sub>16</sub> )...	<table border="1"><tr><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	0	0	0	0	0	0	0	$\overline{\text{INT}}_4$ interrupt control register	(6F <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0	
⊗	0	0	0	0	0	0	0																	
⊗	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0														
Port P10 direction register	(18 <sub>16</sub> )...	00 <sub>16</sub>	A-D conversion interrupt control register	(70 <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>?</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	?	0	0	0											
⊗	⊗	⊗	⊗	⊗	?	0	0	0																
Port P11 direction register	(19 <sub>16</sub> )...	00 <sub>16</sub>	UART 0 transmit interrupt control register	(71 <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0										
⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0															
Port P12 direction register	(1C <sub>16</sub> )...	<table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	UART 0 receive interrupt control register	(72 <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0
⊗	⊗	⊗	⊗	⊗	⊗	0	0	0																
⊗	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0														
A-D control register 0	(1E <sub>16</sub> )...	<table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>?</td><td>?</td><td>?</td></tr></table>	0	0	0	0	0	?	?	?	UART 1 transmit interrupt control register	(73 <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0		
0	0	0	0	0	?	?	?																	
⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0															
A-D control register 1	(1F <sub>16</sub> )...	<table border="1"><tr><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr></table>	⊗	0	0	0	0	0	0	0	1	UART 1 receive interrupt control register	(74 <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0	
⊗	0	0	0	0	0	0	0	1																
⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0															
UART 0 Transmit/Receive mode register	(30 <sub>16</sub> )...	00 <sub>16</sub>	Timer A0 interrupt control register	(75 <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0										
⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0															
UART 1 Transmit/Receive mode register	(38 <sub>16</sub> )...	00 <sub>16</sub>	Timer A1 interrupt control register	(76 <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0										
⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0															
UART 0 Transmit/Receive control register 0	(34 <sub>16</sub> )...	<table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	1	0	0	0	Timer A2 interrupt control register	(77 <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0		
0	0	0	0	1	0	0	0																	
⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0															
UART 1 Transmit/Receive control register 0	(3C <sub>16</sub> )...	<table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	1	0	0	0	Timer A3 interrupt control register	(78 <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0		
0	0	0	0	1	0	0	0																	
⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0															
UART 0 Transmit/Receive control register 1	(35 <sub>16</sub> )...	<table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr></table>	0	0	0	0	0	0	1	0	Timer A4 interrupt control register	(79 <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0		
0	0	0	0	0	0	1	0																	
⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0															
UART 1 Transmit/Receive control register 1	(3D <sub>16</sub> )...	<table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr></table>	0	0	0	0	0	0	1	0	Timer B0 interrupt control register	(7A <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0		
0	0	0	0	0	0	1	0																	
⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0															
Count start register	(40 <sub>16</sub> )...	00 <sub>16</sub>	Timer B1 interrupt control register	(7B <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0										
⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0															
One-shot start register	(42 <sub>16</sub> )...	<table border="1"><tr><td>0</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	⊗	⊗	0	0	0	0	0	Timer B2 interrupt control register	(7C <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0		
0	⊗	⊗	0	0	0	0	0																	
⊗	⊗	⊗	⊗	⊗	⊗	0	0	0	0															
Up-down register	(44 <sub>16</sub> )...	<table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	$\overline{\text{INT}}_0$ interrupt control register	(7D <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	0	0	0	0	0	0	0			
0	0	0	0	0	0	0	0																	
⊗	⊗	0	0	0	0	0	0	0																
Timer A clock division select register	(45 <sub>16</sub> )...	<table border="1"><tr><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>⊗</td><td>0</td><td>0</td></tr></table>	⊗	⊗	⊗	⊗	⊗	⊗	0	0	$\overline{\text{INT}}_1$ interrupt control register	(7E <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	0	0	0	0	0	0	0			
⊗	⊗	⊗	⊗	⊗	⊗	0	0																	
⊗	⊗	0	0	0	0	0	0	0																
Timer A0 mode register	(56 <sub>16</sub> )...	00 <sub>16</sub>	$\overline{\text{INT}}_2$ interrupt control register	(7F <sub>16</sub> )... <table border="1"><tr><td>⊗</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	⊗	⊗	0	0	0	0	0	0	0											
⊗	⊗	0	0	0	0	0	0	0																
Timer A1 mode register	(57 <sub>16</sub> )...	00 <sub>16</sub>	Processor status register PS	<table border="1"><tr><td>0</td><td>0</td><td>0</td><td>?</td><td>?</td><td>0</td><td>0</td><td>0</td><td>1</td><td>?</td><td>?</td></tr></table>	0	0	0	?	?	0	0	0	1	?	?									
0	0	0	?	?	0	0	0	1	?	?														
Timer A2 mode register	(58 <sub>16</sub> )...	00 <sub>16</sub>	Program bank register PG	00 <sub>16</sub>																				
Timer A3 mode register	(59 <sub>16</sub> )...	00 <sub>16</sub>	Program counter PC <sub>H</sub>	Contents at address FFFF <sub>16</sub>																				
Timer A4 mode register	(5A <sub>16</sub> )...	00 <sub>16</sub>	Program counter PC <sub>L</sub>	Contents at address FFFE <sub>16</sub>																				
Timer B0 mode register	(5B <sub>16</sub> )...	<table border="1"><tr><td>0</td><td>0</td><td>?</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	?	⊗	0	0	0	0	Direct page registers DPR0 to DPR3	0000 <sub>16</sub>												
0	0	?	⊗	0	0	0	0																	
Timer B1 mode register	(5C <sub>16</sub> )...	<table border="1"><tr><td>0</td><td>0</td><td>?</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	?	⊗	0	0	0	0	Data bank register DT	00 <sub>16</sub>												
0	0	?	⊗	0	0	0	0																	
Timer B2 mode register	(5D <sub>16</sub> )...	<table border="1"><tr><td>0</td><td>0</td><td>?</td><td>⊗</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	?	⊗	0	0	0	0	Stack pointer	FFF <sub>16</sub>												
0	0	?	⊗	0	0	0	0																	

**Notes 1:** The contents of the other registers and RAM are undefined at reset and must be initialized by software.  
**2:** The status just after reset depends on the voltage level applied to pin MD0.  
**3:** At power-on reset, these bits are clear to "0". At hardware or software reset, on the other hand, these bits retain the state just before reset.

Fig. 6 Microcomputer internal status just after reset (1)

**PRELIMINARY**  
Notice: This is not a final specification.  
Some parametric limits are subject to change.

$\overline{CS}_0$ control register L	Address (80 <sub>16</sub> )... <table border="1"><tr><td>Note 2</td><td>1</td><td>0</td><td>X</td><td>0</td><td>Note 3</td><td>1</td><td>0</td></tr></table>	Note 2	1	0	X	0	Note 3	1	0	DMA0 interrupt control register	Address (B2 <sub>16</sub> )... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0
Note 2	1	0	X	0	Note 3	1	0												
X	X	X	X	0	0	0	0												
$\overline{CS}_0$ control register H	(81 <sub>16</sub> )... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>1</td></tr></table>	X	X	X	X	X	0	0	1	DMA1 interrupt control register	(B3 <sub>16</sub> )... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0
X	X	X	X	X	0	0	1												
X	X	X	X	0	0	0	0												
$\overline{CS}_1$ control register L	(82 <sub>16</sub> )... <table border="1"><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Note 3</td><td>1</td><td>0</td></tr></table>	0	1	0	0	0	Note 3	1	0	DMA2 interrupt control register	(B4 <sub>16</sub> )... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0
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$\overline{CS}_1$ control register H	(83 <sub>16</sub> )... <table border="1"><tr><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td></tr></table>	0	X	X	X	X	0	0	0	DMA3 interrupt control register	(B5 <sub>16</sub> )... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	0	0	0	0
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$\overline{CS}_2$ control register L	(84 <sub>16</sub> )... <table border="1"><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Note 3</td><td>1</td><td>0</td></tr></table>	0	1	0	0	0	Note 3	1	0	DMA0 mode register L	(CC <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
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$\overline{CS}_2$ control register H	(85 <sub>16</sub> )... <table border="1"><tr><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td></tr></table>	0	X	X	X	X	0	0	0	DMA0 mode register H	(CD <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
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$\overline{CS}_3$ control register L	(86 <sub>16</sub> )... <table border="1"><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Note 3</td><td>1</td><td>0</td></tr></table>	0	1	0	0	0	Note 3	1	0	DMA0 control register	(CE <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
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$\overline{CS}_3$ control register H	(87 <sub>16</sub> )... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td></tr></table>	X	X	X	X	X	0	0	0	DMA1 mode register L	(DC <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
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Area $\overline{CS}_0$ start address register	(8A <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	1	0	0	0	0	DMA1 mode register H	(DD <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
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Area $\overline{CS}_1$ start address register	(8C <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	DMA1 control register	(DE <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
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Area $\overline{CS}_2$ start address register	(8E <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	DMA2 mode register L	(EC <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
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Area $\overline{CS}_3$ start address register	(90 <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	DMA2 mode register H	(ED <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
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Real-time output control register	(A0 <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	DMA2 control register	(EE <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
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DRAM control register	(A8 <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	DMA3 mode register L	(FC <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
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$\overline{CTS}/\overline{RTS}$ separate select register	(AC <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	DMA3 mode register H	(FD <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
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DMAC control register L	(B0 <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0	DMA3 control register	(FE <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0
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DMAC control register H	(B1 <sub>16</sub> )... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	0	0	0	0	0	0	0	0										
0	0	0	0	0	0	0	0												

**Notes 1:** The contents of the other registers and RAM are undefined at reset and must be initialized by software.  
**2:** The status just after reset depends on the voltage level applied to pin MD0.  
**3:** While V<sub>SS</sub> level voltage is applied to pin BYTE, these bits are "0". While V<sub>CC</sub> level voltage is applied to pin BYTE, on the other hand, these bits are "1".

Fig. 7 Microcomputer internal registers' status just after reset (2)

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

## INPUT/OUTPUT PINS

Each of ports P3 to P9 and P12 has an direction register, and each bit can be programmed for input or output. A pin becomes an output pin when the corresponding bit of direction register is "1", and an input pin when it is "0".

When a pin is programmed as an output pin, the data written to its port latch is output to the output pin. When a pin is programmed as an output pin, the contents of the port latch are read out instead of the value of the pin. Accordingly, a previously output value can be read out correctly even when the output "H" voltage is lowered or the output "L" voltage is raised, owing to an external load, etc.

A pin programmed as an input pin is placed in the floating state, and the value input to the pin can be read out correctly. When a pin is programmed as an input pin, the data can be written only in the port latch, and the pin remains floating.

Each of Figures 8 and 9 shows the block diagram for each port pin.

Table 2. Correspondence between external buses, bus control signals, and programmable I/O port pins

External buses, Bus control signals	Standby state select bit	
	0	1
A0 to A7, A8 to A15, A16 to A23	A0 to A7, A8 to A15, A16 to A23	P100 to P107 (Note 2), P110 to P117 (Note 2), P00 to P07 (Note 2)
D0 to D7, D8 to D15	D0 to D7, D8 to D15 (Note 1)	P10 to P17 (Note 2), P20 to P27
$\overline{RD}$ , $\overline{BLW}$ , $\overline{BHW}$	$\overline{RD}$ , $\overline{BLW}$ , $\overline{BHW}$ (Note 1)	P31, P32 (Note 2), P33
$\overline{CS0}$	$\overline{CS0}$	P90 (Note 2)

**Notes 1:** When the external data bus width = 8 bits (BYTE = VCC level), this becomes a programmable I/O port pin, regardless of the standby state select bit's contents.

**2:** Pin functions of port pins P0, P1, P31, P32, P90, P10, P11 are not shown in the pin configuration. However, relationship with corresponding bus signals and ports is listed in Table 2. For the addresses of these port's registers and direction registers, refer to the location of the peripheral devices' control registers (Figures 2 and 3).

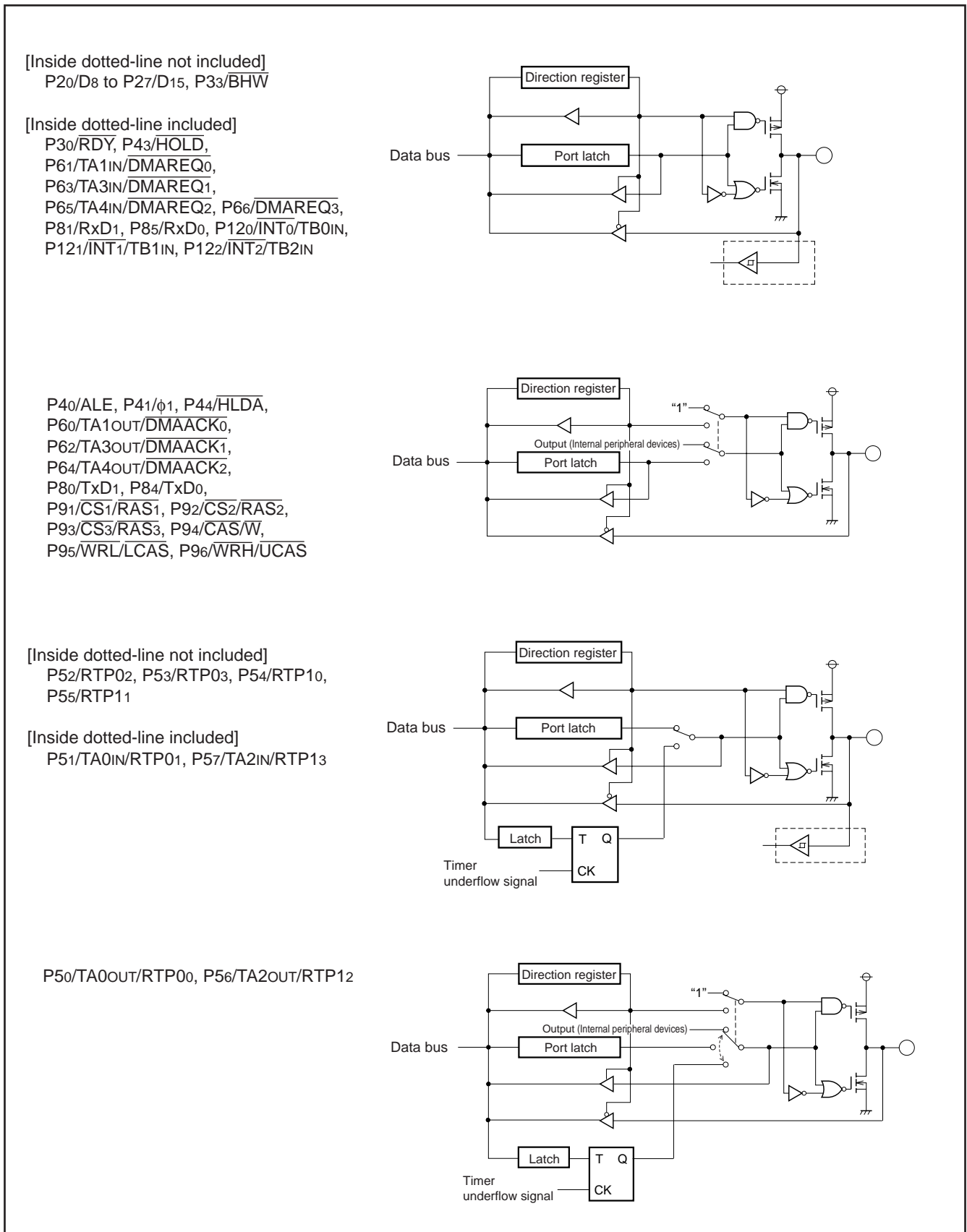


Fig. 8 Block diagram for each port pin (1)



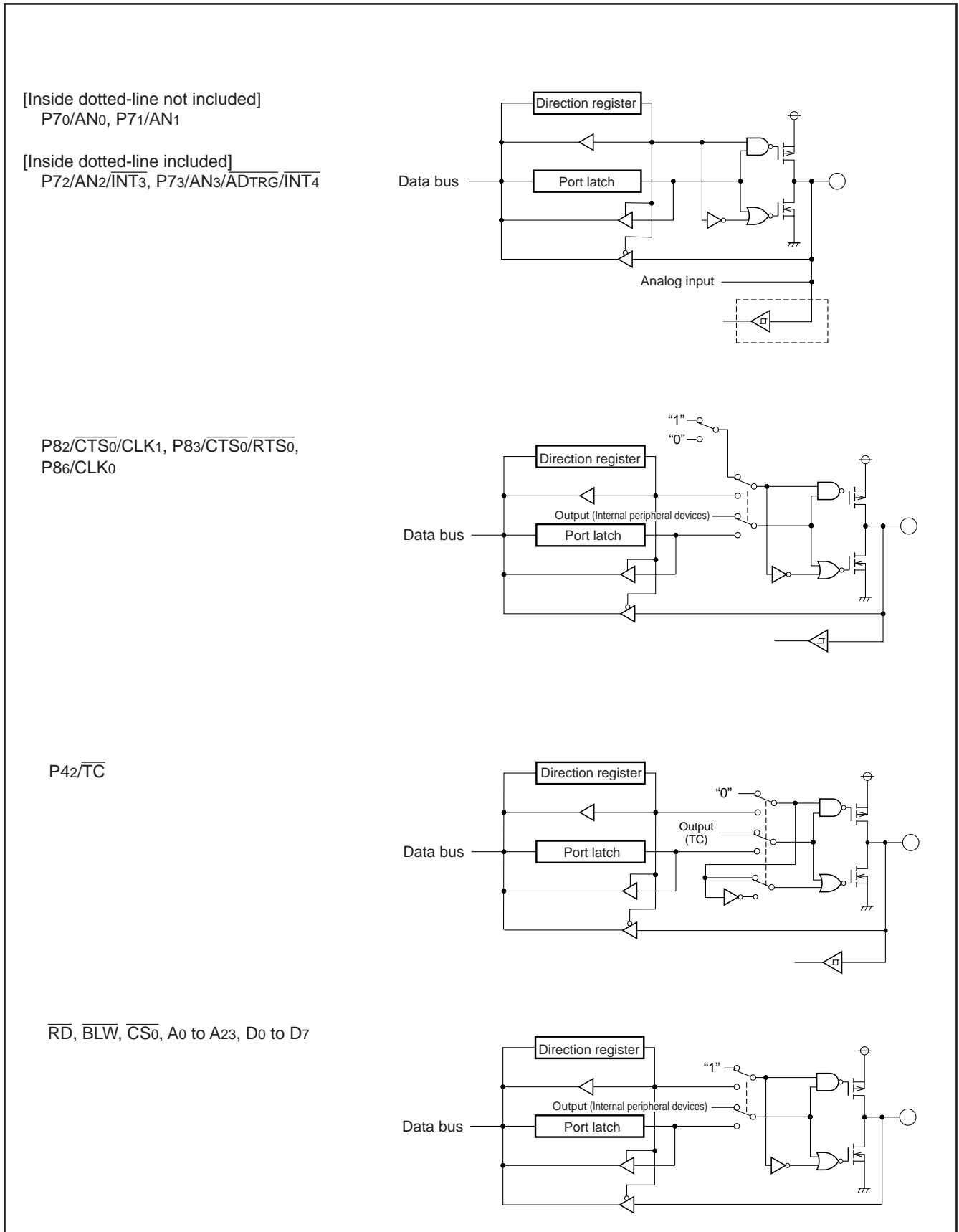


Fig. 9 Block diagram for each port pin (2)

**PRELIMINARY**  
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**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Ratings	Unit
VCC	Power source voltage	-0.3 to 6.5	V
AVCC	Analog power source voltage	-0.3 to 6.5	V
Vi	Input voltage D <sub>0</sub> -D <sub>7</sub> , D <sub>8</sub> /P <sub>20</sub> -D <sub>15</sub> /P <sub>27</sub> , P <sub>30</sub> , P <sub>33</sub> , P <sub>40</sub> -P <sub>44</sub> , P <sub>50</sub> -P <sub>57</sub> , P <sub>60</sub> -P <sub>66</sub> , P <sub>70</sub> -P <sub>73</sub> , P <sub>80</sub> -P <sub>86</sub> , P <sub>91</sub> -P <sub>96</sub> , P <sub>120</sub> -P <sub>122</sub> , VREF, XIN, RESET, BYTE, MD0, MD1, NMI	-0.3 to Vcc+0.3	V
Vo	Output voltage A <sub>0</sub> -A <sub>23</sub> , RD, BLW, BHW/P33, CS <sub>0</sub> , D <sub>0</sub> -D <sub>7</sub> , D <sub>8</sub> /P <sub>20</sub> -D <sub>15</sub> /P <sub>27</sub> , P <sub>30</sub> , P <sub>40</sub> -P <sub>44</sub> , P <sub>50</sub> -P <sub>57</sub> , P <sub>60</sub> -P <sub>66</sub> , P <sub>70</sub> -P <sub>73</sub> , P <sub>80</sub> -P <sub>86</sub> , P <sub>91</sub> -P <sub>96</sub> , P <sub>120</sub> -P <sub>122</sub> , XOUT	-0.3 to Vcc+0.3	V
Pd	Power dissipation	300	mW
Topr	Operating temperature	-20 to 85	°C
Tstg	Storage temperature	-40 to 150	°C

**RECOMMENDED OPERATING CONDITIONS** (Vcc = 5 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
VCC	Power source voltage	4.5	5	5.5	V
AVCC	Analog power source voltage		Vcc		V
VSS	Power source voltage		0		V
AVSS	Analog power source voltage		0		V
VIH	High-level input voltage P <sub>20</sub> -P <sub>27</sub> , P <sub>30</sub> , P <sub>33</sub> , P <sub>40</sub> -P <sub>44</sub> , P <sub>50</sub> -P <sub>57</sub> , P <sub>60</sub> -P <sub>66</sub> , P <sub>70</sub> -P <sub>73</sub> , P <sub>80</sub> -P <sub>86</sub> , P <sub>91</sub> -P <sub>96</sub> , P <sub>120</sub> -P <sub>122</sub> , XIN, RESET, BYTE, MD0, MD1, NMI	0.8VCC		VCC	V
VIH	High-level input voltage D <sub>0</sub> -D <sub>7</sub> , D <sub>8</sub> -D <sub>15</sub>	0.5VCC		VCC	V
VIL	Low-level input voltage P <sub>20</sub> -P <sub>27</sub> , P <sub>30</sub> , P <sub>33</sub> , P <sub>40</sub> -P <sub>44</sub> , P <sub>50</sub> -P <sub>57</sub> , P <sub>60</sub> -P <sub>66</sub> , P <sub>70</sub> -P <sub>73</sub> , P <sub>80</sub> -P <sub>86</sub> , P <sub>91</sub> -P <sub>96</sub> , P <sub>120</sub> -P <sub>122</sub> , XIN, RESET, BYTE, MD0, MD1, NMI	0		0.2VCC	V
VIL	Low-level input voltage D <sub>0</sub> -D <sub>7</sub> , D <sub>8</sub> -D <sub>15</sub>	0		0.16VCC	V
IOH (peak)	High-level peak output current A <sub>0</sub> -A <sub>23</sub> , RD, BLW, BHW/P33, CS <sub>0</sub> , D <sub>0</sub> -D <sub>7</sub> , D <sub>8</sub> /P <sub>20</sub> -D <sub>15</sub> /P <sub>27</sub> , P <sub>30</sub> , P <sub>40</sub> -P <sub>44</sub> , P <sub>50</sub> -P <sub>57</sub> , P <sub>60</sub> -P <sub>66</sub> , P <sub>70</sub> -P <sub>73</sub> , P <sub>80</sub> -P <sub>86</sub> , P <sub>91</sub> -P <sub>96</sub> , P <sub>120</sub> -P <sub>122</sub>			-10	mA
IOH (avg)	High-level average output current A <sub>0</sub> -A <sub>23</sub> , RD, BLW, BHW/P33, CS <sub>0</sub> , D <sub>0</sub> -D <sub>7</sub> , D <sub>8</sub> /P <sub>20</sub> -D <sub>15</sub> /P <sub>27</sub> , P <sub>30</sub> , P <sub>40</sub> -P <sub>44</sub> , P <sub>50</sub> -P <sub>57</sub> , P <sub>60</sub> -P <sub>66</sub> , P <sub>70</sub> -P <sub>73</sub> , P <sub>80</sub> -P <sub>86</sub> , P <sub>91</sub> -P <sub>96</sub> , P <sub>120</sub> -P <sub>122</sub>			-5	mA
IOL (peak)	Low-level peak output current A <sub>0</sub> -A <sub>23</sub> , RD, BLW, BHW/P33, CS <sub>0</sub> , D <sub>0</sub> -D <sub>7</sub> , D <sub>8</sub> /P <sub>20</sub> -D <sub>15</sub> /P <sub>27</sub> , P <sub>30</sub> , P <sub>40</sub> -P <sub>44</sub> , P <sub>50</sub> -P <sub>57</sub> , P <sub>60</sub> -P <sub>66</sub> , P <sub>70</sub> -P <sub>73</sub> , P <sub>80</sub> -P <sub>86</sub> , P <sub>91</sub> -P <sub>96</sub> , P <sub>120</sub> -P <sub>122</sub>			10	mA
IOL (avg)	Low-level average output current A <sub>0</sub> -A <sub>23</sub> , RD, BLW, BHW/P33, CS <sub>0</sub> , D <sub>0</sub> -D <sub>7</sub> , D <sub>8</sub> /P <sub>20</sub> -D <sub>15</sub> /P <sub>27</sub> , P <sub>30</sub> , P <sub>40</sub> -P <sub>44</sub> , P <sub>50</sub> -P <sub>57</sub> , P <sub>60</sub> -P <sub>66</sub> , P <sub>70</sub> -P <sub>73</sub> , P <sub>80</sub> -P <sub>86</sub> , P <sub>91</sub> -P <sub>96</sub> , P <sub>120</sub> -P <sub>122</sub>			5	mA
f(XIN)	External clock input frequency			20	MHz

**Notes 1:** Average output current is the average value of an interval of 100 ms.

**2:** The sum of IOL(peak) for A<sub>0</sub>-A<sub>23</sub>, D<sub>0</sub>-D<sub>7</sub>, D<sub>8</sub>/P<sub>20</sub>-D<sub>15</sub>/P<sub>27</sub>, ports P<sub>80</sub>-P<sub>86</sub> must be 80 mA or less, the sum of IOH(peak) for A<sub>0</sub>-A<sub>23</sub>, D<sub>0</sub>-D<sub>7</sub>, D<sub>8</sub>/P<sub>20</sub>-D<sub>15</sub>/P<sub>27</sub>, ports P<sub>80</sub>-P<sub>86</sub> must be 80 mA or less, the sum of IOL(peak) for ports P<sub>30</sub>, RD, BLW, BHW/P33, CS<sub>0</sub>, P<sub>40</sub>-P<sub>44</sub>, P<sub>50</sub>-P<sub>57</sub>, P<sub>60</sub>-P<sub>66</sub>, P<sub>70</sub>-P<sub>73</sub>, P<sub>91</sub>-P<sub>96</sub>, P<sub>120</sub>-P<sub>122</sub> must be 80 mA or less, the sum of IOH(peak) for P<sub>30</sub>, RD, BLW, BHW/P33, CS<sub>0</sub>, P<sub>40</sub>-P<sub>44</sub>, P<sub>50</sub>-P<sub>57</sub>, P<sub>60</sub>-P<sub>66</sub>, P<sub>70</sub>-P<sub>73</sub>, P<sub>91</sub>-P<sub>96</sub>, P<sub>120</sub>-P<sub>122</sub> must be 80 mA or less.

**PRELIMINARY**  
Notice: This is not a final specification.  
Some parametric limits are subject to change.

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }85\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 20\text{ MHz}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	High-level output voltage A0–A23, $\overline{CS}_0$ , D0–D7, D8/P20–D15/P27, P30, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P93, P120–P122	I <sub>OH</sub> = –10 mA	3			V
VOH	High-level output voltage A0–A23, $\overline{CS}_0$ , D0–D7, D8/P20–D15/P27, P40, P44, P91–P93	I <sub>OH</sub> = –400 $\mu\text{A}$	4.7			V
VOH	High-level output voltage $\overline{RD}$ , $\overline{BLW}$ , $\overline{BHW}/P33$ , P94/CAS $\overline{W}$ , P95/WRL/LCAS, P96/WRH/UCAS	I <sub>OH</sub> = –10 mA	3.4			V
		I <sub>OH</sub> = –400 $\mu\text{A}$	4.8			
VOL	Low-level output voltage A0–A23, $\overline{CS}_0$ , D0–D7, D8/P20–D15/P27, P30, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P93, P120–P122	I <sub>OL</sub> = 10 mA			2	V
VOL	Low-level output voltage A0–A23, $\overline{CS}_0$ , D0–D7, D8/P20–D15/P27, P40, P44, P91–P93	I <sub>OL</sub> = 2 mA			0.45	V
VOL	Low-level output voltage $\overline{RD}$ , $\overline{BLW}$ , $\overline{BHW}/P33$ , P94/CAS $\overline{W}$ , P95/WRL/LCAS, P96/WRH/UCAS	I <sub>OL</sub> = 10 mA			1.6	V
		I <sub>OL</sub> = 2 mA			0.4	
VT+ –VT–	Hysteresis TA0IN–TA4IN, TB0IN–TB2IN, $\overline{INT}_0$ – $\overline{INT}_4$ , $\overline{DMAREQ}_0$ – $\overline{DMAREQ}_3$ , $\overline{ADTRG}$ , $\overline{CTS}_0$ , CLK0, CLK1, NMI, RDY, HOLD, RxD0, RxD1		0.4		1	V
VT+ –VT–	Hysteresis $\overline{RESET}$		0.5		1.5	V
VT+ –VT–	Hysteresis XIN		0.1		0.3	V
I <sub>IH</sub>	High-level input current D0–D7, D8/P20–D15/P27, P30, P33, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P120–P122, XIN, $\overline{RESET}$ , BYTE, MD0, MD1, NMI	V <sub>I</sub> = 5.0 V			5	$\mu\text{A}$
I <sub>IL</sub>	Low-level input current D0–D7, D8/P20–D15/P27, P30, P33, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P120–P122, XIN, $\overline{RESET}$ , BYTE, MD0, MD1, NMI	V <sub>I</sub> = 0 V			–5	$\mu\text{A}$
VRAM	RAM hold voltage	When clock is stopped.	2			V
ICC	Power source current	At reset in micro-processor mode, output-only pins are open, and the other pins are connected to V <sub>SS</sub> .	f(X <sub>IN</sub> ) = 20 MHz.	25	50	mA
			T <sub>a</sub> = 25 °C when clock is stopped.		1	
			T <sub>a</sub> = 80 °C when clock is stopped.		20	

**PRELIMINARY**  
Notice: This is not a final specification.  
Some parametric limits are subject to change.

### A-D CONVERTER CHARACTERISTICS

(VCC = AVCC = 5 V ± 10 %, VSS = AVSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
—————	Resolution	VREF = VCC		10	Bits
—————	Absolute accuracy	VREF = VCC	10-bit resolution mode	± 3	LSB
			8-bit resolution mode	± 2	LSB
RLADDER	Ladder resistance	VREF = VCC	5		kΩ
tCONV	Conversion time	f(XIN) ≤ 20 MHz	10-bit resolution mode	5.9	μs
			8-bit resolution mode	2.45 (Note)	
VREF	Reference voltage	—————	2.7	VCC	V
VIA	Analog input voltage	—————	0	VREF	V

**Note:** This is applied when A-D conversion frequency ( $f_{AD}$ ) =  $f_{1(\phi)}$ .

**PRELIMINARY**  
Notice: This is not a final specification.  
Some parametric limits are subject to change.

## PERIPHERAL DEVICE INPUT/OUTPUT TIMING

(VCC = 5 V ± 10 %, VSS = 0 V, Ta = -20 to 85 °C, f(XIN) = 20 MHz unless otherwise noted)

\* For limits depending on f(XIN), their calculation formulas are shown below. Also, the values at f(XIN) = 20 MHz are shown in ( ).

### Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	80		ns
tw(TAH)	TAiIN input high-level pulse width	40		ns
tw(TAL)	TAiIN input low-level pulse width	40		ns

### Timer A input (Gating input in timer mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
tc(TA)	TAiIN input cycle time	f(XIN) ≤ 20 MHz	$\frac{16 \times 10^9}{f(XIN)}$ (800)		ns
tw(TAH)	TAiIN input high-level pulse width	f(XIN) ≤ 20 MHz	$\frac{8 \times 10^9}{f(XIN)}$ (400)		ns
tw(TAL)	TAiIN input low-level pulse width	f(XIN) ≤ 20 MHz	$\frac{8 \times 10^9}{f(XIN)}$ (400)		ns

**Note :** The TAiIN input cycle time requires 4 or more cycles of a count source. The TAiIN input high-level pulse width and the TAiIN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f2 at f(XIN) ≤ 20 MHz.

### Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
tc(TA)	TAiIN input cycle time	f(XIN) ≤ 20 MHz	$\frac{8 \times 10^9}{f(XIN)}$ (400)		ns
tw(TAH)	TAiIN input high-level pulse width		80		ns
tw(TAL)	TAiIN input low-level pulse width		80		ns

### Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tw(TAH)	TAiIN input high-level pulse width	80		ns
tw(TAL)	TAiIN input low-level pulse width	80		ns

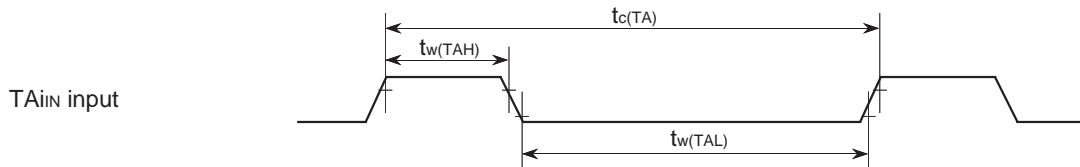
### Timer A input (Up-down input and Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high-level pulse width	1000		ns
tw(UPL)	TAiOUT input low-level pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

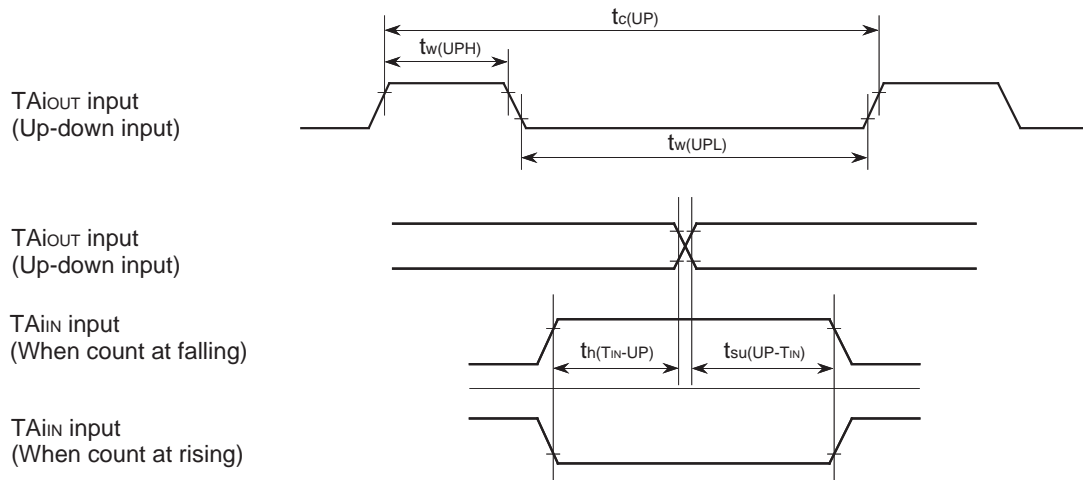
**Timer A input** (Two-phase pulse input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(TA)$	TAiIN input cycle time	800		ns
$t_{su}(TA_{jIN}-TA_{jOUT})$	TAjIN input setup time	200		ns
$t_{su}(TA_{jOUT}-TA_{jIN})$	TAjOUT input setup time	200		ns

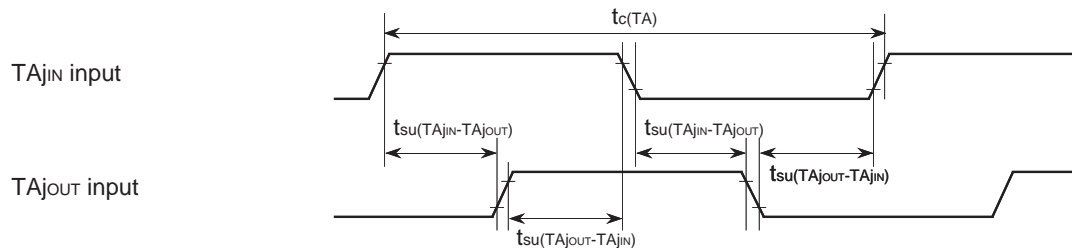
- Gating input in timer mode
- Count input in event counter mode
- External trigger input in one-shot pulse mode
- External trigger input in pulse width modulation mode



- Up-down input and Count input in event counter mode



- Two-phase pulse input in event counter mode



Test conditions

- Vcc = 5 V ± 10 %, Ta = -20 to 85 °C
- Input timing voltage : VIL = 1.0 V, VIH = 4.0 V

**PRELIMINARY**  
Notice: This is not a final specification.  
Some parametric limits are subject to change.

**Timer B input** (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>c</sub> (TB)	TBiIN input cycle time (one edge count)	80		ns
t <sub>w</sub> (TBH)	TBiIN input high-level pulse width (one edge count)	40		ns
t <sub>w</sub> (TBL)	TBiIN input low-level pulse width (one edge count)	40		ns
t <sub>c</sub> (TB)	TBiIN input cycle time (both edge count)	160		ns
t <sub>w</sub> (TBH)	TBiIN input high-level pulse width (both edge count)	80		ns
t <sub>w</sub> (TBL)	TBiIN input low-level pulse width (both edge count)	80		ns

**Timer B input** (Pulse period measurement mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
t <sub>c</sub> (TB)	TBiIN input cycle time	f(XIN) ≤ 20 MHz	$\frac{16 \times 10^9}{f(XIN)}$ (800)		ns
t <sub>w</sub> (TBH)	TBiIN input high-level pulse width	f(XIN) ≤ 20 MHz	$\frac{8 \times 10^9}{f(XIN)}$ (400)		ns
t <sub>w</sub> (TBL)	TBiIN input low-level pulse width	f(XIN) ≤ 20 MHz	$\frac{8 \times 10^9}{f(XIN)}$ (400)		ns

**Note:** The TBiIN input cycle time requires 4 or more cycles of a count source. The TBiIN input high-level pulse width and the TBiIN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f<sub>2</sub> at f(XIN) ≤ 20 MHz.

**Timer B input** (Pulse width measurement mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
t <sub>c</sub> (TB)	TBiIN input cycle time	f(XIN) ≤ 20 MHz	$\frac{16 \times 10^9}{f(XIN)}$ (800)		ns
t <sub>w</sub> (TBH)	TBiIN input high-level pulse width	f(XIN) ≤ 20 MHz	$\frac{8 \times 10^9}{f(XIN)}$ (400)		ns
t <sub>w</sub> (TBL)	TBiIN input low-level pulse width	f(XIN) ≤ 20 MHz	$\frac{8 \times 10^9}{f(XIN)}$ (400)		ns

**Note:** The TBiIN input cycle time requires 4 or more cycles of a count source. The TBiIN input high-level pulse width and the TBiIN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f<sub>2</sub> at f(XIN) ≤ 20 MHz.

**A-D trigger input**

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>c</sub> (AD)	ADTRG input cycle time (minimum allowable trigger)	1000		ns
t <sub>w</sub> (ADL)	ADTRG input low-level pulse width	125		ns

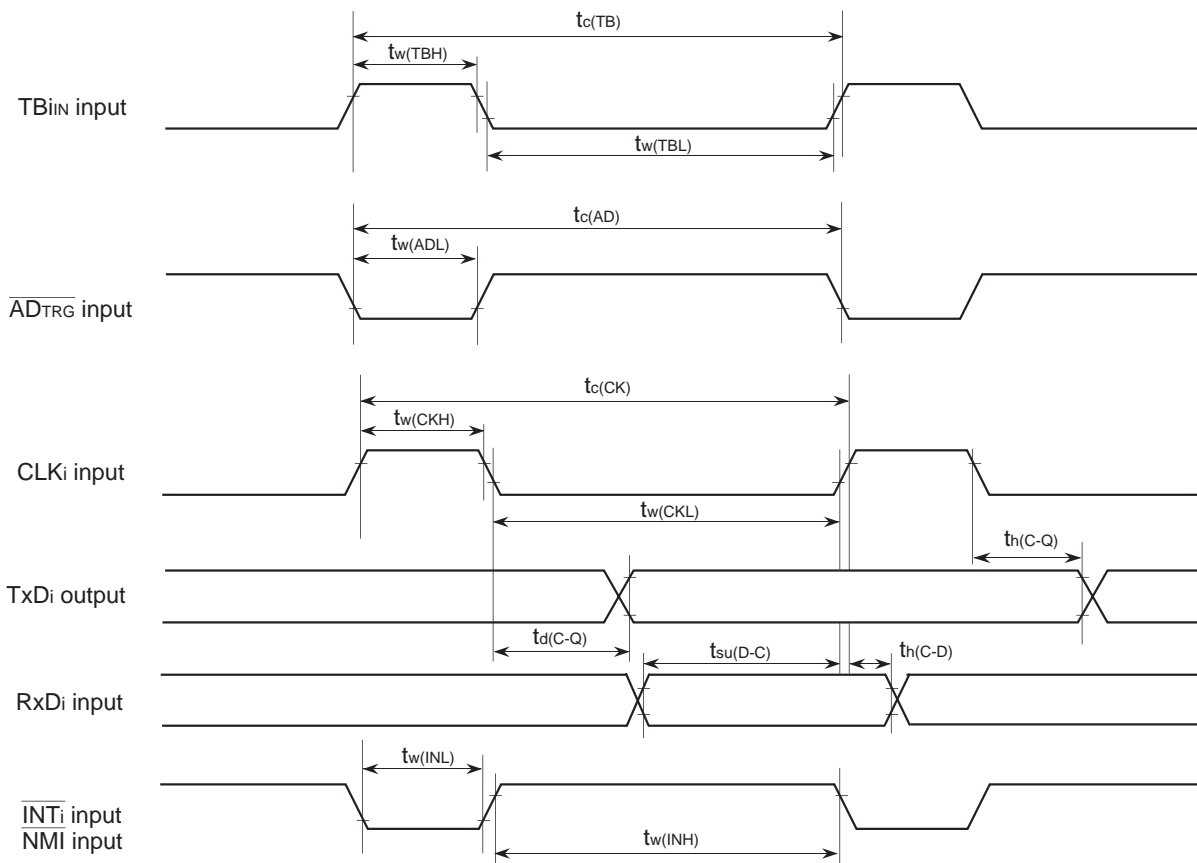
**PRELIMINARY**  
Notice: This is not a final specification.  
Some parametric limits are subject to change.

**Serial I/O**

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(\text{CK})$	CLKi input cycle time	200		ns
$t_w(\text{CKH})$	CLKi input high-level pulse width	100		ns
$t_w(\text{CKL})$	CLKi input low-level pulse width	100		ns
$t_d(\text{C-Q})$	TxDi output delay time		80	ns
$t_h(\text{C-Q})$	TxDi hold time	0		ns
$t_{su}(\text{D-C})$	RxDi input setup time	20		ns
$t_h(\text{C-D})$	RxDi input hold time	90		ns

**External interrupt ( $\overline{\text{INT}}_i$ ) input,  $\overline{\text{NMI}}$  input**

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_w(\text{INH})$	$\overline{\text{INT}}_i$ input/ $\overline{\text{NMI}}$ input high-level pulse width	250		ns
$t_w(\text{INL})$	$\overline{\text{INT}}_i$ input/ $\overline{\text{NMI}}$ input low-level pulse width	250		ns



**Test conditions**

- $V_{CC} = 5 \text{ V} \pm 10 \%$ ,  $T_a = -20 \text{ to } 85 \text{ }^\circ\text{C}$
- Input timing voltage :  $V_{IL} = 1.0 \text{ V}$ ,  $V_{IH} = 4.0 \text{ V}$
- Output timing voltage :  $V_{OL} = 0.8 \text{ V}$ ,  $V_{OH} = 2.0 \text{ V}$ ,  $C_L = 50 \text{ pF}$



**PRELIMINARY**  
Notice: This is not a final specification.  
Some parametric limits are subject to change.

## READY, HOLD TIMING

**Timing requirements** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }85\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 20\text{ MHz}$ , unless otherwise noted)

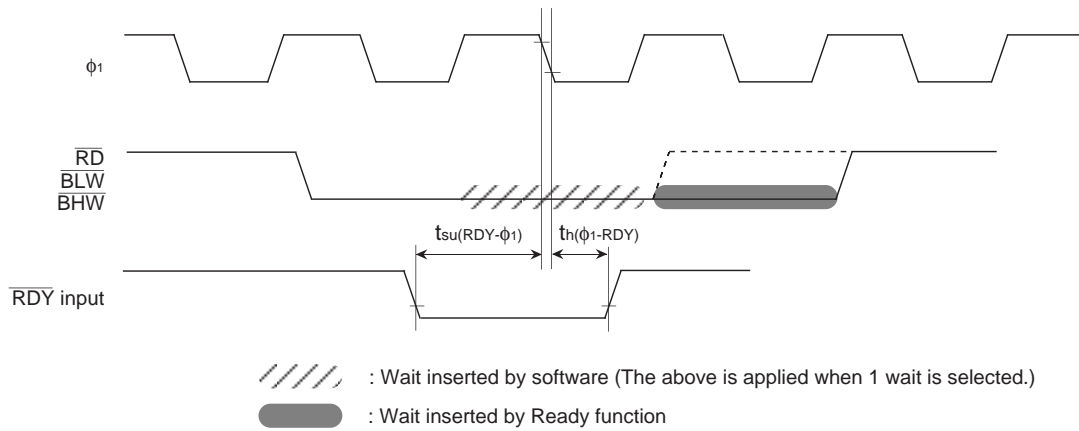
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su}(RDY-\phi 1)$	$\overline{RDY}$ input setup time	40		ns
$t_{su}(HOLD-\phi 1)$	$\overline{HOLD}$ input setup time	40		ns
$t_{h}(\phi 1-RDY)$	$\overline{RDY}$ input hold time	0		ns
$t_{h}(\phi 1-HOLD)$	$\overline{HOLD}$ input hold time	0		ns

**Switching characteristics** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }85\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 20\text{ MHz}$ , unless otherwise noted)

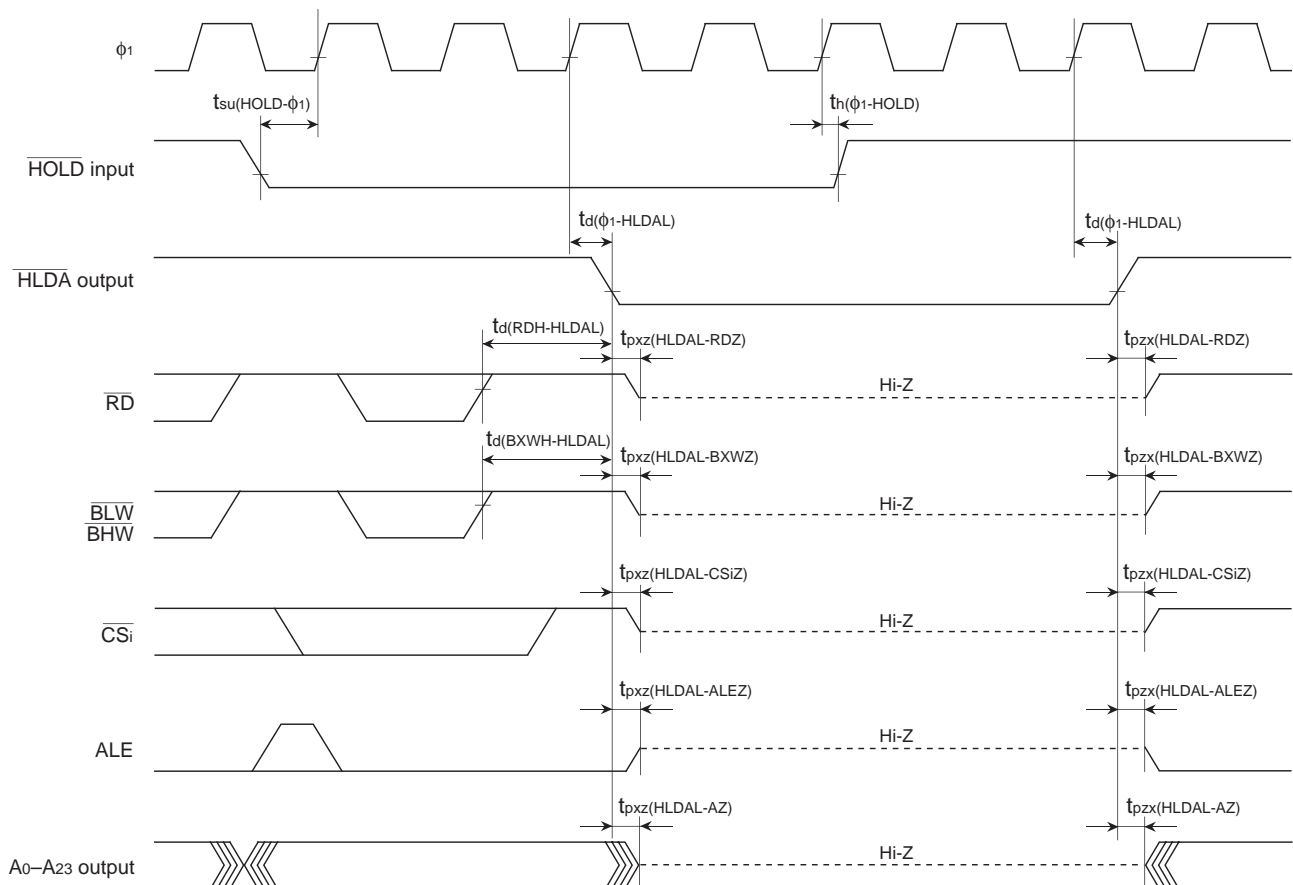
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_d(\phi 1-HLDAL)$	$\overline{HLDA}$ output delay time		20	ns
$t_d(RDH-HLDAL)$	$\overline{HLDA}$ low-level output delay time after read	$t_c - 15$ (Note)		ns
$t_d(BXWH-HLDAL)$	$\overline{HLDA}$ low-level output delay time after write	$t_c - 15$ (Note)		ns
$t_{pxz}(HLDAL-RDZ)$	Floating start delay time	-15	10	ns
$t_{pxz}(HLDAL-BXWZ)$	Floating start delay time	-15	10	ns
$t_{pxz}(HLDAL-CSIZ)$	Floating start delay time	-15	10	ns
$t_{pxz}(HLDAL-ALEZ)$	Floating start delay time	-15	10	ns
$t_{pxz}(HLDAL-AZ)$	Floating start delay time	-15	10	ns
$t_{pzx}(HLDAL-RDZ)$	Floating release delay time	0		ns
$t_{pzx}(HLDAL-BXWZ)$	Floating release delay time	0		ns
$t_{pzx}(HLDAL-CSIZ)$	Floating release delay time	0		ns
$t_{pzx}(HLDAL-ALEZ)$	Floating release delay time	0		ns
$t_{pzx}(HLDAL-AZ)$	Floating release delay time	0		ns

Note:  $t_c = 1/f(X_{IN})$ .

**RDY input**



**HOLD input**



**Test conditions**

- $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = -20$  to  $85\text{ }^\circ\text{C}$
- RDY input, HOLD input :  $V_{IL} = 1.0\text{ V}$ ,  $V_{IH} = 4.0\text{ V}$
- HLDA output :  $V_{OL} = 0.8\text{ V}$ ,  $V_{OH} = 2.0\text{ V}$ ,  $C_L = 50\text{ pF}$

**PRELIMINARY**  
Notice: This is not a final specification.  
Some parametric limits are subject to change.

## External bus timing

For limits depending on  $f(X_{IN})$ , their calculation formulas are shown below.

$W = 0$  (0 wait)

$W = 1$  (1 wait)

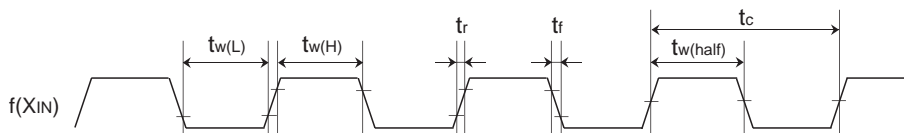
$W = 2$  (2 wait)

$t_c = 1/f(X_{IN})$ .

**Timing Requirements** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20$  to  $85\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 20\text{ MHz}$ , unless otherwise noted)

Symbol	Parameter	Limits				Unit
		When 0/1/2 wait is selected		When ALE expansion wait is selected		
		Min.	Max.	Min.	Max.	
$t_c$	External clock input cycle time	50		50		ns
$t_{w(\text{half})}$	External clock input pulse width with half input-voltage	$0.45t_c$	$0.55t_c$	$0.45t_c$	$0.55t_c$	ns
$t_{w(\text{H})}$	External clock input high-level pulse width	$0.5t_c - 8$		$0.5t_c - 8$		ns
$t_{w(\text{L})}$	External clock input low-level pulse width	$0.5t_c - 8$		$0.5t_c - 8$		ns
$t_r$	External clock input rise time		8		8	ns
$t_f$	External clock input fall time		8		8	ns
$t_{a(\text{A-D})}$	Address access time		$(2 + W)t_c - 45$		$4t_c - 45$	ns
$t_{a(\text{CSIL-D})}$	Chip select access time		$(1.5 + W)t_c - 35$		$3.5t_c - 35$	ns
$t_{a(\text{RDL-D})}$	Read access time		$(1 + W)t_c - 30$		$2t_c - 30$	ns
$t_{su(\text{D-RDL})}$	Read data setup time	15		15		ns
$t_{h(\text{RDH-D})}$	Data input hold time after read	0		0		ns
$t_{a(\text{BA-D})}$	Address access time at burst ROM access		$(1 + W)t_c - 35$		$2t_c - 35$	ns
$t_{h(\text{BA-D})}$	Data hold time after address at burst ROM access	0		0		ns

### External clock input



#### Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = -20$  to  $85\text{ }^\circ\text{C}$
- Input timing voltage :  $V_{IL} = 1.0\text{ V}$ ,  $V_{IH} = 4.0\text{ V}$  ( $t_{w(\text{H})}$ ,  $t_{w(\text{L})}$ ,  $t_r$ ,  $t_f$ )
- Input timing voltage :  $2.5\text{ V}$  ( $t_c$ ,  $t_{w(\text{half})}$ )

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**Switching characteristics** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20$  to  $85\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 20\text{ MHz}$ , unless otherwise noted)

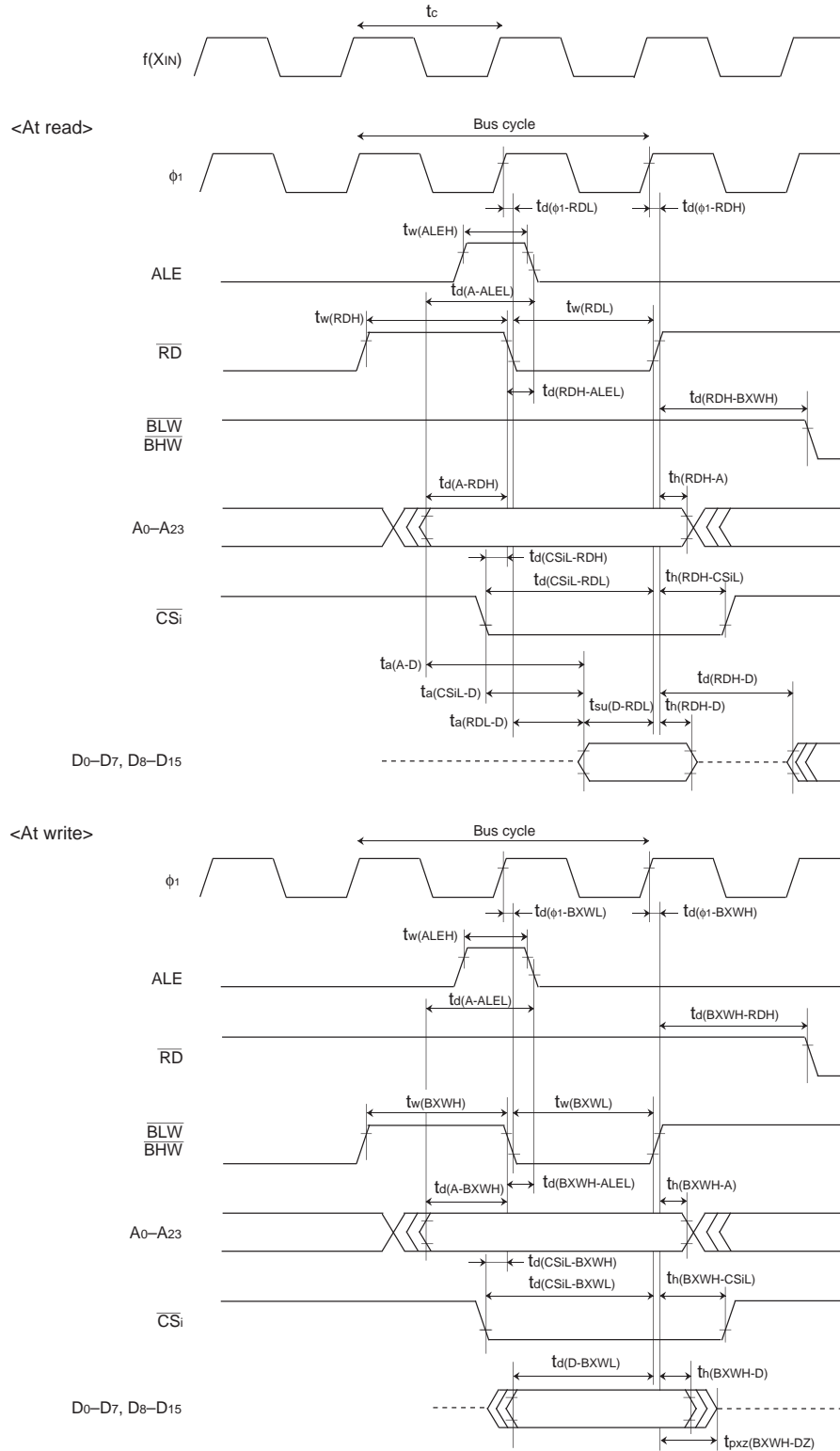
Symbol	Parameter	Limits				Unit
		When 0/1/2 wait is selected		When ALE expansion wait is selected		
		Min.	Max.	Min.	Max.	
$t_{d(\phi 1\text{-RDL})}$	Read low-level output delay time	-10	15	-10	15	ns
$t_{d(\phi 1\text{-RDH})}$	Read high-level output delay time	-10	10	-10	10	ns
$t_{d(\phi 1\text{-BXWL})}$	Write low-level output delay time	-10	15	-10	15	ns
$t_{d(\phi 1\text{-BXWH})}$	Write high-level output delay time	-10	10	-10	10	ns
$t_w(\text{ALEH})$	ALE pulse width	0.5tc - 20		tc - 20		ns
$t_d(\text{A-ALE})$	ALE completion delay time after address stabilization	tc - 30		1.5tc - 30		ns
$t_w(\text{RDL})$	Read output pulse width	$(1 + W)tc - 15$		2tc - 15		ns
$t_w(\text{RDH})$	Read output high-level width <b>(Note 1)</b>	tc - 15		2tc - 15		ns
$t_d(\text{RDH-BXWH})$	Write disable valid time after read <b>(Note 2)</b>	tc - 15		tc - 15		ns
$t_d(\text{A-RDH})$	Address valid time before read	tc - 30		2tc - 30		ns
$t_h(\text{RDH-A})$	Address hold time after read <b>(Note 3)</b>	8		8		ns
$t_d(\text{RDH-ALEL})$	ALE completion delay time after read start			20		ns
$t_d(\text{ALEL-RDH})$	Read disable valid time after ALE completion			0.5tc - 20		ns
$t_d(\text{CSIL-RDH})$	Chip select valid time before read	0.5tc - 20		1.5tc - 20		ns
$t_d(\text{CSIL-RDL})$	Chip select output valid time before read completion	$(1.5 + W)tc - 20$		3.5tc - 20		ns
$t_h(\text{RDH-CSIL})$	Chip select hold time after read	0.5tc - 20		0.5tc - 20		ns
$t_d(\text{RDH-D})$	Next write cycle data output delay time after read <b>(Note 2)</b>	tc - 15		tc - 15		ns
$t_w(\text{BXWL})$	Write output pulse width	$(1 + W)tc - 15$		2tc - 15		ns
$t_w(\text{BXWH})$	Write output high-level width <b>(Note 1)</b>	tc - 15		2tc - 15		ns
$t_d(\text{BXWH-RDH})$	Read disable valid time after write <b>(Note 2)</b>	tc - 15		tc - 15		ns
$t_d(\text{A-BXWH})$	Address valid time before write	tc - 30		2tc-30		ns
$t_h(\text{BXWH-A})$	Address hold time after write <b>(Note 3)</b>	8		8		ns
$t_d(\text{BXWH-ALEL})$	ALE completion delay time after write start			20		ns
$t_d(\text{ALEL-BXWH})$	Write disable valid time after ALE completion			0.5tc - 20		ns
$t_d(\text{CSIL-BXWH})$	Chip select valid time before write	0.5tc - 20		1.5tc - 20		ns
$t_d(\text{CSIL-BXWL})$	Chip select output valid time before write completion	$(1.5 + W)tc - 20$		3.5tc - 20		ns
$t_h(\text{BXWH-CSIL})$	Chip select hold time after write	0.5tc - 20		0.5tc - 20		ns
$t_d(\text{D-BXWL})$	Data output valid time before write completion	$(1 + W)tc - 20$		2tc - 20		ns
$t_h(\text{BXWH-D})$	Data hold time after write	0.5tc - 10		0.5tc - 10		ns
$t_{pxz}(\text{BXWH-DZ})$	Floating start delay time after write			0.5tc + 10		ns

**Notes 1:** When the bus cycle just before this parameter is for the area where the recovery cycle insertion is selected, this parameter is extended by tc (ns).

**2:** When accessing the area where the recovery cycle insertion is selected, this parameter is extended by tc (ns).

**3:** When accessing the area where the recovery cycle insertion is selected, this parameter is extended by tc (ns). However, except for the case at instruction prefetch.

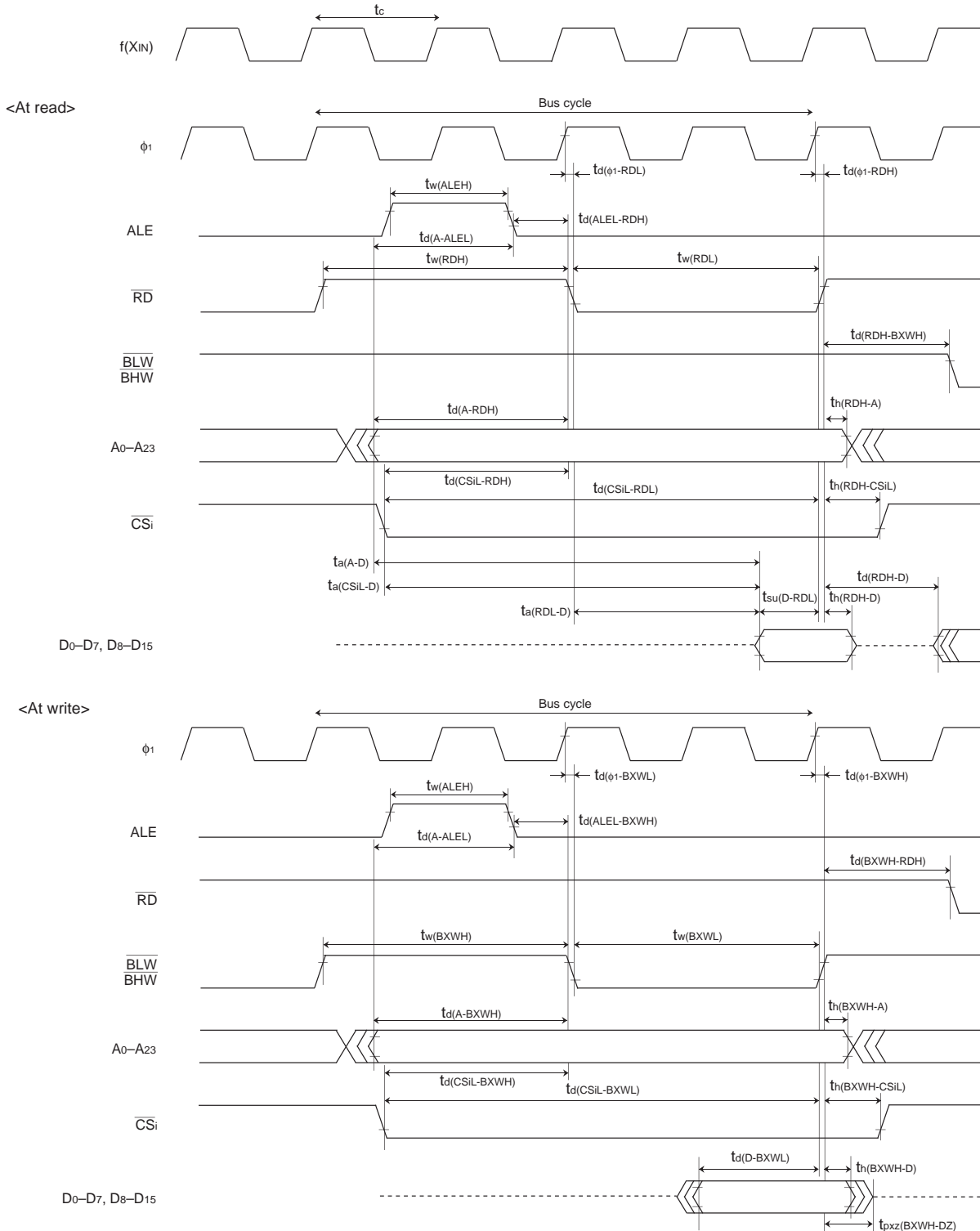
Normal access: 0/1/2 wait



**Test conditions**

- $V_{CC} = 5 V \pm 10 \%$ ,  $T_a = -20$  to  $85 \text{ }^\circ\text{C}$
- Input timing voltage :  $V_{IL} = 0.8 V$ ,  $V_{IH} = 2.5 V$
- Output timing voltage :  $V_{OL} = 0.8 V$ ,  $V_{OH} = 2.0 V$ ,  $C_L = 15 \text{ pF}$  ( $\overline{CSi}$ )
- Output timing voltage :  $V_{OL} = 0.8 V$ ,  $V_{OH} = 2.0 V$ ,  $C_L = 50 \text{ pF}$  (except for  $\overline{CSi}$ )

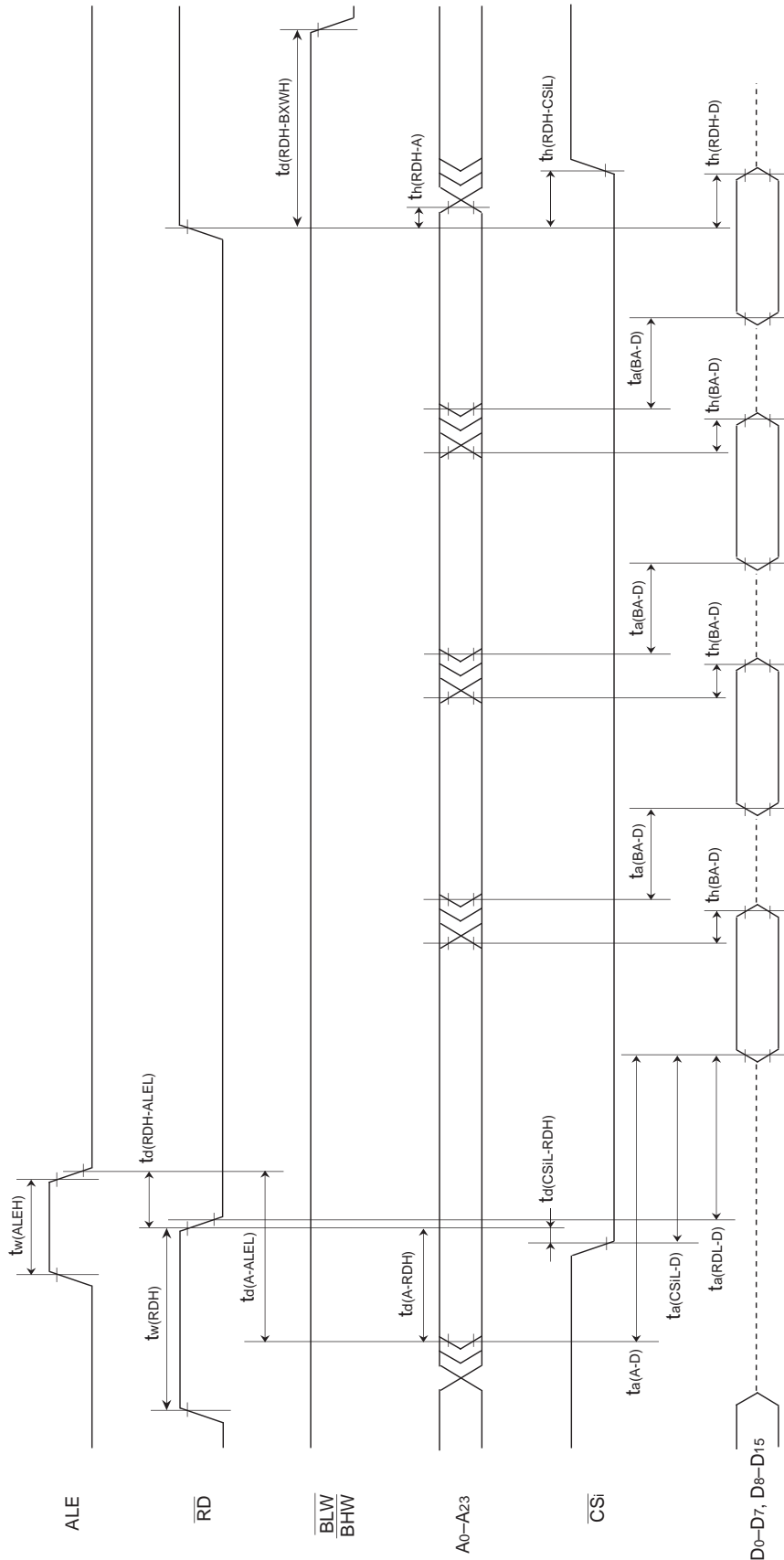
Normal access : ALE extension wait



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = -20\text{ to }85\text{ }^\circ\text{C}$
- Input timing voltage :  $V_{IL} = 0.8\text{ V}$ ,  $V_{IH} = 2.5\text{ V}$
- Output timing voltage :  $V_{OL} = 0.8\text{ V}$ ,  $V_{OH} = 2.0\text{ V}$ ,  $C_L = 15\text{ pF}$  (CSi)
- Output timing voltage :  $V_{OL} = 0.8\text{ V}$ ,  $V_{OH} = 2.0\text{ V}$ ,  $C_L = 50\text{ pF}$  (except for CSi)

Burst ROM access : 0/1/2 wait at instruction prefetch



- Test conditions
- $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = -20$  to  $85\text{ }^\circ\text{C}$
  - Input timing voltage :  $V_{IL} = 0.8\text{ V}$ ,  $V_{IH} = 2.5\text{ V}$
  - Output timing voltage :  $V_{OL} = 0.8\text{ V}$ ,  $V_{OH} = 2.0\text{ V}$ ,  $C_L = 15\text{ pF}$  (CSi)
  - Output timing voltage :  $V_{OL} = 0.8\text{ V}$ ,  $V_{OH} = 2.0\text{ V}$ ,  $C_L = 50\text{ pF}$  (except for CSi)

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

**DRAM access**

**Timing Requirements** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 0\text{ to }70\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 20\text{ MHz}$ , unless otherwise noted)

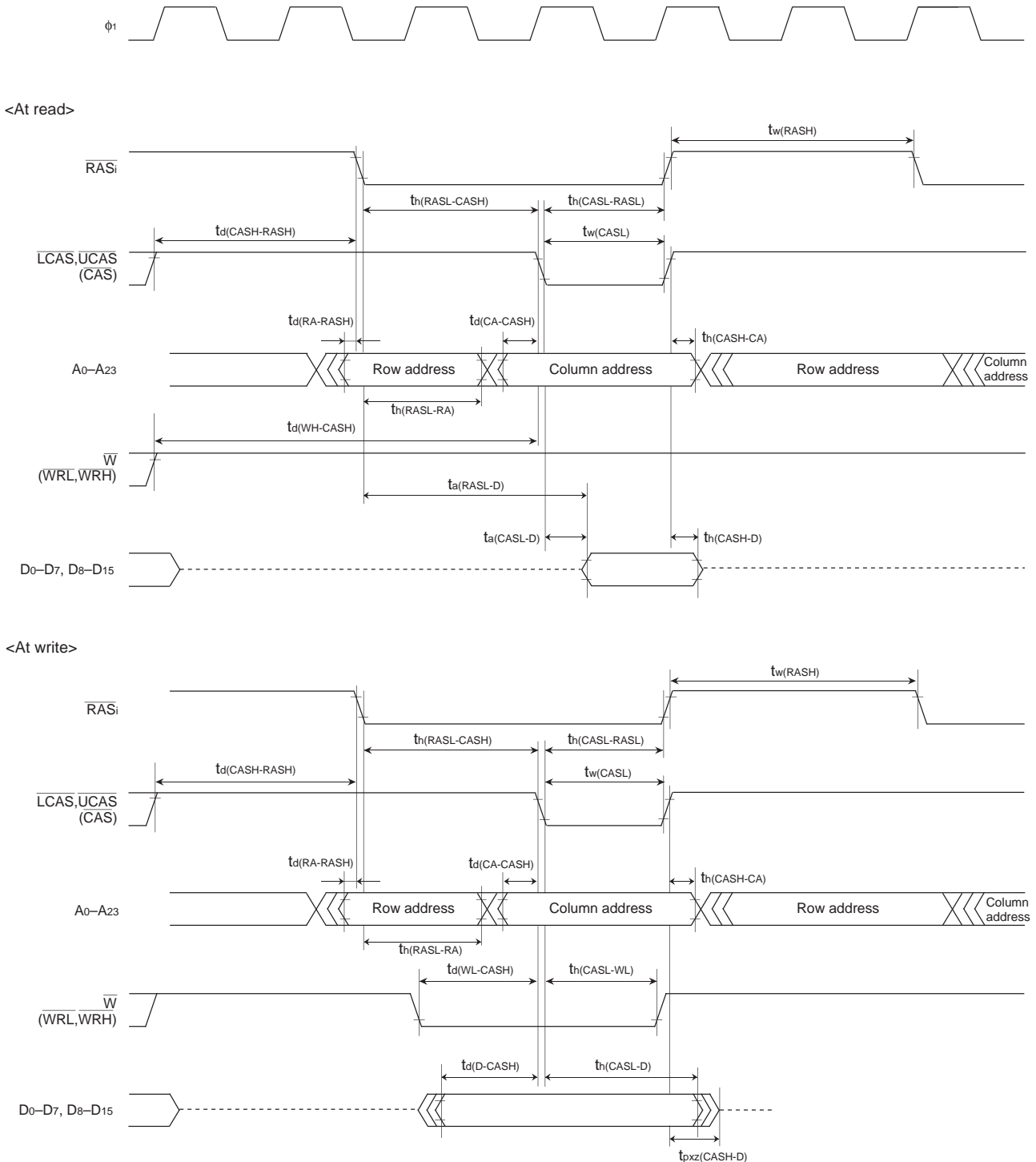
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_a(\text{RASL-D})$	$\overline{\text{RAS}}$ access time		$2.5t_c - 35$	ns
$t_a(\text{CASL-D})$	$\overline{\text{CAS}}$ access time		$t_c - 30$	ns
$t_h(\text{CASH-D})$	Data input hold time after $\overline{\text{CAS}}$	0		ns

**Switching characteristics** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 0\text{ to }70\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 20\text{ MHz}$ , unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_w(\text{RASH})$	$\overline{\text{RAS}}$ high-level pulse width	$1.5t_c - 20$		ns
$t_d(\text{CASH-RASH})$	$\overline{\text{CAS}}$ high-level valid time before $\overline{\text{RAS}}$	$1.5t_c - 20$		ns
$t_h(\text{RASL-CASH})$	$\overline{\text{CAS}}$ high-level hold time after $\overline{\text{RAS}}$ 's low level	$1.5t_c - 20$		ns
$t_h(\text{CASL-RASL})$	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ 's low level	$t_c - 15$		ns
$t_w(\text{CASL})$	$\overline{\text{CAS}}$ low-level pulse width	$t_c - 15$		ns
$t_d(\text{RA-RASH})$	Row address valid time before $\overline{\text{RAS}}$	$0.5t_c - 25$		ns
$t_h(\text{RASL-RA})$	Row address hold time after $\overline{\text{RAS}}$ 's low level	$t_c - 40$		ns
$t_d(\text{CA-CASH})$	Column address valid time before $\overline{\text{CAS}}$	$0.5t_c - 20$		ns
$t_h(\text{CASH-CA})$	Column address hold time after $\overline{\text{CAS}}$ 's high level	0		ns
$t_d(\text{WH-CASH})$	$\overline{\text{W}}$ high-level valid time before $\overline{\text{CAS}}$	$3t_c - 15$		ns
$t_d(\text{WL-CASH})$	$\overline{\text{W}}$ low-level valid time before $\overline{\text{CAS}}$	$t_c - 15$		ns
$t_h(\text{CASL-WL})$	$\overline{\text{W}}$ hold time after $\overline{\text{CAS}}$ 's low level	$t_c - 15$		ns
$t_d(\text{D-CASH})$	Data output valid time before $\overline{\text{CAS}}$	$t_c - 20$		ns
$t_h(\text{CASL-D})$	Data output hold time after $\overline{\text{CAS}}$ 's low level	$1.5t_c - 15$		ns
$t_{pxz}(\text{CASH-D})$	Floating start delay time after $\overline{\text{CAS}}$	$0.5t_c + 10$		ns
$t_d(\text{CAF-CASH})$	Column address valid time before $\overline{\text{CAS}}$ (When fast page access ON is selected)	$t_c - 40$		ns
$t_d(\text{WFL-CASH})$	$\overline{\text{W}}$ low-level valid time before $\overline{\text{CAS}}$ (When fast page access ON is selected)	$0.5t_c - 20$		ns
$t_d(\text{DF-CASH})$	Data output valid time before $\overline{\text{CAS}}$ (When fast page access ON is selected)	$0.5t_c - 20$		ns
$t_{pxz}(\text{WH-D})$	Floating start delay time after write		$0.5t_c + 10$	ns



DRAM access : fast page access = OFF

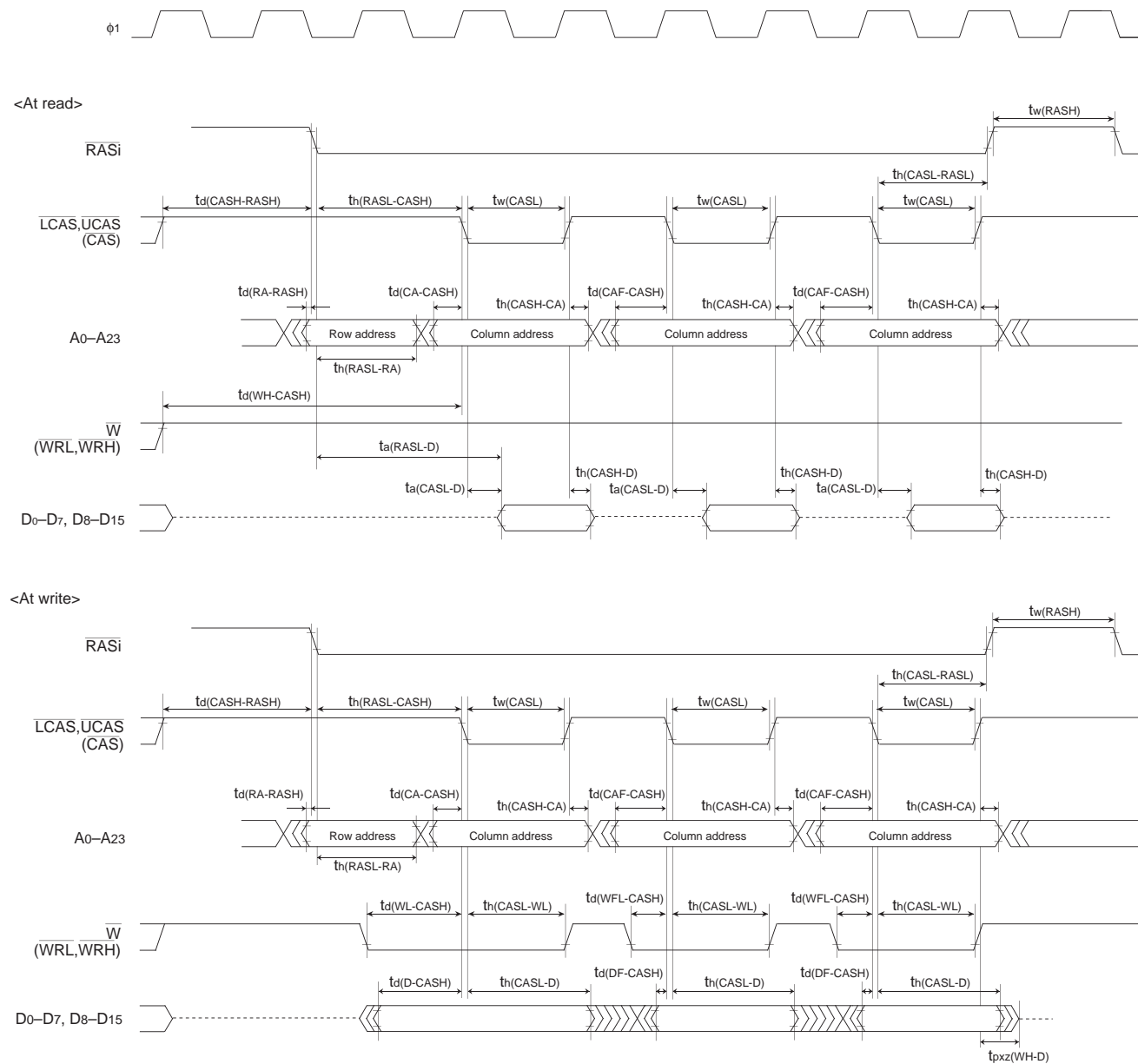


Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = 0$  to  $70^\circ\text{C}$
- Input timing voltage :  $V_{IL} = 0.8\text{ V}$ ,  $V_{IH} = 2.5\text{ V}$
- Output timing voltage :  $V_{OL} = 0.8\text{ V}$ ,  $V_{OH} = 2.0\text{ V}$ ,  $C_L = 15\text{ pF}$  ( $\overline{RAS}_i$ )
- Output timing voltage :  $V_{OL} = 0.8\text{ V}$ ,  $V_{OH} = 2.0\text{ V}$ ,  $C_L = 50\text{ pF}$  (except for  $\overline{RAS}_i$ )

**PRELIMINARY**  
Notice: This is not a final specification.  
Some parametric limits are subject to change.

DRAM access : fast page access = ON



Test conditions  
 •V<sub>CC</sub> = 5 V ± 10 %, T<sub>a</sub> = 0 to 70 °C  
 •Input timing voltage : V<sub>IL</sub> = 0.8 V, V<sub>IH</sub> = 2.5 V  
 •Output timing voltage : V<sub>OL</sub> = 0.8 V, V<sub>OH</sub> = 2.0 V, C<sub>L</sub> = 15 pF ( $\overline{\text{RASi}}$ )  
 •Output timing voltage : V<sub>OL</sub> = 0.8 V, V<sub>OH</sub> = 2.0 V, C<sub>L</sub> = 50 pF (except for  $\overline{\text{RASi}}$ )

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to change.

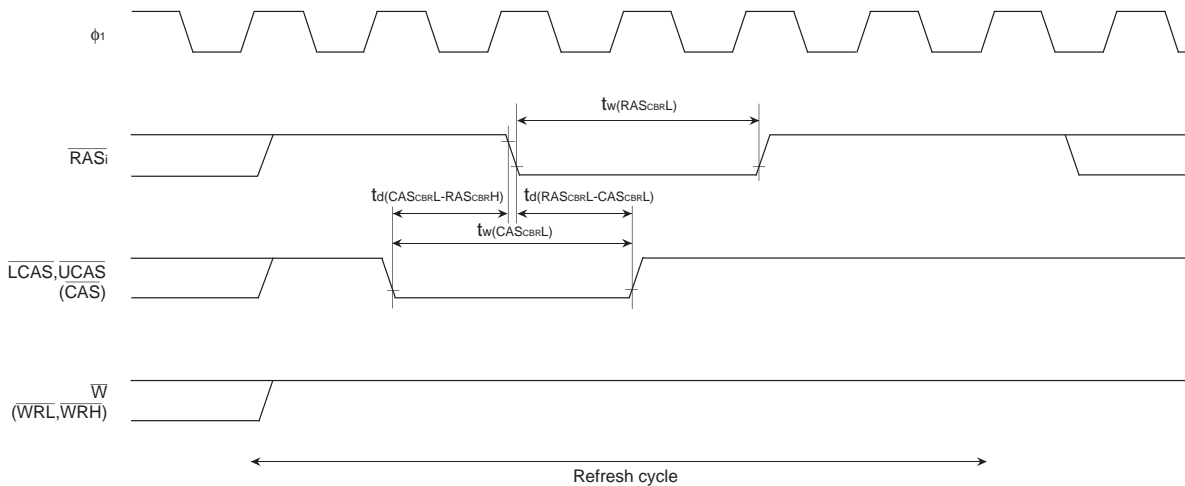
## DRAM refresh

**Switching characteristics** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 0\text{ to }70\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 20\text{ MHz}$ , unless otherwise noted)

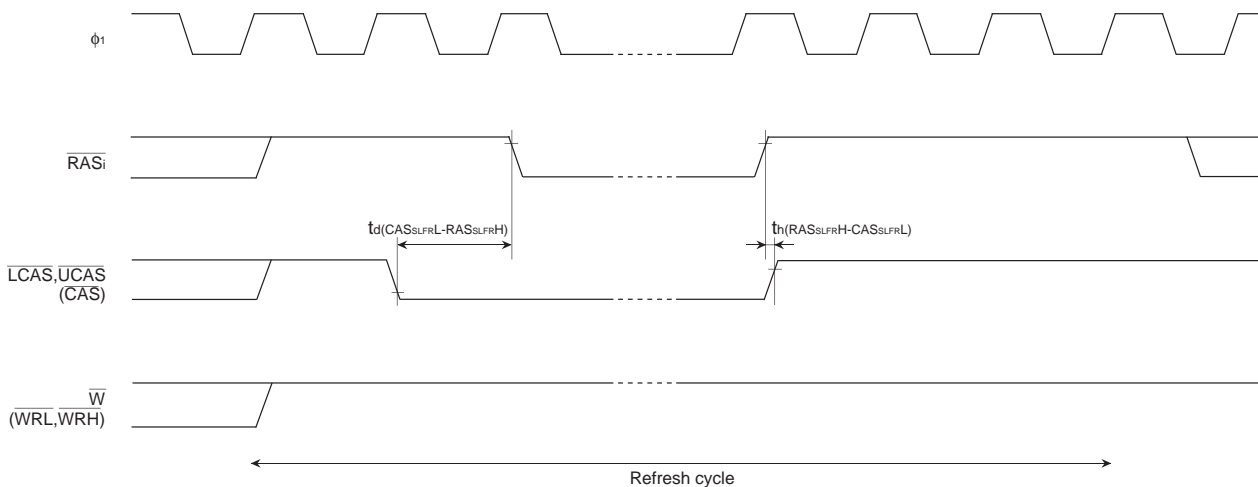
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_w(\overline{\text{RAS}}_{\text{CBRL}})$	$\overline{\text{RAS}}$ low-level pulse width (At $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	$2t_c - 15$		ns
$t_w(\overline{\text{CAS}}_{\text{CBRL}})$	$\overline{\text{CAS}}$ low-level pulse width (At $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	$2t_c - 15$		ns
$t_d(\overline{\text{CAS}}_{\text{CBRL}} - \overline{\text{RAS}}_{\text{CBRH}})$	$\overline{\text{RAS}}$ high-level valid time after $\overline{\text{CAS}}$ 's low level start (At $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	$t_c - 15$		ns
$t_d(\overline{\text{RAS}}_{\text{CBRL}} - \overline{\text{CAS}}_{\text{CBRL}})$	$\overline{\text{CAS}}$ low-level valid time after $\overline{\text{RAS}}$ 's low level start (At $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	$t_c - 15$		ns
$t_d(\overline{\text{CAS}}_{\text{SLFRH}} - \overline{\text{RAS}}_{\text{SLFRH}})$	$\overline{\text{RAS}}$ high-level valid time after $\overline{\text{CAS}}$ 's low level start (At self refresh)	$t_c - 15$		ns
$t_h(\overline{\text{RAS}}_{\text{SLFRH}} - \overline{\text{CAS}}_{\text{SLFRL}})$	$\overline{\text{CAS}}$ low-level hold time after $\overline{\text{RAS}}$ 's high level (At self refresh)	-15	15	ns

**PRELIMINARY**  
Notice: This is not a final specification.  
Some parametric limits are subject to change.

DRAM refresh :  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh



DRAM refresh : self refresh



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = 0\text{ to }70\text{ }^\circ\text{C}$
- Output timing voltage :  $V_{OL} = 0.8\text{ V}$ ,  $V_{OH} = 2.0\text{ V}$ ,  $C_L = 15\text{ pF}$  ( $\overline{\text{RAS}}_i$ )
- Output timing voltage :  $V_{OL} = 0.8\text{ V}$ ,  $V_{OH} = 2.0\text{ V}$ ,  $C_L = 50\text{ pF}$  (except for  $\overline{\text{RAS}}_i$ )

**PRELIMINARY**  
Notice: This is not a final specification.  
Some parametric limits are subject to change.

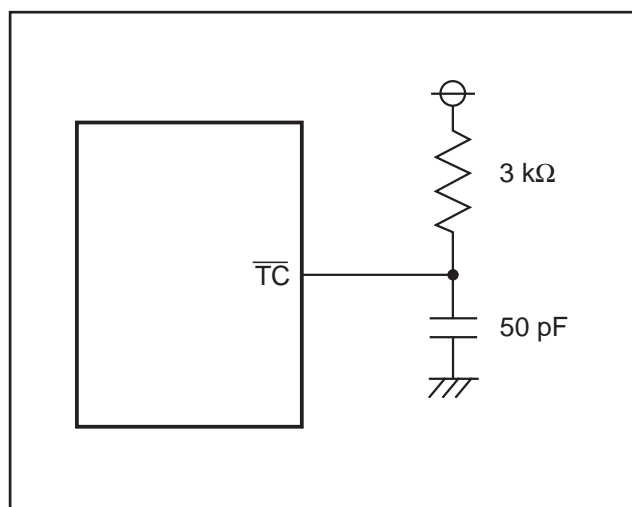
## DMA transfer timing

**Timing Requirements** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }85\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 20\text{ MHz}$ , unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su}(TC_{INL}-\phi_1)$	$\overline{TC}$ input setup time	40		ns
$t_w(TC_{INL})$	$\overline{TC}$ input pulse width	$t_c + 20$		ns
$t_{su}(DRQL-\phi_1)$	$\overline{DMAREQ}_i$ input setup time	40		ns
$t_w(DRQL)$	$\overline{DMAREQ}_i$ input pulse width	$t_c$		ns

**Switching characteristics** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }85\text{ }^\circ\text{C}$ ,  $f(X_{IN}) = 20\text{ MHz}$ , unless otherwise noted)

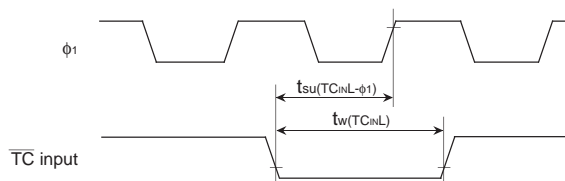
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_w(TCL)$	$\overline{TC}$ output pulse width	$t_c - 20$		ns
$t_d(RDH-TCL)$	$\overline{TC}$ output start delay time after read	$t_c - 15$		ns
$t_d(BXWH-TCL)$	$\overline{TC}$ output start delay time after write	$t_c - 15$		ns
$t_d(TCL-DMAACKL)$	$\overline{DMAACK}$ low-level output valid time after $\overline{TC}$ output start	$2.5t_c - 20$		ns



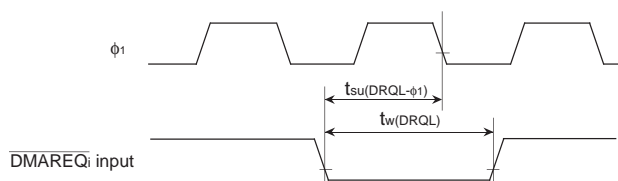
Test circuit for  $\overline{TC}$  output

**PRELIMINARY**  
Notice: This is not a final specification.  
Some parametric limits are subject to change.

●  $\overline{TC}$  input



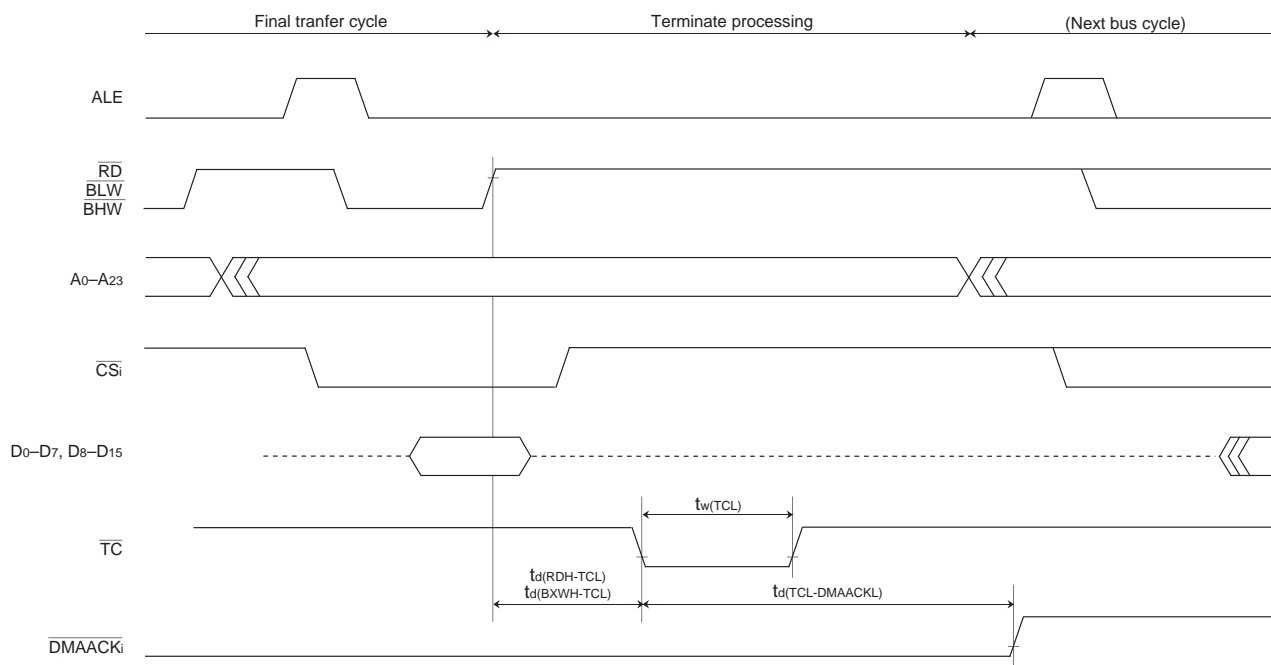
●  $\overline{DMAREQ}_i$  input



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = -20$  to  $85\text{ }^\circ\text{C}$
- Input timing voltage :  $V_{IL} = 1.0\text{ V}$ ,  $V_{IH} = 4.0\text{ V}$
- Output timing voltage :  $V_{OL} = 0.8\text{ V}$ ,  $V_{OH} = 2.0\text{ V}$ ,  $C_L = 50\text{ pF}$

● Transfer terminate timing



Test conditions

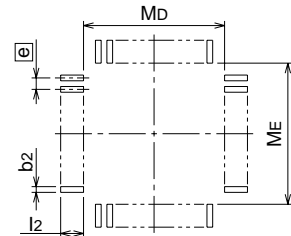
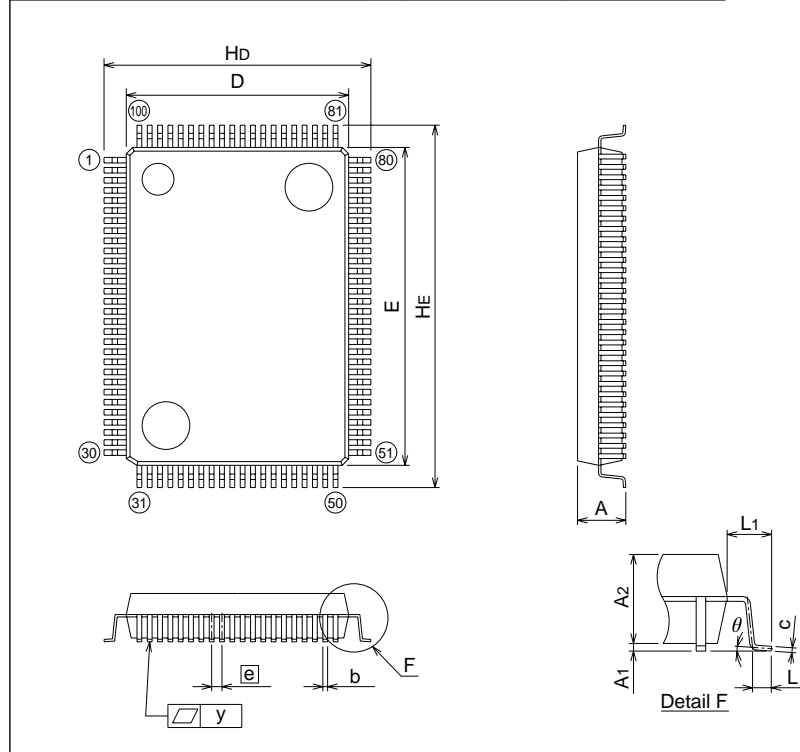
- $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = -20$  to  $85\text{ }^\circ\text{C}$
- Output timing voltage :  $V_{OL} = 0.8\text{ V}$ ,  $V_{OH} = 2.0\text{ V}$ ,  $C_L = 50\text{ pF}$

**PACKAGE OUTLINE**

**100P6S-A**

**Plastic 100pin 14X20mm body QFP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	-	1.58	Alloy 42



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	3.05
A1	0	0.1	0.2
A2	-	2.8	-
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	-	0.65	-
Hd	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	-	1.4	-
y	-	-	0.1
theta	0°	-	10°
b2	-	0.35	-
l2	1.3	-	-
MD	-	14.6	-
ME	-	20.6	-

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REVISION DESCRIPTION LIST

M37920S4CGP Datasheet

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1.00	First Edition	990916