

M16C/6N4 Group

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0003-0100Z
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1. Overview

The M16C/6N4 group of single-chip microcomputers are built using the high-performance silicon gate CMOS process using an M16C/60 Series CPU core and are packaged in a 100-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed. Being equipped with two CAN (Controller Area Network) modules in M16C/6N4 group, the microcomputer is suited to drive automotive and industrial control systems. The CAN modules comply with the 2.0B specification. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Automotive, industrial control systems and other automobile, other

1.2 Performance Outline

Table 1.1 lists a performance outline of M16C/6N4 group.

Table 1.1 Performance outline of M16C/6N4 Group

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		50.0 ns (f(BCLK)=20MHz, 1/1 prescaler, without software wait)
Memory capacity	ROM	(Refer to the product list)
	RAM	(Refer to the product list)
I/O port	P0 to P10 (except P8 ₅)	8 bits × 10, 7 bits × 1
Input port	P8 ₅	1 bit × 1 (NMI pin level judgment)
Multifunction timer	TA0, TA1, TA2, TA3, TA4	Output: 16 bits × 5 channels
	TB0, TB1, TB2, TB3, TB4, TB5	Input: 16 bits × 6 channels
Serial I/O	UART0, UART1, UART2	3 channels: UART, clock synchronous, I ² C-bus (Note 1) (option) or IEBus (Note 2) (option)
	SI/O3	1 channel: Clock synchronous
A-D converter		10 bits × (8 × 3 + 2) channels
D-A converter		8 bits × 2 channels
DMAC		2 channels (trigger: 24 sources)
CRC calculation circuit		1 circuit: CRC-CCITT
CAN Module		2 channels with 2.0B specification
Watchdog timer		15 bits × 1 (with prescaler)
Interrupt		31 internal and 9 external sources, 4 software sources, 7 levels
Clock generation circuit		4 circuits <ul style="list-style-type: none"> · Main clock } These circuit contain a built-in feedback resistor; · Sub clock } and external ceramic/quartz oscillator · Ring oscillator · PLL frequency synthesizer Main clock oscillation stop and re-oscillation detection function
Power supply voltage		4.2 to 5.5V (f(BCLK) = 20MHz, 1/1 prescaler, without software wait)
Flash memory	Program/erase voltage	5.0 ± 0.5 V
	Number of program/erase	100 times
Power consumption		Mask ROM version: 18 mA (V _{cc} =5V, (f(BCLK)=20MHz, 1/1 prescaler, without software wait) Flash memory version: 20 mA (V _{cc} =5V, (f(BCLK)=20MHz, 1/1 prescaler, without software wait)
I/O characteristics	I/O withstand voltage	5.0 V
	Output current	5 mA
Operating ambient temperature		-40 to 85°C (T version) -40 to 125°C (V version) (option)
Memory expansion		Available (to 1 Mbyte)
Device configuration		CMOS high performance silicon gate
Package		100-pin plastic mold QFP

Note 1: I²C-bus is a registered trademark of Koninklijke Philips Electronics N.V.

Note 2: IEBus is a registered trademark of NEC Electronics Corporation.

option: If you desire this option, please so specify.

1.3 Block Diagram

Figure 1.1 shows a block diagram of M16C/6N4 group.

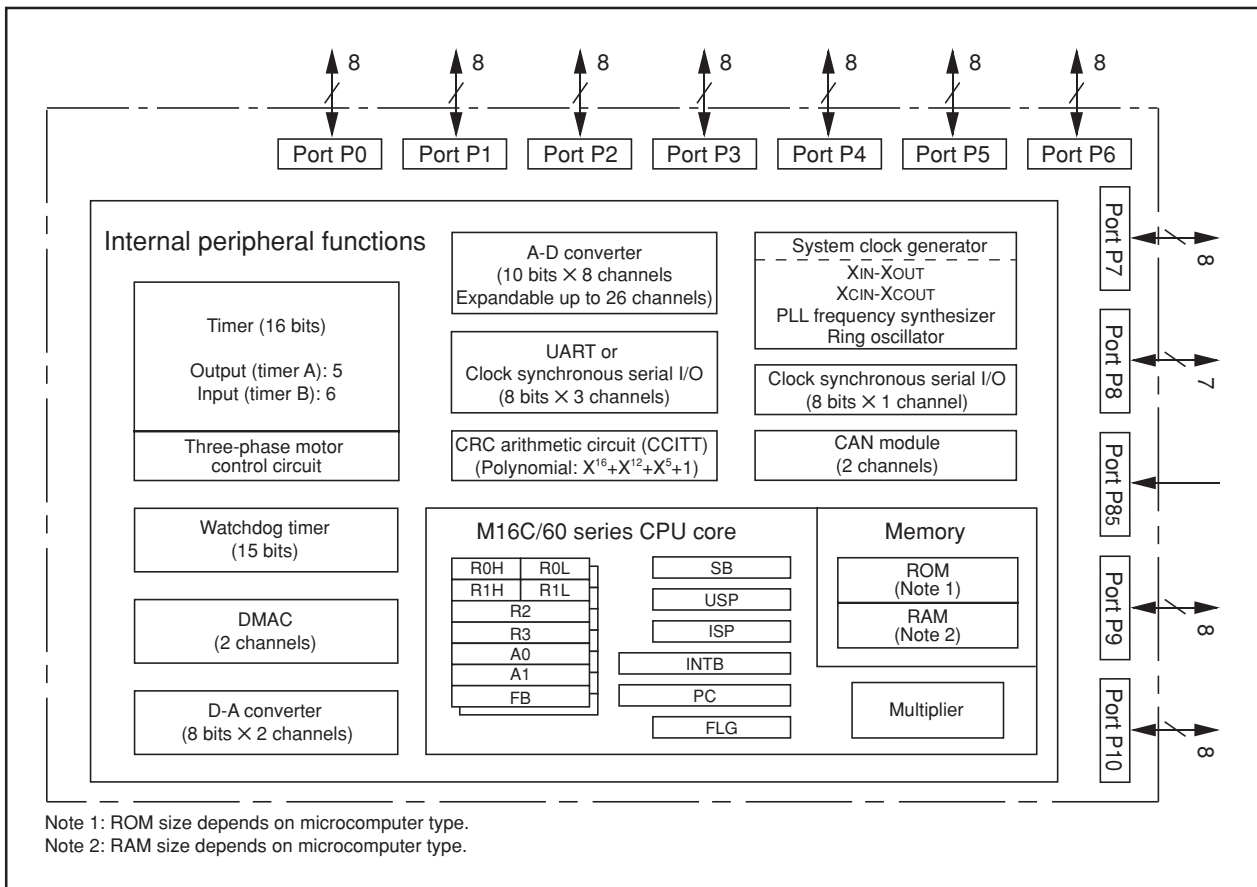


Figure 1.1 Block Diagram

1.4 Product List

Table 1.2 lists the M16C/6N4 group products and Figure 1.2 shows the type numbers, memory sizes and packages.

Table 1.2 Product List

As of May 2003

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M306N4MCT-XXXFP **	128 Kbytes	5 Kbytes	100P6S-A	Mask ROM version
M306N4MCV-XXXFP *				Flash memory version
M306N4FCTFP **				
M306N4FCVFP *	256 Kbytes	10 Kbytes	100P6S-A	Mask ROM version
M306N4MGT-XXXFP *				Flash memory version
M306N4MGV-XXXFP *				
M306N4FGTFP **				
M306N4FGVFP *				

*: Under planning

** : Under development

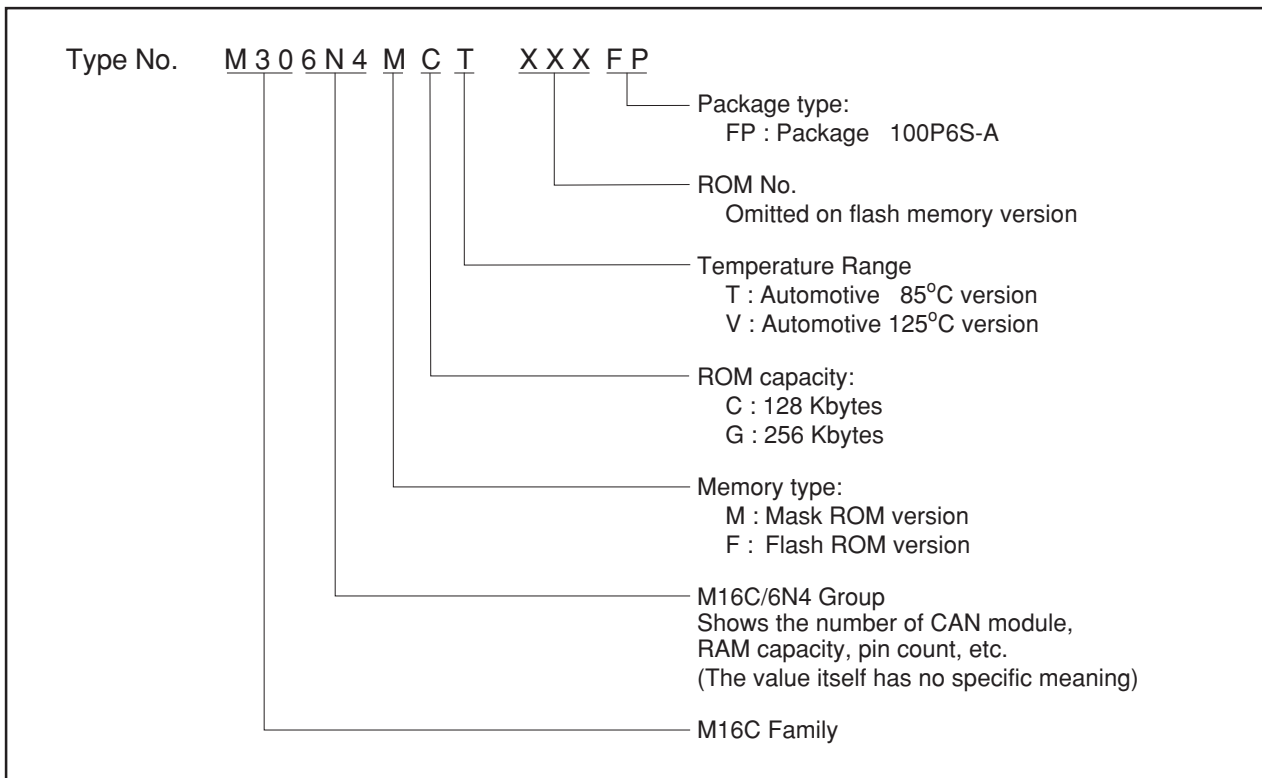


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Configuration

Figure 1.3 shows the pin configuration (top view).

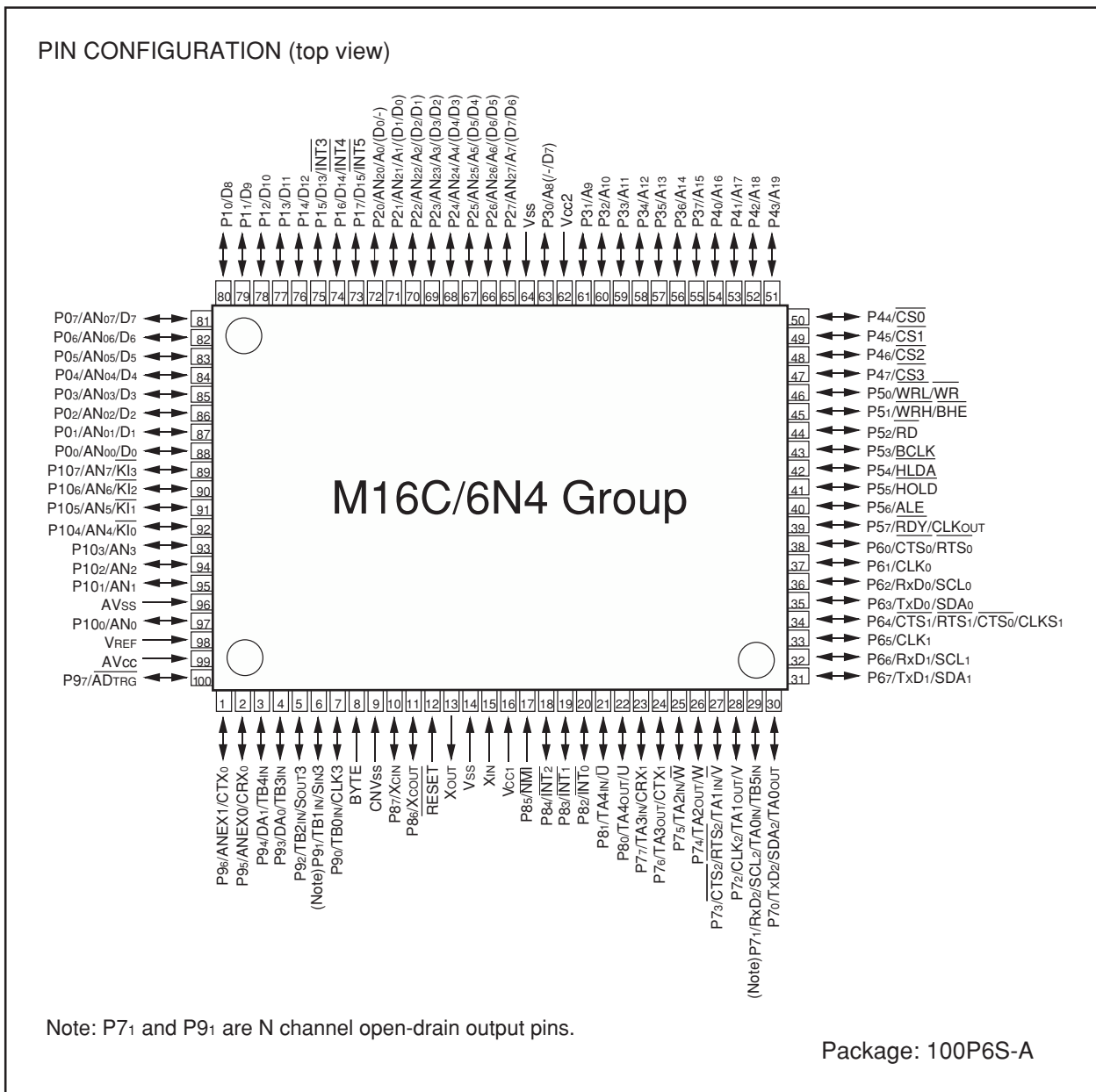


Figure 1.3 Pin Configuration (Top View)

1.6 Pin Description

Tables 1.3 and 1.4 list the pin descriptions.

Table 1.3 Pin Description (1)

Pin name	Signal name	I/O type	Function
VCC1, VCC2 VSS	Power supply input		Apply 4.2 to 5.5 V to the VCC1 and VCC2 pins and 0 V to the VSS pin. The VCC apply condition is that $VCC2 = VCC1$.
CNVSS	CNVSS	Input	This pin switches between processor modes. Connect this pin to the VSS pin when after a reset you want to start operation in single-chip mode (memory expansion mode) or the VCC1 pin when starting operation in microprocessor mode.
RESET	Reset input	Input	"L" on this input resets the microcomputer.
XIN	Clock input	Input	These pins are provided for the main clock oscillation circuit input/output. Connect a ceramic resonator or crystal between the XIN and the XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
XOUT	Clock output	Output	
BYTE	External data bus width select input	Input	This pin selects the width of an external data bus. A 16-bit width is selected when this input is "L"; an 8-bit width is selected when this input is "H". This input must be fixed to either "H" or "L". Connect this pin to the VSS pin when operating in single-chip mode.
AVCC	Analog power supply input		This pin is a power supply input for the A-D converter. Connect this pin to VCC1.
AVSS	Analog power supply input		This pin is a power supply input for the A-D converter. Connect this pin to VSS.
VREF	Reference voltage input	Input	This pin is a reference voltage input for the A-D converter and D-A converter.
P0 to P07	I/O port P0	Input/output	This is an 8-bit CMOS I/O port. This port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. If any port is set for input, selection can be made for it in a program whether or not to have a pull-up resistor in 4-bit unit. This selection is unavailable in memory expansion and microprocessor modes. This port can function as input pins for the A-D converter when so selected in a program.
D0 to D7		Input/output	
P10 to P17	I/O port P1	Input/output	This is an 8-bit I/O port equivalent to P0. P15 to P17 also function as \overline{INT} interrupt input pins as selected by a program.
D8 to D15		Input/output	
P20 to P27	I/O port P2	Input/output	This is an 8-bit I/O port equivalent to P0. This port can function as input pins for the A-D converter when so selected in a program.
A0 to A7		Output	
A0/D0 to A7/D7		Input/output	If the external bus is set as an 8-bit width multiplexed bus, these pins input and output data (D0 to D7) and output 8 low-order address bits (A0 to A7) separated in time by multiplexing.
A0, A1/D0 to A7/D6		Output Input/output	If the external bus is set as a 16-bit width multiplexed bus, these pins input and output data (D0 to D6) and output address (A1 to A7) separated in time by multiplexing. They also output address (A0).
P30 to P37	I/O port P3	Input/output	This is an 8-bit I/O port equivalent to P0.
A8 to A15		Output	
A8/D7, A9 to A15		Input/output Output	If the external bus is set as a 16-bit width multiplexed bus, these pins input and output data (D7) and output address (A8) separated in time by multiplexing. They also output address (A9 to A15).
P40 to P47	I/O port P4	Input/output	This is an 8-bit I/O port equivalent to P0.
A16 to A19, $\overline{CS0}$ to $\overline{CS3}$		Output Output	

Table 1.4 Pin Description (2)

Pin name	Signal name	I/O type	Function
P50 to P57	I/O port P5	Input/output	This is an 8-bit I/O port equivalent to P0. In single-chip mode, P57 in this port outputs a divide-by-8 or divide-by-32 clock of XIN or a clock of the same frequency as XCIN as selected by program.
\overline{WRL} / \overline{WR} , \overline{WRH} / \overline{BHE} , \overline{RD} , \overline{BCLK} , \overline{HLDA} , \overline{HOLD} , \overline{ALE} , \overline{RDY}		Output Output Output Output Input Output Input	Output $\overline{WRL}/\overline{WR}$, $\overline{WRH}/\overline{BHE}$, \overline{RD} , \overline{BCLK} , \overline{HLDA} , and \overline{ALE} signals. $\overline{WRL}/\overline{WR}$ and $\overline{WRH}/\overline{BHE}$ are switchable in a program. Note that \overline{WRL} and \overline{WRH} are always used as a pair, so as \overline{WR} and \overline{BHE} . <ul style="list-style-type: none"> ■ \overline{WRL}, \overline{WRH}, and \overline{RD} selected If the external data bus is a 16-bit width, data are written to even addresses when the \overline{WRL} signal is low, and written to odd addresses when the \overline{WRH} signal is low. Data are read out when the \overline{RD} signal is low. ■ \overline{WR}, \overline{BHE}, and \overline{RD} selected Data are written when the \overline{WR} signal is low, or read out when the \overline{RD} signal is low. Odd addresses are accessed when the \overline{BHE} signal is low. Use this mode when the external data bus is an 8-bit width. The microcomputer goes to a hold state when input to the \overline{HOLD} pin is held low. While in the hold state, \overline{HLDA} outputs a low level. \overline{ALE} is used to latch the address. While the input level of the \overline{RDY} pin is low, the bus of the microcomputer goes to a wait state.
P60 to P67	I/O port P6	Input/output	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as UART0 and UART1 I/O pins as selected by program.
P70 to P77	I/O port P7	Input/output	This is an 8-bit I/O port equivalent to P0 (P71 is an N channel open-drain output). This port can function as input/output pins for timers A0 to A3 when so selected in a program. Furthermore, P70 to P73, P71, P72 to P75 and P76, P77 can also function as input/output pins for UART2, an input pin for timer B5, output pins for the three-phase motor control timer, and input/output pin for the CAN1, respectively.
P80 to P84, P86, P87	I/O port P8	Input/output Input/output Input/output	P80 to P84, P86 and P87 are I/O ports with the same functions as P0. When so selected in a program, P80, P81, and P82 to P84 can function as input/output pins for timer A4 or output pins for the three-phase motor control timer and \overline{INT} interrupt input pins, respectively. P86 and P87, when so selected in a program, both can function as input/output pins for the sub clock oscillator circuit. In that case, connect a crystal resonator between P86 (XCOUT pin) and P87 (XCIN pin).
P85	Input port P85	Input	P85 is an input-only port shared with NMI. An NMI interrupt request is generated when input on this pin changes state from high to low. The NMI function cannot be disabled in a program. A pull-up cannot be set for this pin.
P90 to P97	I/O port P9	Input/output	This is an 8-bit I/O port equivalent to P0 (P91 is an N channel open-drain output). Pins in this port also function as input/output pins for SI/O3, input pins for times B0 to B4, output pins for D-A converter, and input pins for A-D converter or input/output pins for CAN0, or input pins for A-D trigger as selected by program.
P100 to P107	I/O port P10	Input/output	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as input pins for A-D converter as selected by program. Furthermore, P104 to P107 also function as input pins for the key input interrupt function.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

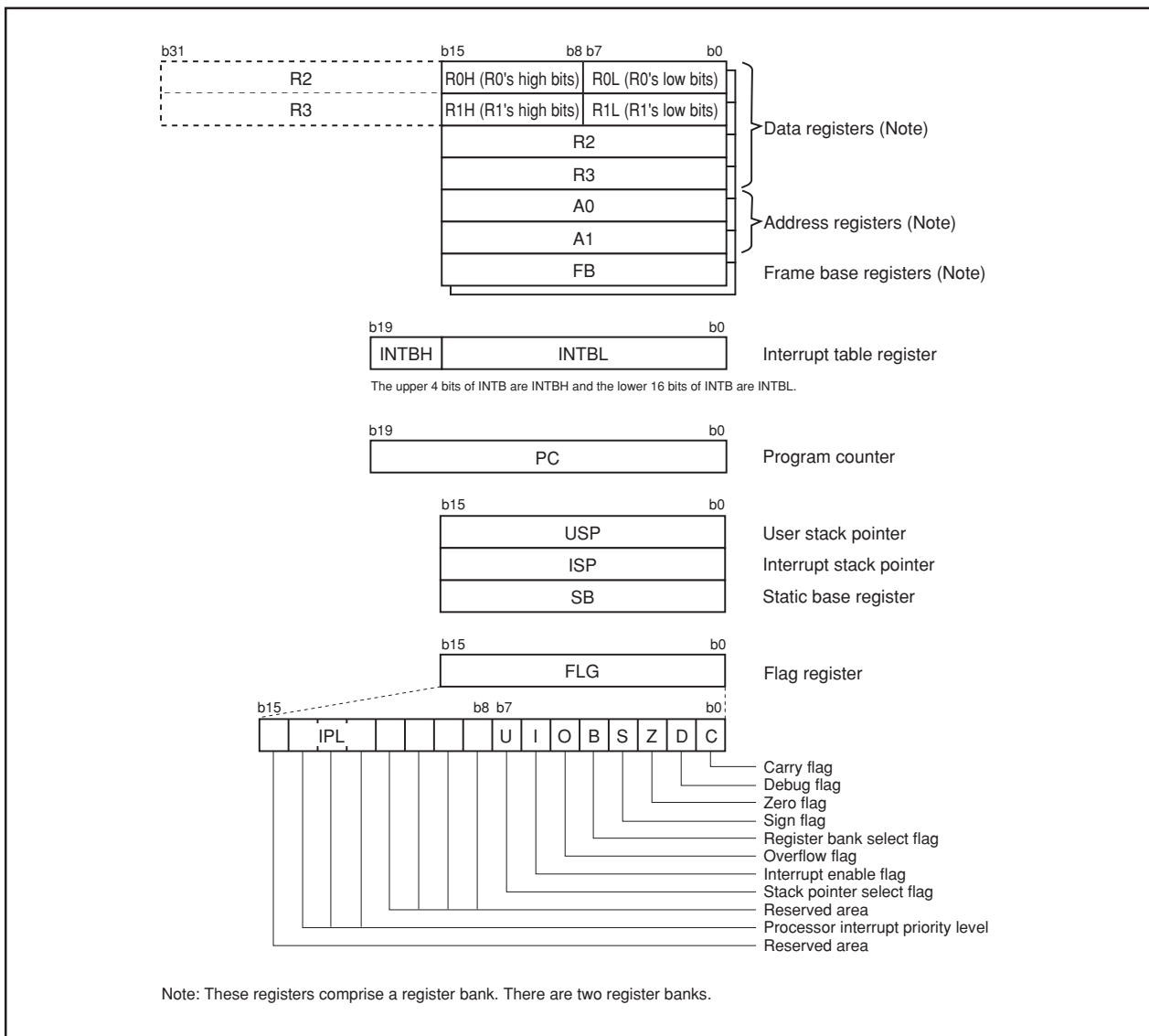


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The A0 register consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

This flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is set to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is set to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt request is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 shows a memory map of the M16C/6N4 group. The address space extends the 1 Mbyte from address 00000₁₆ to FFFFF₁₆.

The internal ROM is allocated in a lower address direction beginning with address FFFFF₁₆. For example, a 128-Kbyte internal ROM is allocated to the addresses from E0000₁₆ to FFFFF₁₆.

The fixed interrupt vector table is allocated to the addresses from FFFDC₁₆ to FFFFF₁₆. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400₁₆. For example, a 5-Kbyte internal RAM is allocated to the addresses from 00400₁₆ to 017FF₁₆. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SFR is allocated to the addresses from 00000₁₆ to 003FF₁₆. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.

The special page vector table is allocated to the addresses from FFE00₁₆ to FFFDB₁₆. This vector is used by the JMPS or JSRS instruction. For details, refer to the "M16C/60 and M16C/20 Series Software Manual".

In memory expansion and microprocessor modes, some areas are reserved for future use and cannot be used by users.

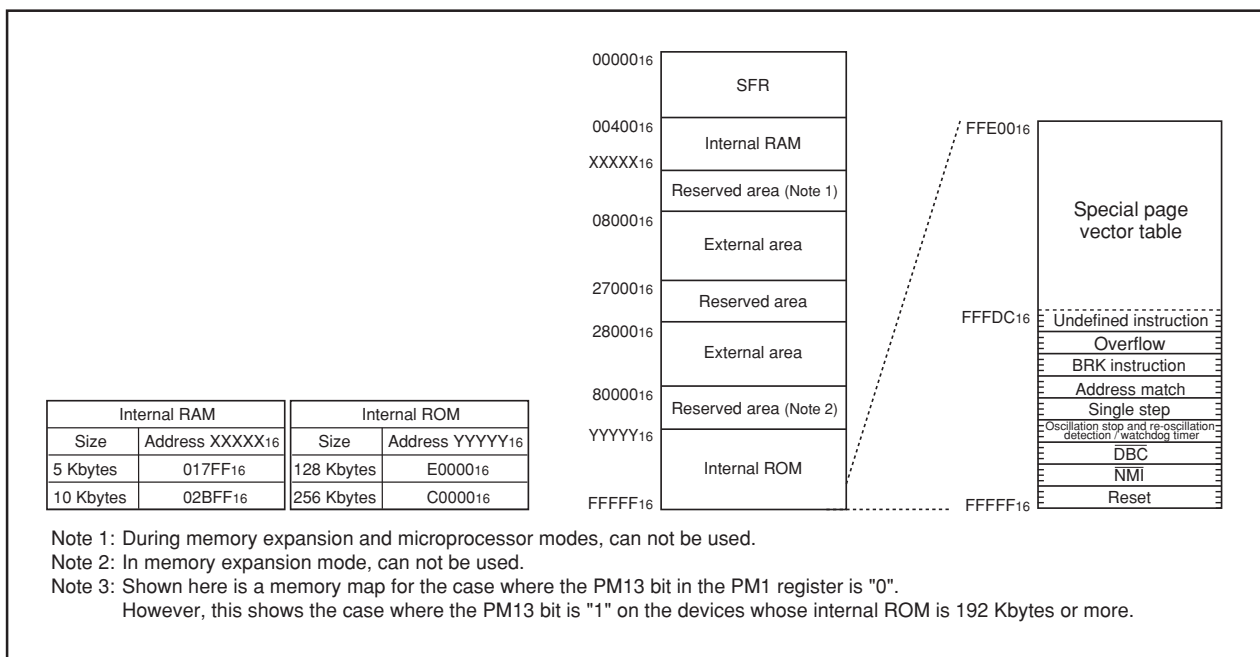


Figure 3.1 Memory Map

4. SFR

Figures 4.1 to 4.16 show the location of peripheral function control registers and the value after reset.

Address	Register	Symbol	After reset
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0 (Note 1)	PM0	00000000 ₂ (CNV _{SS} pin is "L") 00000011 ₂ (CNV _{SS} pin is "H")
0005 ₁₆	Processor mode register 1	PM1	0XXX1000 ₂
0006 ₁₆	System clock control register 0	CM0	01001000 ₂
0007 ₁₆	System clock control register 1	CM1	00100000 ₂
0008 ₁₆	Chip select control register	CSR	00000001 ₂
0009 ₁₆	Address match interrupt enable register	AIER	XXXXXXXX00 ₂
000A ₁₆	Protect register	PRCR	XX000000 ₂
000B ₁₆			
000C ₁₆	Oscillation stop detection register (Note 2)	CM2	0X00X000 ₂
000D ₁₆			
000E ₁₆	Watchdog timer start register	WDTS	XX ₁₆
000F ₁₆	Watchdog timer control register	WDC	00XXXXXX ₂
0010 ₁₆			00 ₁₆
0011 ₁₆	Address match interrupt register 0	RMAD0	00 ₁₆
0012 ₁₆			X0 ₁₆
0013 ₁₆			
0014 ₁₆			00 ₁₆
0015 ₁₆	Address match interrupt register 1	RMAD1	00 ₁₆
0016 ₁₆			X0 ₁₆
0017 ₁₆			
0018 ₁₆			
0019 ₁₆			
001A ₁₆			
001B ₁₆	Chip select expansion control register	CSE	00 ₁₆
001C ₁₆	PLL control register 0	PLC0	0001X010 ₂
001D ₁₆			
001E ₁₆	Processor mode register 2	PM2	XXX00000 ₂
001F ₁₆			
0020 ₁₆			XX ₁₆
0021 ₁₆	DMA0 source pointer	SAR0	XX ₁₆
0022 ₁₆			XX ₁₆
0023 ₁₆			
0024 ₁₆			XX ₁₆
0025 ₁₆	DMA0 destination pointer	DAR0	XX ₁₆
0026 ₁₆			XX ₁₆
0027 ₁₆			
0028 ₁₆	DMA0 transfer counter	TCR0	XX ₁₆
0029 ₁₆			XX ₁₆
002A ₁₆			
002B ₁₆			
002C ₁₆	DMA0 control register	DM0CON	00000X00 ₂
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆			XX ₁₆
0031 ₁₆	DMA1 source pointer	SAR1	XX ₁₆
0032 ₁₆			XX ₁₆
0033 ₁₆			
0034 ₁₆			XX ₁₆
0035 ₁₆	DMA1 destination pointer	DAR1	XX ₁₆
0036 ₁₆			XX ₁₆
0037 ₁₆			
0038 ₁₆	DMA1 transfer counter	TCR1	XX ₁₆
0039 ₁₆			XX ₁₆
003A ₁₆			
003B ₁₆			
003C ₁₆	DMA1 control register	DM1CON	00000X00 ₂
003D ₁₆			
003E ₁₆			
003F ₁₆			

X: Undefined

Note 1: The PM00 and PM01 bits do not change at software reset, watchdog timer reset and oscillation stop detection reset.
 Note 2: The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
 Note 3: The blank areas are reserved and cannot be accessed by users.

Figure 4.1 Location of Peripheral Function Control Registers and Value at After Reset (1)

Address	Register	Symbol	After reset
0040 ₁₆			
0041 ₁₆	CAN0/1 wake up interrupt control register	C01WKIC	XXXXX000 ₂
0042 ₁₆	CAN0 successful reception interrupt control register	C0RECIC	XXXXX000 ₂
0043 ₁₆	CAN0 successful transmission interrupt control register	C0TRMIC	XXXXX000 ₂
0044 ₁₆	INT3 interrupt control register	INT3IC	XX00X000 ₂
0045 ₁₆	Timer B5 interrupt control register	TB5IC	XXXXX000 ₂
0046 ₁₆	Timer B4 interrupt control register	TB4IC	XXXXX000 ₂
	UART1 bus collision detection interrupt control register	U1BCNIC	
0047 ₁₆	Timer B3 interrupt control register	TB3IC	XXXXX000 ₂
	UART0 bus collision detection interrupt control register	U0BCNIC	
0048 ₁₆	CAN1 successful reception interrupt control register	C1RECIC	XX00X000 ₂
	INT5 interrupt control register	INT5IC	
0049 ₁₆	CAN1 successful transmission interrupt control register	C1TRMIC	XX00X000 ₂
	SI/O3 interrupt control register	S3IC	
	INT4 interrupt control register	INT4IC	
004A ₁₆	UART2 bus collision detection interrupt control register	U2BCNIC	XXXXX000 ₂
004B ₁₆	DMA0 interrupt control register	DM0IC	XXXXX000 ₂
004C ₁₆	DMA1 interrupt control register	DM1IC	XXXXX000 ₂
004D ₁₆	CAN0/1 error interrupt control register	C01ERRIC	XXXXX000 ₂
004E ₁₆	A-D conversion interrupt control register	ADIC	XXXXX000 ₂
	Key input interrupt control register	KUPIC	
004F ₁₆	UART2 transmit interrupt control register	S2TIC	XXXXX000 ₂
0050 ₁₆	UART2 receive interrupt control register	S2RIC	XXXXX000 ₂
0051 ₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX000 ₂
0052 ₁₆	UART0 receive interrupt control register	S0RIC	XXXXX000 ₂
0053 ₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX000 ₂
0054 ₁₆	UART1 receive interrupt control register	S1RIC	XXXXX000 ₂
0055 ₁₆	Timer A0 interrupt control register	TA0IC	XXXXX000 ₂
0056 ₁₆	Timer A1 interrupt control register	TA1IC	XXXXX000 ₂
0057 ₁₆	Timer A2 interrupt control register	TA2IC	XXXXX000 ₂
0058 ₁₆	Timer A3 interrupt control register	TA3IC	XXXXX000 ₂
0059 ₁₆	Timer A4 interrupt control register	TA4IC	XXXXX000 ₂
005A ₁₆	Timer B0 interrupt control register	TB0IC	XXXXX000 ₂
005B ₁₆	Timer B1 interrupt control register	TB1IC	XXXXX000 ₂
005C ₁₆	Timer B2 interrupt control register	TB2IC	XXXXX000 ₂
005D ₁₆	INT0 interrupt control register	INT0IC	XX00X000 ₂
005E ₁₆	INT1 interrupt control register	INT1IC	XX00X000 ₂
005F ₁₆	INT2 interrupt control register	INT2IC	XX00X000 ₂
0060 ₁₆	CAN0 message box 0: Identifier / DLC		XX ₁₆
0061 ₁₆			XX ₁₆
0062 ₁₆			XX ₁₆
0063 ₁₆			XX ₁₆
0064 ₁₆			XX ₁₆
0065 ₁₆			XX ₁₆
0066 ₁₆	CAN0 message box 0: Data field		XX ₁₆
0067 ₁₆			XX ₁₆
0068 ₁₆			XX ₁₆
0069 ₁₆			XX ₁₆
006A ₁₆			XX ₁₆
006B ₁₆			XX ₁₆
006C ₁₆	CAN0 message box 0: Time stamp		XX ₁₆
006D ₁₆			XX ₁₆
006E ₁₆	CAN0 message box 1: Identifier / DLC		XX ₁₆
006F ₁₆			XX ₁₆
0070 ₁₆			XX ₁₆
0071 ₁₆			XX ₁₆
0072 ₁₆			XX ₁₆
0073 ₁₆			XX ₁₆
0074 ₁₆	CAN0 message box 1: data Field		XX ₁₆
0075 ₁₆			XX ₁₆
0076 ₁₆			XX ₁₆
0077 ₁₆			XX ₁₆
0078 ₁₆			XX ₁₆
0079 ₁₆			XX ₁₆
007A ₁₆	CAN0 message box 1: Time stamp		XX ₁₆
007B ₁₆			XX ₁₆
007C ₁₆			XX ₁₆
007D ₁₆			XX ₁₆
007E ₁₆			XX ₁₆
007F ₁₆			XX ₁₆

X: Undefined

Note: The blank area is reserved and cannot be accessed by users.

Figure 4.2 Location of Peripheral Function Control Registers and Value at After Reset (2)

Address	Register	Symbol	After reset
0080 ₁₆	CAN0 message box 2: Identifier / DLC		XX ₁₆
0081 ₁₆			XX ₁₆
0082 ₁₆			XX ₁₆
0083 ₁₆			XX ₁₆
0084 ₁₆			XX ₁₆
0085 ₁₆			XX ₁₆
0086 ₁₆	CAN0 message box 2: Data field		XX ₁₆
0087 ₁₆			XX ₁₆
0088 ₁₆			XX ₁₆
0089 ₁₆			XX ₁₆
008A ₁₆			XX ₁₆
008B ₁₆			XX ₁₆
008C ₁₆	CAN0 message box 2: Time stamp		XX ₁₆
008D ₁₆			XX ₁₆
008E ₁₆			XX ₁₆
008F ₁₆	CAN0 message box 3: Identifier / DLC		XX ₁₆
0090 ₁₆			XX ₁₆
0091 ₁₆			XX ₁₆
0092 ₁₆			XX ₁₆
0093 ₁₆			XX ₁₆
0094 ₁₆			XX ₁₆
0095 ₁₆	CAN0 message box 3: Data field		XX ₁₆
0096 ₁₆			XX ₁₆
0097 ₁₆			XX ₁₆
0098 ₁₆			XX ₁₆
0099 ₁₆			XX ₁₆
009A ₁₆			XX ₁₆
009B ₁₆	CAN0 message box 3: Time stamp		XX ₁₆
009C ₁₆			XX ₁₆
009D ₁₆			XX ₁₆
009E ₁₆	CAN0 message box 4: Identifier / DLC		XX ₁₆
009F ₁₆			XX ₁₆
00A0 ₁₆			XX ₁₆
00A1 ₁₆			XX ₁₆
00A2 ₁₆			XX ₁₆
00A3 ₁₆			XX ₁₆
00A4 ₁₆	CAN0 message box 4: Data field		XX ₁₆
00A5 ₁₆			XX ₁₆
00A6 ₁₆			XX ₁₆
00A7 ₁₆			XX ₁₆
00A8 ₁₆			XX ₁₆
00A9 ₁₆			XX ₁₆
00AA ₁₆	CAN0 message box 4: Time stamp		XX ₁₆
00AB ₁₆			XX ₁₆
00AC ₁₆			XX ₁₆
00AD ₁₆	CAN0 message box 5: Identifier / DLC		XX ₁₆
00AE ₁₆			XX ₁₆
00AF ₁₆			XX ₁₆
00B0 ₁₆			XX ₁₆
00B1 ₁₆			XX ₁₆
00B2 ₁₆			XX ₁₆
00B3 ₁₆	CAN0 message box 5: Data field		XX ₁₆
00B4 ₁₆			XX ₁₆
00B5 ₁₆			XX ₁₆
00B6 ₁₆			XX ₁₆
00B7 ₁₆			XX ₁₆
00B8 ₁₆			XX ₁₆
00B9 ₁₆	CAN0 message box 5: Time stamp		XX ₁₆
00BA ₁₆			XX ₁₆
00BB ₁₆			XX ₁₆
00BC ₁₆			XX ₁₆
00BD ₁₆			XX ₁₆
00BE ₁₆			XX ₁₆
00BF ₁₆			XX ₁₆

X: Undefined

Figure 4.3 Location of Peripheral Function Control Registers and Value at After Reset (3)

Address	Register	Symbol	After reset
00C0 ₁₆	CAN0 message box 6: Identifier / DLC		XX ₁₆
00C1 ₁₆			XX ₁₆
00C2 ₁₆			XX ₁₆
00C3 ₁₆			XX ₁₆
00C4 ₁₆			XX ₁₆
00C5 ₁₆			XX ₁₆
00C6 ₁₆	CAN0 message box 6: Data field		XX ₁₆
00C7 ₁₆			XX ₁₆
00C8 ₁₆			XX ₁₆
00C9 ₁₆			XX ₁₆
00CA ₁₆			XX ₁₆
00CB ₁₆			XX ₁₆
00CC ₁₆	CAN0 message box 6: Time stamp		XX ₁₆
00CD ₁₆			XX ₁₆
00CE ₁₆			XX ₁₆
00CF ₁₆	CAN0 message box 7: Identifier / DLC		XX ₁₆
00D0 ₁₆			XX ₁₆
00D1 ₁₆			XX ₁₆
00D2 ₁₆			XX ₁₆
00D3 ₁₆			XX ₁₆
00D4 ₁₆			XX ₁₆
00D5 ₁₆	CAN0 message box 7: Data field		XX ₁₆
00D6 ₁₆			XX ₁₆
00D7 ₁₆			XX ₁₆
00D8 ₁₆			XX ₁₆
00D9 ₁₆			XX ₁₆
00DA ₁₆			XX ₁₆
00DB ₁₆	CAN0 message box 7: Time stamp		XX ₁₆
00DC ₁₆			XX ₁₆
00DD ₁₆			XX ₁₆
00DE ₁₆	CAN0 message box 8: Identifier / DLC		XX ₁₆
00DF ₁₆			XX ₁₆
00E0 ₁₆			XX ₁₆
00E1 ₁₆			XX ₁₆
00E2 ₁₆			XX ₁₆
00E3 ₁₆			XX ₁₆
00E4 ₁₆	CAN0 message box 8: Data field		XX ₁₆
00E5 ₁₆			XX ₁₆
00E6 ₁₆			XX ₁₆
00E7 ₁₆			XX ₁₆
00E8 ₁₆			XX ₁₆
00E9 ₁₆			XX ₁₆
00EA ₁₆	CAN0 message box 8: Time stamp		XX ₁₆
00EB ₁₆			XX ₁₆
00EC ₁₆			XX ₁₆
00ED ₁₆	CAN0 message box 9: Identifier / DLC		XX ₁₆
00EE ₁₆			XX ₁₆
00EF ₁₆			XX ₁₆
00F0 ₁₆			XX ₁₆
00F1 ₁₆			XX ₁₆
00F2 ₁₆			XX ₁₆
00F3 ₁₆	CAN0 message box 9: Data field		XX ₁₆
00F4 ₁₆			XX ₁₆
00F5 ₁₆			XX ₁₆
00F6 ₁₆			XX ₁₆
00F7 ₁₆			XX ₁₆
00F8 ₁₆			XX ₁₆
00F9 ₁₆	CAN0 message box 9: Time stamp		XX ₁₆
00FA ₁₆			XX ₁₆
00FB ₁₆			XX ₁₆
00FC ₁₆			XX ₁₆
00FD ₁₆			XX ₁₆
00FE ₁₆			XX ₁₆
00FF ₁₆			XX ₁₆

X: Undefined

Figure 4.4 Location of Peripheral Function Control Registers and Value at After Reset (4)

Address	Register	Symbol	After reset		
0100 ₁₆	CAN0 message box 10: Identifier / DLC		XX ₁₆		
0101 ₁₆			XX ₁₆		
0102 ₁₆			XX ₁₆		
0103 ₁₆			XX ₁₆		
0104 ₁₆			XX ₁₆		
0105 ₁₆			XX ₁₆		
0106 ₁₆	CAN0 message box 10: Data field		XX ₁₆		
0107 ₁₆			XX ₁₆		
0108 ₁₆			XX ₁₆		
0109 ₁₆			XX ₁₆		
010A ₁₆			XX ₁₆		
010B ₁₆			XX ₁₆		
010C ₁₆	CAN0 message box 10: Time stamp		XX ₁₆		
010D ₁₆			XX ₁₆		
010E ₁₆			XX ₁₆		
010F ₁₆			XX ₁₆		
0110 ₁₆			XX ₁₆		
0111 ₁₆			CAN0 message box 11: Identifier / DLC		XX ₁₆
0112 ₁₆	XX ₁₆				
0113 ₁₆	XX ₁₆				
0114 ₁₆	XX ₁₆				
0115 ₁₆	XX ₁₆				
0116 ₁₆	XX ₁₆				
0117 ₁₆	CAN0 message box 11: Data field		XX ₁₆		
0118 ₁₆			XX ₁₆		
0119 ₁₆			XX ₁₆		
011A ₁₆			XX ₁₆		
011B ₁₆			XX ₁₆		
011C ₁₆			XX ₁₆		
011D ₁₆	CAN0 message box 11: Time stamp		XX ₁₆		
011E ₁₆			XX ₁₆		
011F ₁₆			XX ₁₆		
0120 ₁₆			CAN0 message box 12: Identifier / DLC		XX ₁₆
0121 ₁₆					XX ₁₆
0122 ₁₆					XX ₁₆
0123 ₁₆	XX ₁₆				
0124 ₁₆	XX ₁₆				
0125 ₁₆	XX ₁₆				
0126 ₁₆	CAN0 message box 12: Data field		XX ₁₆		
0127 ₁₆			XX ₁₆		
0128 ₁₆			XX ₁₆		
0129 ₁₆			XX ₁₆		
012A ₁₆			XX ₁₆		
012B ₁₆			XX ₁₆		
012C ₁₆	CAN0 message box 12: Time stamp		XX ₁₆		
012D ₁₆			XX ₁₆		
012E ₁₆			XX ₁₆		
012F ₁₆			XX ₁₆		
0130 ₁₆			CAN0 message box 13: Identifier / DLC		XX ₁₆
0131 ₁₆					XX ₁₆
0132 ₁₆	XX ₁₆				
0133 ₁₆	XX ₁₆				
0134 ₁₆	XX ₁₆				
0135 ₁₆	XX ₁₆				
0136 ₁₆	CAN0 message box 13: Data field		XX ₁₆		
0137 ₁₆			XX ₁₆		
0138 ₁₆			XX ₁₆		
0139 ₁₆			XX ₁₆		
013A ₁₆			XX ₁₆		
013B ₁₆			XX ₁₆		
013C ₁₆	CAN0 message box 13: Time stamp		XX ₁₆		
013D ₁₆			XX ₁₆		
013E ₁₆			XX ₁₆		
013F ₁₆			XX ₁₆		

X: Undefined

Figure 4.5 Location of Peripheral Function Control Registers and Value at After Reset (5)

Address	Register	Symbol	After reset
0140 ₁₆	CAN0 message box 14: Identifier /DLC		XX ₁₆
0141 ₁₆			XX ₁₆
0142 ₁₆			XX ₁₆
0143 ₁₆			XX ₁₆
0144 ₁₆			XX ₁₆
0145 ₁₆			XX ₁₆
0146 ₁₆	CAN0 message box 14: Data field		XX ₁₆
0147 ₁₆			XX ₁₆
0148 ₁₆			XX ₁₆
0149 ₁₆			XX ₁₆
014A ₁₆			XX ₁₆
014B ₁₆			XX ₁₆
014C ₁₆	CAN0 message box 14: Time stamp		XX ₁₆
014D ₁₆			XX ₁₆
014E ₁₆			XX ₁₆
014F ₁₆	CAN0 message box 15: Identifier /DLC		XX ₁₆
0150 ₁₆			XX ₁₆
0151 ₁₆			XX ₁₆
0152 ₁₆			XX ₁₆
0153 ₁₆			XX ₁₆
0154 ₁₆			XX ₁₆
0155 ₁₆	CAN0 message box 15: Data field		XX ₁₆
0156 ₁₆			XX ₁₆
0157 ₁₆			XX ₁₆
0158 ₁₆			XX ₁₆
0159 ₁₆			XX ₁₆
015A ₁₆			XX ₁₆
015B ₁₆	CAN0 message box 15: Time stamp		XX ₁₆
015C ₁₆			XX ₁₆
015D ₁₆			XX ₁₆
015E ₁₆	CAN0 global mask register	COGMR	XX ₁₆
015F ₁₆			XX ₁₆
0160 ₁₆			XX ₁₆
0161 ₁₆			XX ₁₆
0162 ₁₆			XX ₁₆
0163 ₁₆			XX ₁₆
0164 ₁₆	CAN0 local mask A register	COLMAR	XX ₁₆
0165 ₁₆			XX ₁₆
0166 ₁₆			XX ₁₆
0167 ₁₆			XX ₁₆
0168 ₁₆			XX ₁₆
0169 ₁₆			XX ₁₆
016A ₁₆	CAN0 local mask B register	COLMBR	XX ₁₆
016B ₁₆			XX ₁₆
016C ₁₆			XX ₁₆
016D ₁₆			XX ₁₆
016E ₁₆			XX ₁₆
016F ₁₆			XX ₁₆
0170 ₁₆			XX ₁₆
0171 ₁₆			XX ₁₆
0172 ₁₆			
0173 ₁₆			
0174 ₁₆			
0175 ₁₆			
0176 ₁₆			
0177 ₁₆			
0178 ₁₆			
0179 ₁₆			
017A ₁₆			
017B ₁₆			
017C ₁₆			
017D ₁₆			
017E ₁₆			
017F ₁₆			

X: Undefined

Note: The blank areas are reserved and cannot be accessed by users.

Figure 4.6 Location of Peripheral Function Control Registers and Value at After Reset (6)

Address	Register	Symbol	After reset
0180 ₁₆			
0181 ₁₆			
0182 ₁₆			
0183 ₁₆			
0184 ₁₆			
0185 ₁₆			
0186 ₁₆			
0187 ₁₆			
0188 ₁₆			
0189 ₁₆			
018A ₁₆			
018B ₁₆			
018C ₁₆			
018D ₁₆			
018E ₁₆			
018F ₁₆			
0190 ₁₆			
0191 ₁₆			
0192 ₁₆			
0193 ₁₆			
0194 ₁₆			
0195 ₁₆			
0196 ₁₆			
0197 ₁₆			
0198 ₁₆			
0199 ₁₆			
019A ₁₆			
019B ₁₆			
019C ₁₆			
019D ₁₆			
019E ₁₆			
019F ₁₆			
01A0 ₁₆			
01A1 ₁₆			
01A2 ₁₆			
01A3 ₁₆			
01A4 ₁₆			
01A5 ₁₆			
01A6 ₁₆			
01A7 ₁₆			
01A8 ₁₆			
01A9 ₁₆			
01AA ₁₆			
01AB ₁₆			
01AC ₁₆			
01AD ₁₆			
01AE ₁₆			
01AF ₁₆			
01B0 ₁₆			
01B1 ₁₆			
01B2 ₁₆			
01B3 ₁₆			
01B4 ₁₆			
01B5 ₁₆	Flash memory control register 1 (Note 1)	FMR1	0X00XX0X ₂
01B6 ₁₆			
01B7 ₁₆	Flash memory control register 0 (Note 1)	FMR0	XX000001 ₂
01B8 ₁₆			00 ₁₆
01B9 ₁₆	Address match interrupt register 2	RMAD2	00 ₁₆
01BA ₁₆			X0 ₁₆
01BB ₁₆	Address match interrupt enable register 2	AIER2	XXXXXX00 ₂
01BC ₁₆			00 ₁₆
01BD ₁₆	Address match interrupt register 3	RMAD3	00 ₁₆
01BE ₁₆			X0 ₁₆
01BF ₁₆			

X: Undefined

Note 1: This register is included in flash memory version.
 Note 2: The blank areas are reserved and cannot be accessed by users.

Figure 4.7 Location of Peripheral Function Control Registers and Value at After Reset (7)

Address	Register	Symbol	After reset
01C0 ₁₆	Timer B3,4,5 count start flag	TBSR	000XXXXX ₂
01C1 ₁₆			
01C2 ₁₆	Timer A1-1 register	TA11	XX ₁₆
01C3 ₁₆			XX ₁₆
01C4 ₁₆	Timer A2-1 register	TA21	XX ₁₆
01C5 ₁₆			XX ₁₆
01C6 ₁₆	Timer A4-1 register	TA41	XX ₁₆
01C7 ₁₆			XX ₁₆
01C8 ₁₆	Three-phase PWM control register 0	INVC0	00 ₁₆
01C9 ₁₆	Three-phase PWM control register 1	INVC1	00 ₁₆
01CA ₁₆	Three-phase output buffer register 0	IDB0	00 ₁₆
01CB ₁₆	Three-phase output buffer register 1	IDB1	00 ₁₆
01CC ₁₆	Dead time timer	DTT	XX ₁₆
01CD ₁₆	Timer B2 interrupt occurrence frequency set counter	ICTB2	XX ₁₆
01CE ₁₆			
01CF ₁₆			
01D0 ₁₆	Timer B3 register	TB3	XX ₁₆
01D1 ₁₆			XX ₁₆
01D2 ₁₆	Timer B4 register	TB4	XX ₁₆
01D3 ₁₆			XX ₁₆
01D4 ₁₆	Timer B5 register	TB5	XX ₁₆
01D5 ₁₆			XX ₁₆
01D6 ₁₆			
01D7 ₁₆			
01D8 ₁₆			
01D9 ₁₆			
01DA ₁₆			
01DB ₁₆	Timer B3 mode register	TB3MR	00XX0000 ₂
01DC ₁₆	Timer B4 mode register	TB4MR	00XX0000 ₂
01DD ₁₆	Timer B5 mode register	TB5MR	00XX0000 ₂
01DE ₁₆	Interrupt cause select register 0	IFSR0	00XX0000 ₂
01DF ₁₆	Interrupt cause select register 1	IFSR1	00 ₁₆
01E0 ₁₆	SI/O3 transmit/receive register	S3TRR	XX ₁₆
01E1 ₁₆			
01E2 ₁₆	SI/O3 control register	S3C	01000000 ₂
01E3 ₁₆	SI/O3 bit rate generator	S3BRG	XX ₁₆
01E4 ₁₆			
01E5 ₁₆			
01E6 ₁₆			
01E7 ₁₆			
01E8 ₁₆			
01E9 ₁₆			
01EA ₁₆			
01EB ₁₆			
01EC ₁₆	UART0 special mode register 4	U0SMR4	00 ₁₆
01ED ₁₆	UART0 special mode register 3	U0SMR3	000X0X0X ₂
01EE ₁₆	UART0 special mode register 2	U0SMR2	X0000000 ₂
01EF ₁₆	UART0 special mode register	U0SMR	X0000000 ₂
01F0 ₁₆	UART1 special mode register 4	U1SMR4	00 ₁₆
01F1 ₁₆	UART1 special mode register 3	U1SMR3	000X0X0X ₂
01F2 ₁₆	UART1 special mode register 2	U1SMR2	X0000000 ₂
01F3 ₁₆	UART1 special mode register	U1SMR	X0000000 ₂
01F4 ₁₆	UART2 special mode register 4	U2SMR4	00 ₁₆
01F5 ₁₆	UART2 special mode register 3	U2SMR3	000X0X0X ₂
01F6 ₁₆	UART2 special mode register 2	U2SMR2	X0000000 ₂
01F7 ₁₆	UART2 special mode register	U2SMR	X0000000 ₂
01F8 ₁₆	UART2 transmit/receive mode register	U2MR	00 ₁₆
01F9 ₁₆	UART2 bit rate generator	U2BRG	XX ₁₆
01FA ₁₆	UART2 transmit buffer register	U2TB	XX ₁₆
01FB ₁₆			XX ₁₆
01FC ₁₆	UART2 transmit/receive mode register 0	U2C0	00001000 ₂
01FD ₁₆	UART2 transmit/receive mode register 1	U2C1	00000010 ₂
01FE ₁₆	UART2 receive buffer register	U2RB	XX ₁₆
01FF ₁₆			XX ₁₆

X: Undefined

Note: The blank areas are reserved and cannot be accessed by users.

Figure 4.8 Location of Peripheral Function Control Registers and Value at After Reset (8)

Address	Register	Symbol	After reset
0200 ₁₆	CAN0 message control register 0	COMCTL0	00 ₁₆
0201 ₁₆	CAN0 message control register 1	COMCTL1	00 ₁₆
0202 ₁₆	CAN0 message control register 2	COMCTL2	00 ₁₆
0203 ₁₆	CAN0 message control register 3	COMCTL3	00 ₁₆
0204 ₁₆	CAN0 message control register 4	COMCTL4	00 ₁₆
0205 ₁₆	CAN0 message control register 5	COMCTL5	00 ₁₆
0206 ₁₆	CAN0 message control register 6	COMCTL6	00 ₁₆
0207 ₁₆	CAN0 message control register 7	COMCTL7	00 ₁₆
0208 ₁₆	CAN0 message control register 8	COMCTL8	00 ₁₆
0209 ₁₆	CAN0 message control register 9	COMCTL9	00 ₁₆
020A ₁₆	CAN0 message control register 10	COMCTL10	00 ₁₆
020B ₁₆	CAN0 message control register 11	COMCTL11	00 ₁₆
020C ₁₆	CAN0 message control register 12	COMCTL12	00 ₁₆
020D ₁₆	CAN0 message control register 13	COMCTL13	00 ₁₆
020E ₁₆	CAN0 message control register 14	COMCTL14	00 ₁₆
020F ₁₆	CAN0 message control register 15	COMCTL15	00 ₁₆
0210 ₁₆	CAN0 control register	C0CTLR	X0000001 ₂
0211 ₁₆			XX0X0000 ₂
0212 ₁₆	CAN0 status register	C0STR	00 ₁₆
0213 ₁₆			X0000001 ₂
0214 ₁₆	CAN0 slot status register	C0SSTR	00 ₁₆
0215 ₁₆			00 ₁₆
0216 ₁₆	CAN0 interrupt control register	C0ICR	00 ₁₆
0217 ₁₆			00 ₁₆
0218 ₁₆	CAN0 extended register	C0IDR	00 ₁₆
0219 ₁₆			00 ₁₆
021A ₁₆	CAN0 configuration register	C0CONR	XX ₁₆
021B ₁₆			XX ₁₆
021C ₁₆	CAN0 receive error count register	C0RECR	00 ₁₆
021D ₁₆	CAN0 transmit error count register	C0TECR	00 ₁₆
021E ₁₆	CAN0 time stamp register	C0TSR	00 ₁₆
021F ₁₆			00 ₁₆
0220 ₁₆	CAN1 message control register 0	C1MCTL0	00 ₁₆
0221 ₁₆	CAN1 message control register 1	C1MCTL1	00 ₁₆
0222 ₁₆	CAN1 message control register 2	C1MCTL2	00 ₁₆
0223 ₁₆	CAN1 message control register 3	C1MCTL3	00 ₁₆
0224 ₁₆	CAN1 message control register 4	C1MCTL4	00 ₁₆
0225 ₁₆	CAN1 message control register 5	C1MCTL5	00 ₁₆
0226 ₁₆	CAN1 message control register 6	C1MCTL6	00 ₁₆
0227 ₁₆	CAN1 message control register 7	C1MCTL7	00 ₁₆
0228 ₁₆	CAN1 message control register 8	C1MCTL8	00 ₁₆
0229 ₁₆	CAN1 message control register 9	C1MCTL9	00 ₁₆
022A ₁₆	CAN1 message control register 10	C1MCTL10	00 ₁₆
022B ₁₆	CAN1 message control register 11	C1MCTL11	00 ₁₆
022C ₁₆	CAN1 message control register 12	C1MCTL12	00 ₁₆
022D ₁₆	CAN1 message control register 13	C1MCTL13	00 ₁₆
022E ₁₆	CAN1 message control register 14	C1MCTL14	00 ₁₆
022F ₁₆	CAN1 message control register 15	C1MCTL15	00 ₁₆
0230 ₁₆	CAN1 control register	C1CTLR	X0000001 ₂
0231 ₁₆			XX0X0000 ₂
0232 ₁₆	CAN1 status register	C1STR	00 ₁₆
0233 ₁₆			X0000001 ₂
0234 ₁₆	CAN1 slot status register	C1SSTR	00 ₁₆
0235 ₁₆			00 ₁₆
0236 ₁₆	CAN1 interrupt control register	C1ICR	00 ₁₆
0237 ₁₆			00 ₁₆
0238 ₁₆	CAN1 extended register	C1IDR	00 ₁₆
0239 ₁₆			00 ₁₆
023A ₁₆	CAN1 configuration register	C1CONR	XX ₁₆
023B ₁₆			XX ₁₆
023C ₁₆	CAN1 receive error count register	C1RECR	00 ₁₆
023D ₁₆	CAN1 transmit error count register	C1TECR	00 ₁₆
023E ₁₆	CAN1 time stamp register	C1TSR	00 ₁₆
023F ₁₆			00 ₁₆

X: Undefined

Figure 4.9 Location of Peripheral Function Control Registers and Value at After Reset (9)

Address	Register	Symbol	After reset
0240 ₁₆			
0241 ₁₆			
0242 ₁₆	CAN0 acceptance filter support register	C0AFS	XX ₁₆
0243 ₁₆			XX ₁₆
0244 ₁₆	CAN1 acceptance filter support register	C1AFS	XX ₁₆
0245 ₁₆			XX ₁₆
0246 ₁₆			
0247 ₁₆			
0248 ₁₆			
0249 ₁₆			
024A ₁₆			
024B ₁₆			
024C ₁₆			
024D ₁₆			
024E ₁₆			
024F ₁₆			
0250 ₁₆			
0251 ₁₆			
0252 ₁₆			
0253 ₁₆			
0254 ₁₆			
0255 ₁₆			
0256 ₁₆			
0257 ₁₆			
0258 ₁₆			
0259 ₁₆			
025A ₁₆			
025B ₁₆			
025C ₁₆			
025D ₁₆			
025E ₁₆	Peripheral function clock select register	PCLKR	00 ₁₆
025F ₁₆	CAN0/1 clock select register	CCLKR	00 ₁₆
0260 ₁₆	CAN1 message box 0: Identifier / DLC		XX ₁₆
0261 ₁₆			XX ₁₆
0262 ₁₆			XX ₁₆
0263 ₁₆			XX ₁₆
0264 ₁₆			XX ₁₆
0265 ₁₆			XX ₁₆
0266 ₁₆	CAN1 message box 0: Data field		XX ₁₆
0267 ₁₆			XX ₁₆
0268 ₁₆			XX ₁₆
0269 ₁₆			XX ₁₆
026A ₁₆			XX ₁₆
026B ₁₆			XX ₁₆
026C ₁₆	CAN1 message box 0:Time stamp		XX ₁₆
026D ₁₆			XX ₁₆
026E ₁₆	CAN1 message box 1: Identifier / DLC		XX ₁₆
026F ₁₆			XX ₁₆
0270 ₁₆			XX ₁₆
0271 ₁₆			XX ₁₆
0272 ₁₆			XX ₁₆
0273 ₁₆			XX ₁₆
0274 ₁₆	CAN1 message box 1: Data field		XX ₁₆
0275 ₁₆			XX ₁₆
0276 ₁₆			XX ₁₆
0277 ₁₆			XX ₁₆
0278 ₁₆			XX ₁₆
0279 ₁₆			XX ₁₆
027A ₁₆	CAN1 message box 1:Time stamp		XX ₁₆
027B ₁₆			XX ₁₆
027C ₁₆			XX ₁₆
027D ₁₆			XX ₁₆
027E ₁₆			XX ₁₆
027F ₁₆			XX ₁₆

X: Undefined

Note: The blank areas are reserved and cannot be accessed by users.

Figure 4.10 Location of Peripheral Function Control Registers and Value at After Reset (10)

Address	Register	Symbol	After reset
0280 ₁₆	CAN1 message box 2: Identifier / DLC		XX ₁₆
0281 ₁₆			XX ₁₆
0282 ₁₆			XX ₁₆
0283 ₁₆			XX ₁₆
0284 ₁₆			XX ₁₆
0285 ₁₆			XX ₁₆
0286 ₁₆	CAN1 message box 2: Data field		XX ₁₆
0287 ₁₆			XX ₁₆
0288 ₁₆			XX ₁₆
0289 ₁₆			XX ₁₆
028A ₁₆			XX ₁₆
028B ₁₆			XX ₁₆
028C ₁₆	CAN1 message box 2: Time stamp		XX ₁₆
028D ₁₆			XX ₁₆
028E ₁₆	CAN1 message box 3: Identifier / DLC		XX ₁₆
028F ₁₆			XX ₁₆
0290 ₁₆			XX ₁₆
0291 ₁₆			XX ₁₆
0292 ₁₆			XX ₁₆
0293 ₁₆			XX ₁₆
0294 ₁₆	CAN1 message box 3: Data field		XX ₁₆
0295 ₁₆			XX ₁₆
0296 ₁₆			XX ₁₆
0297 ₁₆			XX ₁₆
0298 ₁₆			XX ₁₆
0299 ₁₆			XX ₁₆
029A ₁₆	CAN1 message box 3: Time stamp		XX ₁₆
029B ₁₆			XX ₁₆
029C ₁₆			XX ₁₆
029D ₁₆			XX ₁₆
029E ₁₆	CAN1 message box 4: Identifier / DLC		XX ₁₆
029F ₁₆			XX ₁₆
02A0 ₁₆			XX ₁₆
02A1 ₁₆			XX ₁₆
02A2 ₁₆			XX ₁₆
02A3 ₁₆			XX ₁₆
02A4 ₁₆	CAN1 message box 4: Data field		XX ₁₆
02A5 ₁₆			XX ₁₆
02A6 ₁₆			XX ₁₆
02A7 ₁₆			XX ₁₆
02A8 ₁₆			XX ₁₆
02A9 ₁₆			XX ₁₆
02AA ₁₆	CAN1 message box 4: Time stamp		XX ₁₆
02AB ₁₆			XX ₁₆
02AC ₁₆			XX ₁₆
02AD ₁₆			XX ₁₆
02AE ₁₆	CAN1 message box 5: Identifier / DLC		XX ₁₆
02AF ₁₆			XX ₁₆
02B0 ₁₆			XX ₁₆
02B1 ₁₆			XX ₁₆
02B2 ₁₆			XX ₁₆
02B3 ₁₆			XX ₁₆
02B4 ₁₆	CAN1 message box 5: Data field		XX ₁₆
02B5 ₁₆			XX ₁₆
02B6 ₁₆			XX ₁₆
02B7 ₁₆			XX ₁₆
02B8 ₁₆			XX ₁₆
02B9 ₁₆			XX ₁₆
02BA ₁₆	CAN1 message box 5: Time stamp		XX ₁₆
02BB ₁₆			XX ₁₆
02BC ₁₆			XX ₁₆
02BD ₁₆			XX ₁₆
02BE ₁₆			XX ₁₆
02BF ₁₆			XX ₁₆

X: Undefined

Figure 4.11 Location of Peripheral Function Control Registers and Value at After Reset (11)

Address	Register	Symbol	After reset
02C0 ₁₆	CAN1 message box 6: Identifier / DLC		XX ₁₆
02C1 ₁₆			XX ₁₆
02C2 ₁₆			XX ₁₆
02C3 ₁₆			XX ₁₆
02C4 ₁₆			XX ₁₆
02C5 ₁₆	CAN1 message box 6: Data field		XX ₁₆
02C6 ₁₆			XX ₁₆
02C7 ₁₆			XX ₁₆
02C8 ₁₆			XX ₁₆
02C9 ₁₆			XX ₁₆
02CA ₁₆	CAN1 message box 6: Time stamp		XX ₁₆
02CB ₁₆			XX ₁₆
02CC ₁₆			XX ₁₆
02CD ₁₆			XX ₁₆
02CE ₁₆			CAN1 message box 7: Identifier / DLC
02CF ₁₆	XX ₁₆		
02D0 ₁₆	XX ₁₆		
02D1 ₁₆	XX ₁₆		
02D2 ₁₆	XX ₁₆		
02D3 ₁₆	CAN1 message box 7: Data field		XX ₁₆
02D4 ₁₆			XX ₁₆
02D5 ₁₆			XX ₁₆
02D6 ₁₆			XX ₁₆
02D7 ₁₆			XX ₁₆
02D8 ₁₆	CAN1 message box 7: Time stamp		XX ₁₆
02D9 ₁₆			XX ₁₆
02DA ₁₆			XX ₁₆
02DB ₁₆			XX ₁₆
02DC ₁₆			CAN1 message box 8: Identifier / DLC
02DD ₁₆	XX ₁₆		
02DE ₁₆	XX ₁₆		
02DF ₁₆	XX ₁₆		
02E0 ₁₆	CAN1 message box 8: Data field		
02E1 ₁₆			XX ₁₆
02E2 ₁₆			XX ₁₆
02E3 ₁₆			XX ₁₆
02E4 ₁₆			XX ₁₆
02E5 ₁₆	CAN1 message box 8: Time stamp		XX ₁₆
02E6 ₁₆			XX ₁₆
02E7 ₁₆			XX ₁₆
02E8 ₁₆			XX ₁₆
02E9 ₁₆			CAN1 message box 9: Identifier / DLC
02EA ₁₆	XX ₁₆		
02EB ₁₆	XX ₁₆		
02EC ₁₆	XX ₁₆		
02ED ₁₆	XX ₁₆		
02EE ₁₆	CAN1 message box 9: Data field		XX ₁₆
02EF ₁₆			XX ₁₆
02F0 ₁₆			XX ₁₆
02F1 ₁₆			XX ₁₆
02F2 ₁₆			XX ₁₆
02F3 ₁₆	CAN1 message box 9: Time stamp		XX ₁₆
02F4 ₁₆			XX ₁₆
02F5 ₁₆			XX ₁₆
02F6 ₁₆			XX ₁₆
02F7 ₁₆			XX ₁₆
02F8 ₁₆			XX ₁₆
02F9 ₁₆			XX ₁₆
02FA ₁₆			XX ₁₆
02FB ₁₆			XX ₁₆
02FC ₁₆			XX ₁₆
02FD ₁₆			XX ₁₆
02FE ₁₆			XX ₁₆
02FF ₁₆			XX ₁₆

X: Undefined

Figure 4.12 Location of Peripheral Function Control Registers and Value at After Reset (12)

Address	Register	Symbol	After reset		
0300 ₁₆	CAN1 message box 10: Identifier / DLC		XX ₁₆		
0301 ₁₆			XX ₁₆		
0302 ₁₆			XX ₁₆		
0303 ₁₆			XX ₁₆		
0304 ₁₆			XX ₁₆		
0305 ₁₆	CAN1 message box 10: Data field		XX ₁₆		
0306 ₁₆			XX ₁₆		
0307 ₁₆			XX ₁₆		
0308 ₁₆			XX ₁₆		
0309 ₁₆			XX ₁₆		
030A ₁₆	CAN1 message box 10: Time stamp		XX ₁₆		
030B ₁₆			XX ₁₆		
030C ₁₆			XX ₁₆		
030D ₁₆			XX ₁₆		
030E ₁₆			CAN1 message box 11: Identifier / DLC		XX ₁₆
030F ₁₆	XX ₁₆				
0310 ₁₆	XX ₁₆				
0311 ₁₆	XX ₁₆				
0312 ₁₆	CAN1 message box 11: Data field				XX ₁₆
0313 ₁₆			XX ₁₆		
0314 ₁₆			XX ₁₆		
0315 ₁₆			XX ₁₆		
0316 ₁₆			CAN1 message box 11: Time stamp		XX ₁₆
0317 ₁₆	XX ₁₆				
0318 ₁₆	XX ₁₆				
0319 ₁₆	CAN1 message box 12: Identifier / DLC				XX ₁₆
031A ₁₆					XX ₁₆
031B ₁₆			XX ₁₆		
031C ₁₆			XX ₁₆		
031D ₁₆			XX ₁₆		
031E ₁₆	CAN1 message box 12: Data field		XX ₁₆		
031F ₁₆			XX ₁₆		
0320 ₁₆			XX ₁₆		
0321 ₁₆			XX ₁₆		
0322 ₁₆			CAN1 message box 12: Time stamp		XX ₁₆
0323 ₁₆	XX ₁₆				
0324 ₁₆	XX ₁₆				
0325 ₁₆	CAN1 message box 13: Identifier / DLC				XX ₁₆
0326 ₁₆					XX ₁₆
0327 ₁₆			XX ₁₆		
0328 ₁₆			XX ₁₆		
0329 ₁₆			CAN1 message box 13: Data field		XX ₁₆
032A ₁₆	XX ₁₆				
032B ₁₆	XX ₁₆				
032C ₁₆	XX ₁₆				
032D ₁₆	XX ₁₆				
032E ₁₆	CAN1 message box 13: Time stamp		XX ₁₆		
032F ₁₆			XX ₁₆		
0330 ₁₆			CAN1 message box 13: Identifier / DLC		XX ₁₆
0331 ₁₆					XX ₁₆
0332 ₁₆					XX ₁₆
0333 ₁₆	XX ₁₆				
0334 ₁₆	CAN1 message box 13: Data field				XX ₁₆
0335 ₁₆			XX ₁₆		
0336 ₁₆			XX ₁₆		
0337 ₁₆			XX ₁₆		
0338 ₁₆			XX ₁₆		
0339 ₁₆	CAN1 message box 13: Time stamp		XX ₁₆		
033A ₁₆			XX ₁₆		
033B ₁₆			XX ₁₆		
033C ₁₆			XX ₁₆		
033D ₁₆			XX ₁₆		
033E ₁₆	CAN1 message box 13: Time stamp		XX ₁₆		
033F ₁₆			XX ₁₆		

X: Undefined

Figure 4.13 Location of Peripheral Function Control Registers and Value at After Reset (13)

Address	Register	Symbol	After reset
0340 ₁₆	CAN1 message box 14: Identifier / DLC		XX ₁₆
0341 ₁₆			XX ₁₆
0342 ₁₆			XX ₁₆
0343 ₁₆			XX ₁₆
0344 ₁₆			XX ₁₆
0345 ₁₆			XX ₁₆
0346 ₁₆	CAN1 message box 14: Data field		XX ₁₆
0347 ₁₆			XX ₁₆
0348 ₁₆			XX ₁₆
0349 ₁₆			XX ₁₆
034A ₁₆			XX ₁₆
034B ₁₆			XX ₁₆
034C ₁₆	CAN1 message box 14: Time stamp		XX ₁₆
034D ₁₆			XX ₁₆
034E ₁₆	CAN1 message box 14: Time stamp		XX ₁₆
034F ₁₆			XX ₁₆
0350 ₁₆	CAN1 message box 15: Identifier / DLC		XX ₁₆
0351 ₁₆			XX ₁₆
0352 ₁₆			XX ₁₆
0353 ₁₆			XX ₁₆
0354 ₁₆			XX ₁₆
0355 ₁₆			XX ₁₆
0356 ₁₆	CAN1 message box 15: Data field		XX ₁₆
0357 ₁₆			XX ₁₆
0358 ₁₆			XX ₁₆
0359 ₁₆			XX ₁₆
035A ₁₆			XX ₁₆
035B ₁₆			XX ₁₆
035C ₁₆	CAN1 message box 15: Time stamp		XX ₁₆
035D ₁₆			XX ₁₆
035E ₁₆	CAN1 message box 15: Time stamp		XX ₁₆
035F ₁₆			XX ₁₆
0360 ₁₆	CAN1 global mask register	C1GMR	XX ₁₆
0361 ₁₆			XX ₁₆
0362 ₁₆			XX ₁₆
0363 ₁₆			XX ₁₆
0364 ₁₆			XX ₁₆
0365 ₁₆			XX ₁₆
0366 ₁₆	CAN1 local mask A register	C1LMAR	XX ₁₆
0367 ₁₆			XX ₁₆
0368 ₁₆			XX ₁₆
0369 ₁₆			XX ₁₆
036A ₁₆	CAN1 local mask B register	C1LMBR	XX ₁₆
036B ₁₆			XX ₁₆
036C ₁₆			XX ₁₆
036D ₁₆			XX ₁₆
036E ₁₆			XX ₁₆
036F ₁₆			XX ₁₆
0370 ₁₆	CAN1 local mask B register		XX ₁₆
0371 ₁₆			XX ₁₆
0372 ₁₆			
0373 ₁₆			
0374 ₁₆			
0375 ₁₆			
0376 ₁₆			
0377 ₁₆			
0378 ₁₆			
0379 ₁₆			
037A ₁₆			
037B ₁₆			
037C ₁₆			
037D ₁₆			
037E ₁₆			
037F ₁₆			

X: Undefined

Note: The blank areas are reserved and cannot be accessed by users.

Figure 4.14 Location of Peripheral Function Control Registers and Value at After Reset (14)

Address	Register	Symbol	After reset
0380 ₁₆	Count start flag	TABSR	00 ₁₆
0381 ₁₆	Clock prescaler reset flag	CPSRF	0XXXXXXX ₂
0382 ₁₆	One-shot start flag	ONSF	00 ₁₆
0383 ₁₆	Trigger select register	TRGSR	00 ₁₆
0384 ₁₆	Up-down flag	UDF	00 ₁₆
0385 ₁₆			
0386 ₁₆	Timer A0 register	TA0	XX ₁₆
0387 ₁₆			XX ₁₆
0388 ₁₆	Timer A1 register	TA1	XX ₁₆
0389 ₁₆			XX ₁₆
038A ₁₆	Timer A2 register	TA2	XX ₁₆
038B ₁₆			XX ₁₆
038C ₁₆	Timer A3 register	TA3	XX ₁₆
038D ₁₆			XX ₁₆
038E ₁₆	Timer A4 register	TA4	XX ₁₆
038F ₁₆			XX ₁₆
0390 ₁₆	Timer B0 register	TB0	XX ₁₆
0391 ₁₆			XX ₁₆
0392 ₁₆	Timer B1 register	TB1	XX ₁₆
0393 ₁₆			XX ₁₆
0394 ₁₆	Timer B2 register	TB2	XX ₁₆
0395 ₁₆			XX ₁₆
0396 ₁₆	Timer A0 mode register	TA0MR	00 ₁₆
0397 ₁₆	Timer A1 mode register	TA1MR	00 ₁₆
0398 ₁₆	Timer A2 mode register	TA2MR	00 ₁₆
0399 ₁₆	Timer A3 mode register	TA3MR	00 ₁₆
039A ₁₆	Timer A4 mode register	TA4MR	00 ₁₆
039B ₁₆	Timer B0 mode register	TB0MR	00XX0000 ₂
039C ₁₆	Timer B1 mode register	TB1MR	00XX0000 ₂
039D ₁₆	Timer B2 mode register	TB2MR	00XX0000 ₂
039E ₁₆	Timer B2 special mode register	TB2SC	XXXXXX00 ₂
039F ₁₆			
03A0 ₁₆	UART0 transmit/receive mode register	U0MR	00 ₁₆
03A1 ₁₆	UART0 bit rate generator	U0BRG	XX ₁₆
03A2 ₁₆	UART0 transmit buffer register	U0TB	XX ₁₆
03A3 ₁₆			XX ₁₆
03A4 ₁₆	UART0 transmit/receive control register 0	U0C0	00001000 ₂
03A5 ₁₆	UART0 transmit/receive control register 1	U0C1	00000010 ₂
03A6 ₁₆	UART0 receive buffer register	U0RB	XX ₁₆
03A7 ₁₆			XX ₁₆
03A8 ₁₆	UART1 transmit/receive mode register	U1MR	00 ₁₆
03A9 ₁₆	UART1 bit rate generator	U1BRG	XX ₁₆
03AA ₁₆	UART1 transmit buffer register	U1TB	XX ₁₆
03AB ₁₆			XX ₁₆
03AC ₁₆	UART1 transmit/receive control register 0	U1C0	00001000 ₂
03AD ₁₆	UART1 transmit/receive control register 1	U1C1	00000010 ₂
03AE ₁₆	UART1 receive buffer register	U1RB	XX ₁₆
03AF ₁₆			XX ₁₆
03B0 ₁₆	UART transmit/receive control register 2	UCON	X0000000 ₂
03B1 ₁₆			
03B2 ₁₆			
03B3 ₁₆			
03B4 ₁₆			
03B5 ₁₆			
03B6 ₁₆			
03B7 ₁₆			
03B8 ₁₆	DMA0 request cause select register	DM0SL	00 ₁₆
03B9 ₁₆			
03BA ₁₆	DMA1 request cause select register	DM1SL	00 ₁₆
03BB ₁₆			
03BC ₁₆	CRC data register	CRCD	XX ₁₆
03BD ₁₆			XX ₁₆
03BE ₁₆	CRC input register	CRCIN	XX ₁₆
03BF ₁₆			

X: Undefined

Note: The blank areas are reserved and cannot be accessed by users.

Figure 4.15 Location of Peripheral Function Control Registers and Value at After Reset (15)

Address	Register	Symbol	After reset
03C0 ₁₆	A-D register 0	AD0	XX ₁₆
03C1 ₁₆			XX ₁₆
03C2 ₁₆	A-D register 1	AD1	XX ₁₆
03C3 ₁₆			XX ₁₆
03C4 ₁₆	A-D register 2	AD2	XX ₁₆
03C5 ₁₆			XX ₁₆
03C6 ₁₆	A-D register 3	AD3	XX ₁₆
03C7 ₁₆			XX ₁₆
03C8 ₁₆	A-D register 4	AD4	XX ₁₆
03C9 ₁₆			XX ₁₆
03CA ₁₆	A-D register 5	AD5	XX ₁₆
03CB ₁₆			XX ₁₆
03CC ₁₆	A-D register 6	AD6	XX ₁₆
03CD ₁₆			XX ₁₆
03CE ₁₆	A-D register 7	AD7	XX ₁₆
03CF ₁₆			XX ₁₆
03D0 ₁₆			
03D1 ₁₆			
03D2 ₁₆			
03D3 ₁₆			
03D4 ₁₆	A-D control register 2	ADCON2	00 ₁₆
03D5 ₁₆			
03D6 ₁₆	A-D control register 0	ADCON0	00000XXX ₂
03D7 ₁₆	A-D control register 1	ADCON1	00 ₁₆
03D8 ₁₆	D-A register 0	DA0	XX ₁₆
03D9 ₁₆			
03DA ₁₆	D-A register 1	DA1	XX ₁₆
03DB ₁₆			
03DC ₁₆	D-A control register	DACON	00 ₁₆
03DD ₁₆			
03DE ₁₆			
03DF ₁₆			
03E0 ₁₆	Port P0 register	P0	XX ₁₆
03E1 ₁₆	Port P1 register	P1	XX ₁₆
03E2 ₁₆	Port P0 direction register	PD0	00 ₁₆
03E3 ₁₆	Port P1 direction register	PD1	00 ₁₆
03E4 ₁₆	Port P2 register	P2	XX ₁₆
03E5 ₁₆	Port P3 register	P3	XX ₁₆
03E6 ₁₆	Port P2 direction register	PD2	00 ₁₆
03E7 ₁₆	Port P3 direction register	PD3	00 ₁₆
03E8 ₁₆	Port P4 register	P4	XX ₁₆
03E9 ₁₆	Port P5 register	P5	XX ₁₆
03EA ₁₆	Port P4 direction register	PD4	00 ₁₆
03EB ₁₆	Port P5 direction register	PD5	00 ₁₆
03EC ₁₆	Port P6 register	P6	XX ₁₆
03ED ₁₆	Port P7 register	P7	XX ₁₆
03EE ₁₆	Port P6 direction register	PD6	00 ₁₆
03EF ₁₆	Port P7 direction register	PD7	00 ₁₆
03F0 ₁₆	Port P8 register	P8	XX ₁₆
03F1 ₁₆	Port P9 register	P9	XX ₁₆
03F2 ₁₆	Port P8 direction register	PD8	00X00000 ₂
03F3 ₁₆	Port P9 direction register	PD9	00 ₁₆
03F4 ₁₆	Port P10 register	P10	XX ₁₆
03F5 ₁₆			
03F6 ₁₆	Port P10 direction register	PD10	00 ₁₆
03F7 ₁₆			
03F8 ₁₆			
03F9 ₁₆			
03FA ₁₆			
03FB ₁₆			
03FC ₁₆	Pull-up control register 0	PUR0	00 ₁₆
03FD ₁₆	Pull-up control register 1	PUR1	00000000 ₂ (Note 1) 00000010 ₂
03FE ₁₆	Pull-up control register 2	PUR2	00 ₁₆
03FF ₁₆	Port control register	PCR	00 ₁₆

X: Undefined

Note 1: At hardware reset, the register is as follows:
 • "00000000₂" where "L" is input to the CNVss pin
 • "00000010₂" where "H" is input to the CNVss pin
 At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:
 • "00000000₂" where the PM01 to PM00 bits in the PM0 register are "00₂" (single-chip mode)
 • "00000010₂" where the PM01 to PM00 bits in the PM0 register are "01₂" (memory expansion mode) or "11₂" (microprocessor mode)

Note 2: The blank areas are reserved and cannot be accessed by users.

Figure 4.16 Location of Peripheral Function Control Registers and Value at After Reset (16)

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated value	Unit
V _{CC1}	Supply voltage		V _{CC1} =AV _{CC}	-0.3 to 6.5	V
V _{CC2}	Supply voltage		V _{CC2}	-0.3 < V _{CC2} = V _{CC1}	V
AV _{CC}	Analog supply voltage		V _{CC1} =AV _{CC}	-0.3 to 6.5	V
V _i	Input voltage	RESET, CNV _{SS} , BYTE, P6 ₀ ~P6 ₇ , P7 ₀ , P7 ₂ ~P7 ₇ , P8 ₀ ~P8 ₇ , P9 ₀ , P9 ₂ ~P9 ₇ , P10 ₀ ~P10 ₇ , V _{REF} , X _{IN}		-0.3 to V _{CC1} +0.3	V
		P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇		-0.3 to V _{CC2} +0.3	V
		P7 ₁ , P9 ₁		-0.3 to 6.5	V
V _o	Output voltage	P6 ₀ ~P6 ₇ , P7 ₀ , P7 ₂ ~P7 ₇ , P8 ₀ ~P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ , P9 ₂ ~P9 ₇ , P10 ₀ ~P10 ₇ , X _{OUT}		-0.3 to V _{CC1} +0.3	V
		P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇		-0.3 to V _{CC2} +0.3	V
		P7 ₁ , P9 ₁		-0.3 to 6.5	V
P _d	Power dissipation		T _{opr} =25°C	700	mW
T _{opr}	Operating ambient temperature			-40 to 85/-40 to 125 (option)	°C
T _{stg}	Storage temperature			-65 to 150	°C

option: If you desire this option, please so specify.

Table 5.2 Recommended Operating Conditions (Note 1)

Symbol	Parameter		Standard			Unit	
			Min.	Typ.	Max.		
V _{CC1} , V _{CC2}	Supply voltage (V _{CC1} =V _{CC2})		4.2	5.0	5.5	V	
AV _{CC}	Analog supply voltage			V _{CC}		V	
V _{SS}	Supply voltage			0		V	
AV _{SS}	Analog supply voltage			0		V	
V _{IH}	HIGH input voltage	P3 ₁ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ , P7 ₂ ~P7 ₇ , P8 ₀ ~P8 ₇ , P9 ₀ , P9 ₂ ~P9 ₇ , P10 ₀ ~P10 ₇ , X _{IN} , RESET, CNV _{SS} , BYTE	0.8V _{CC}		V _{CC}	V	
		P7 ₁ , P9 ₁	0.8V _{CC}		6.5	V	
		P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ (During single-chip mode)	0.8V _{CC}		V _{CC}	V	
		P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ (Data input during memory expansion and microprocessor modes)	0.5V _{CC}		V _{CC}	V	
V _{IL}	LOW input voltage	P3 ₁ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇ , P9 ₀ ~P9 ₇ , P10 ₀ ~P10 ₇ , X _{IN} , RESET, CNV _{SS} , BYTE	0		0.2V _{CC}	V	
		P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ (During single-chip mode)	0		0.2V _{CC}	V	
		P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ (Data input during memory expansion and microprocessor modes)	0		0.16V _{CC}	V	
I _{OH} (peak)	HIGH peak output current	P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ , P7 ₂ ~P7 ₇ , P8 ₀ ~P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ , P9 ₂ ~P9 ₇ , P10 ₀ ~P10 ₇			-10.0	mA	
I _{OH} (avg)	HIGH average output current	P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ , P7 ₂ ~P7 ₇ , P8 ₀ ~P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ , P9 ₂ ~P9 ₇ , P10 ₀ ~P10 ₇			-5.0	mA	
I _{OL} (peak)	LOW peak output current	P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ ~P9 ₇ , P10 ₀ ~P10 ₇			10.0	mA	
I _{OL} (avg)	LOW average output current	P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ ~P9 ₇ , P10 ₀ ~P10 ₇			5.0	mA	
f(X _{IN})	Main clock input oscillation frequency (Notes 4, 5 and 6)	No wait Mask ROM version Flash memory version	V _{CC} =4.2 to 5.5V		0	16	MHz
f(X _{CIN})	Sub clock oscillation frequency			32.768	50	kHz	
f(Ring)	Ring oscillation frequency			1		MHz	
f(PLL)	PLL clock oscillation frequency				20	MHz	
f(BCLK)	CPU operation clock		V _{CC} =4.2 to 5.5V		0	20	MHz
t _{su} (PLL)	PLL frequency synthesizer stabilization wait time				20	ms	

Note 1: Referenced to V_{CC} = 4.2 to 5.5 V at Topr = -40 to 85 °C unless otherwise specified.

Note 2: The mean output current is the mean value within 100 ms.

Note 3: The total I_{OL} (peak) for ports P0, P1, P2, P8₆, P8₇, P9 and P10 must be 80mA max. The total I_{OL} (peak) for ports P3, P4, P5, P6, P7 and P8₀ to P8₄ must be 80mA max. The total I_{OH} (peak) for ports P0, P1, and P2 must be -40mA max. The total I_{OH} (peak) for ports P3, P4 and P5 must be -40mA max. The total I_{OH} (peak) for ports P6, P7 and P8₀ to P8₄ must be -40mA max. The total I_{OH} (peak) for ports P8₆, P8₇, P9 and P10 must be -40mA max.

Note 4: Relationship between main clock oscillation frequency and supply voltage is shown right.

Note 5: Execute program /erase of flash memory by V_{CC} = 5.0 ± 0.5 V.

Note 6: When using 16 MHz or more, use PLL clock.

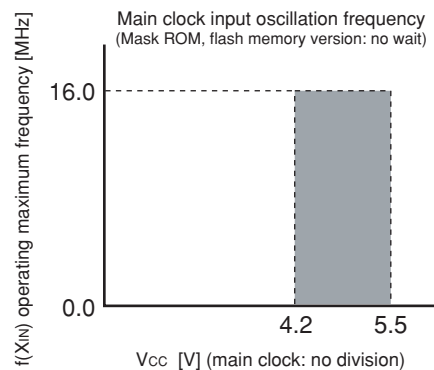


Table 5.3 Electrical Characteristics (Note 1)

Symbol	Parameter		Measuring condition	Standard			Unit	
				Min.	Typ.	Max.		
V _{OH}	HIGH output voltage	P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ , P7 ₂ ~P7 ₇ , P8 ₀ ~P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ , P9 ₂ ~P9 ₇ , P10 ₀ ~P10 ₇	I _{OH} =-5mA	V _{CC} -2.0		V _{CC}	V	
V _{OH}	HIGH output voltage	P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ , P7 ₂ ~P7 ₇ , P8 ₀ ~P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ , P9 ₂ ~P9 ₇ , P10 ₀ ~P10 ₇	I _{OH} =-200μA	V _{CC} -0.3		V _{CC}	V	
V _{OH}	HIGH output voltage	X _{OUT}	HIGHPOWER	I _{OH} =-1mA	3.0		V _{CC}	V
			LOWPOWER	I _{OH} =-0.5mA	3.0		V _{CC}	
	HIGH output voltage	X _{COUT}	HIGHPOWER	With no load applied		2.5		V
			LOWPOWER	With no load applied		1.6		
V _{OL}	LOW output voltage	P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ ~P9 ₇ , P10 ₀ ~P10 ₇	I _{OL} =5mA			2.0	V	
V _{OL}	LOW output voltage	P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ ~P9 ₇ , P10 ₀ ~P10 ₇	I _{OL} =200μA			0.45	V	
V _{OL}	LOW output voltage	X _{OUT}	HIGHPOWER	I _{OL} =1mA			2.0	V
			LOWPOWER	I _{OL} =0.5mA			2.0	
	LOW output voltage	X _{COUT}	HIGHPOWER	With no load applied		0		V
			LOWPOWER	With no load applied		0		
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0 _{IN} ~TA4 _{IN} , TB0 _{IN} ~TB5 _{IN} , INT0~INT5, NMI, AD _{TRG} , CTS0~CTS2, SCL, SDA, CLK0~CLK4, TA2 _{OUT} ~TA4 _{OUT} , Kl0~Kl3, RxDo~RxD2, S _{IN3}		0.2		1.0	V	
V _{T+} -V _{T-}	Hysteresis	RESET		0.2		2.2	V	
I _{IH}	HIGH input current	P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇ , P9 ₀ ~P9 ₇ , P10 ₀ ~P10 ₇ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =5V			5.0	μA	
I _{IL}	LOW input current	P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇ , P9 ₀ ~P9 ₇ , P10 ₀ ~P10 ₇ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =0V			-5.0	μA	
R _{PULLUP}	Pull-up resistance	P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ , P7 ₂ ~P7 ₇ , P8 ₀ ~P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ , P9 ₂ ~P9 ₇ , P10 ₀ ~P10 ₇	V _I =0V	30	50	170	kΩ	
R _{FIXIN}	Feedback resistance	X _{IN}			1.5		MΩ	
R _{IXCIN}	Feedback resistance	X _{CIN}			15		MΩ	
V _{RAM}	RAM retention voltage		At stop mode	2.0			V	
I _{CC}	Power supply current (V _{CC} = 4.2 to 5.5V)	In single-chip mode, the output pins are open and other pins are V _{SS} .	Mask ROM	f(BCLK)=20MHz, No division, PLL operation	18	32	mA	
				No division, Ring oscillation	1		mA	
			Flash memory	f(BCLK)=20MHz, No division, PLL operation	20	34	mA	
				No division, Ring oscillation	1.8		mA	
			Flash memory Program	f(BCLK)=10MHz, V _{CC} =5V	15		mA	
			Flash memory Erase	f(BCLK)=10MHz, V _{CC} =5V	25		mA	
			Mask ROM	f(X _{CIN})=32kHz, Low power dissipation mode, ROM (Note 2)	25		μA	
			Flash memory	f(BCLK)=32kHz, Low power dissipation mode, RAM (Note 2)	25		μA	
				f(BCLK)=32kHz, Low power dissipation mode, Flash memory (Note 2)	420		μA	
				Mask ROM	Ring oscillation, Wait mode	50		μA
			Flash memory	f(BCLK)=32kHz, Wait mode (Note 3), Oscillation capacity High	8.5		μA	
				f(BCLK)=32kHz, Wait mode (Note 3), Oscillation capacity Low	3.0		μA	
Stop mode, T _{opr} = 25 °C	0.8	3.0		μA				

Note 1: Referenced to V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V at Topr = -40 to 85 °C, f(BCLK) = 20 MHz unless otherwise specified.

Note 2: This indicates the memory in which the program to be executed exists.

Note 3: With one timer operated using fc32.

Table 5.4 A-D Conversion Characteristics (Note 1)

Symbol	Parameter		Measuring condition	Standard			Unit	
				Min.	Typ.	Max.		
–	Resolution		$V_{REF}=V_{CC}$			10	Bits	
INL	Integral non-linearity error	10 bits	$V_{REF}=V_{CC}=5V$	ANEX0, ANEX1 input, AN ₀ to AN ₇ input, AN ₀₀ to AN ₀₇ input, AN ₂₀ to AN ₂₇ input			±3	LSB
				External operation amp connection mode			±7	LSB
		8 bits	$V_{REF}=AV_{CC}=V_{CC}=5V$				±2	LSB
–	Absolute accuracy	10 bits	$V_{REF}=V_{CC}=5V$	ANEX0, ANEX1 input, AN ₀ to AN ₇ input, AN ₀₀ to AN ₀₇ input, AN ₂₀ to AN ₂₇ input			±3	LSB
				External operation amp connection mode			±7	LSB
		8 bits	$V_{REF}=AV_{CC}=V_{CC}=5V$				±2	LSB
DNL	Differential non-linearity error						±1	LSB
–	Offset error						±3	LSB
–	Gain error						±3	LSB
R _{LADDER}	Ladder resistance		$V_{REF}=V_{CC}$	10		40	kΩ	
t _{CONV}	Conversion time (10 bits), Sample & hold function available		$V_{REF}=V_{CC}=5V, \phi_{AD}=10MHz$	3.3			μs	
	Conversion time (8 bits), Sample & hold function available		$V_{REF}=V_{CC}=5V, \phi_{AD}=10MHz$	2.8			μs	
t _{SAMP}	Sampling time			0.3			μs	
V _{REF}	Reference voltage			2.0		V _{CC}	V	
V _{IA}	Analog input voltage			0		V _{REF}	V	

Note 1: Referenced to $V_{CC} = AV_{CC} = V_{REF} = 4.2$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V, -40 to 85 °C unless otherwise specified.

Note 2: AD operation clock frequency (ϕ_{AD} frequency) must be 10 MHz or less.

Note 3: A case without sample & hold function turn ϕ_{AD} frequency into 250 kHz or more in addition to a limit of Note 2.

A case with sample & hold function turn ϕ_{AD} frequency into 1 MHz or more in addition to a limit of Note 2.

Table 5.5 D-A conversion Characteristics (Note 1)

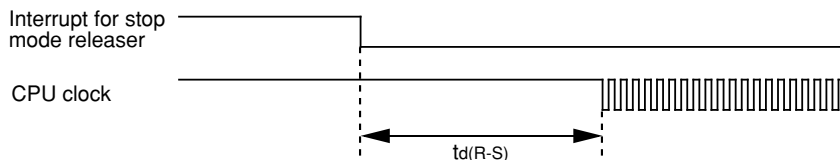
Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
t _{SU}	Setup time				3	μs
R _O	Output resistance		4	10	20	kΩ
I _{VREF}	Reference power supply input current	(Note 2)			1.5	mA

Note 1: Referenced to $V_{CC} = AV_{CC} = V_{REF} = 4.2$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V, -40 to 85 °C unless otherwise specified.

Note 2: This applies when using one D-A converter, with the DAi register (i = 0, 1) for the unused D-A converter set to "00₁₆". The A-D converter's ladder resistance is not included. Also, the current I_{VREF} always flows even though V_{REF} may have been set to be unconnected by the ADCON1 register.

Table 5.6 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
t _{d(P-R)}	Time for internal power supply stabilization during powering-on	$V_{CC} = 4.2$ to 5.5 V			2	ms
t _{d(R-S)}	STOP release time				150	μs
t _{d(W-S)}	Low power dissipation mode wait mode release time				150	μs
t _{d(M-L)}	Time for internal power supply stabilization when main clock oscillation status				50	μs



Timing Requirements(Referenced to $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{op} = -40$ to $85\text{ }^{\circ}\text{C}$ unless otherwise specified)**Table 5.7 External Clock Input (X_{IN} Input)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	62.5		ns
$t_{w(H)}$	External clock input HIGH pulse width	25		ns
$t_{w(L)}$	External clock input LOW pulse width	25		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

Table 5.8 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data input access time (for setting with wait)		(Note 2)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplexed bus area)		(Note 3)	ns
$t_{su(DB-RD)}$	Data input setup time	40		ns
$t_{su(RDY-BCLK)}$	RDY input setup time	30		ns
$t_{su(HOLD-BCLK)}$	HOLD input setup time	40		ns
$t_h(RD-DB)$	Data input hold time	0		ns
$t_h(BCLK-RDY)$	RDY input hold time	0		ns
$t_h(BCLK-HOLD)$	HOLD input hold time	0		ns
$t_d(BCLK-HLDA)$	HLDA output delay time		40	ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 45 \text{ [ns]}$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 45 \text{ [ns]} \quad n \text{ is "2" for 1-wait setting, "3" for 2-wait setting and "4" for 3-wait setting.}$$

Note 3: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 45 \text{ [ns]} \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

Timing Requirements(Referenced to $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{op} = -40$ to $85\text{ }^{\circ}\text{C}$ unless otherwise specified)**Table 5.9 Timer A Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TA _{IIN} input cycle time	100		ns
$t_{w(TAH)}$	TA _{IIN} input HIGH pulse width	40		ns
$t_{w(TAL)}$	TA _{IIN} input LOW pulse width	40		ns

Table 5.10 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TA _{IIN} input cycle time	400		ns
$t_{w(TAH)}$	TA _{IIN} input HIGH pulse width	200		ns
$t_{w(TAL)}$	TA _{IIN} input LOW pulse width	200		ns

Table 5.11 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TA _{IIN} input cycle time	200		ns
$t_{w(TAH)}$	TA _{IIN} input HIGH pulse width	100		ns
$t_{w(TAL)}$	TA _{IIN} input LOW pulse width	100		ns

Table 5.12 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TA _{IIN} input HIGH pulse width	100		ns
$t_{w(TAL)}$	TA _{IIN} input LOW pulse width	100		ns

Table 5.13 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TA _{IOUT} input cycle time	2000		ns
$t_{w(UPH)}$	TA _{IOUT} input HIGH pulse width	1000		ns
$t_{w(UPL)}$	TA _{IOUT} input LOW pulse width	1000		ns
$t_{su(UP-TIN)}$	TA _{IOUT} input setup time	400		ns
$t_{h(TIN-UP)}$	TA _{IOUT} input hold time	400		ns

Table 5.14 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TA _{IIN} input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TA _{IOUT} input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TA _{IIN} input setup time	200		ns

Timing Requirements(Referenced to $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{op} = -40$ to $85\text{ }^{\circ}\text{C}$ unless otherwise specified)**Table 5.15 Timer B Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	80		ns

Table 5.16 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 5.17 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 5.18 A-D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	AD _{TRG} input cycle time (trigger able minimum)	1000		ns
$t_{w(ADL)}$	AD _{TRG} input LOW pulse width	125		ns

Table 5.19 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK _i input cycle time	200		ns
$t_{w(CKH)}$	CLK _i input HIGH pulse width	100		ns
$t_{w(CKL)}$	CLK _i input LOW pulse width	100		ns
$t_{d(C-Q)}$	TxD _i output delay time		80	ns
$t_{h(C-Q)}$	TxD _i hold time	0		ns
$t_{su(D-C)}$	RxD _i input setup time	30		ns
$t_{h(C-D)}$	RxD _i input hold time	90		ns

Table 5.20 External Interrupt INT_i Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	INT _i input HIGH pulse width	250		ns
$t_{w(INL)}$	INT _i input LOW pulse width	250		ns

Switching Characteristics

(Referenced to $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{op} = -40\text{ to }85\text{ }^\circ\text{C}$ unless otherwise specified)

Table 5.21 Memory Expansion Mode and Microprocessor Mode (for setting with no wait)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 5.1		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK) (Note 3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR) (Note 3)		(Note 1)		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]} \quad f(\text{BCLK}) \text{ is } 12.5 \text{ MHz or less.}$$

Note 3: This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR \times \ln(1 - V_{OL} / V_{CC})$$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2 V_{CC}$, $C = 30\text{ pF}$,

$R = 1\text{ k}\Omega$, hold time of output "L" level is

$$t = -30\text{ pF} \times 1\text{ k}\Omega \times \ln(1 - 0.2 V_{CC} / V_{CC}) = 6.7\text{ ns.}$$

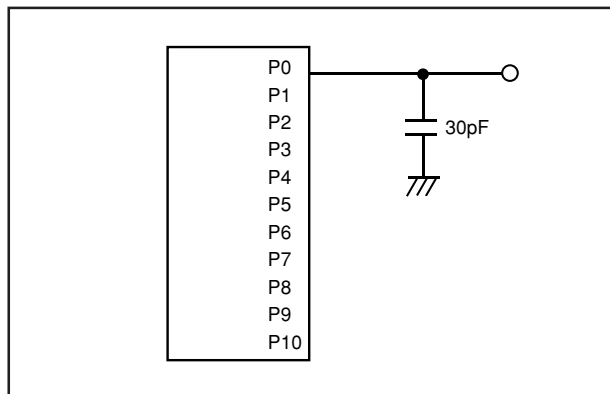
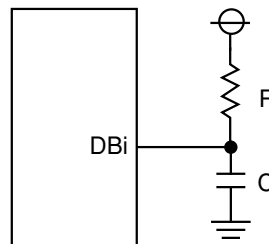


Figure 5.1 Port P0 to P10 Measurement Circuit

Switching Characteristics

(Referenced to $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{op} = -40\text{ to }85\text{ }^\circ\text{C}$ unless otherwise specified)

Table 5.22 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 5.1		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK) (Note 3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR) (Note 3)		(Note 1)		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]}$$

n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting.
When n = 1, f(BCLK) is 12.5 MHz or less.

Note 3: This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

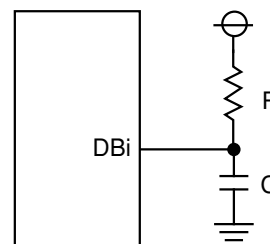
$$t = -CR \times \ln(1 - V_{OL} / V_{CC})$$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2 V_{CC}$, $C = 30\text{ pF}$,

$R = 1\text{ k}\Omega$, hold time of output "L" level is

$$t = -30\text{ pF} \times 1\text{ k}\Omega \times \ln(1 - 0.2 V_{CC} / V_{CC}) = 6.7\text{ ns.}$$



Switching Characteristics(Referenced to $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, at $T_{op} = -40$ to $85\text{ }^{\circ}\text{C}$ unless otherwise specified)**Table 5.23 Memory Expansion Mode and Microprocessor Mode
(for 2- to 3-wait setting, external area access and multiplexed bus selection)**

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 5.1		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{h(RD-CS)}$	Chip select output hold time (refers to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (refers to BCLK)			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (refers to BCLK)		-4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (refers to Address)		(Note 3)		ns
$t_{h(ALE-AD)}$	ALE signal output hold time (refers to Address)		(Note 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of Address	0		ns	
$t_{d(AD-WR)}$	WR signal output delay from the end of Address	0		ns	
$t_{dZ(RD-AD)}$	Address output floating start time		8	ns	

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]} \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

Note 3: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 25 \text{ [ns]}$$

Note 4: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 15 \text{ [ns]}$$

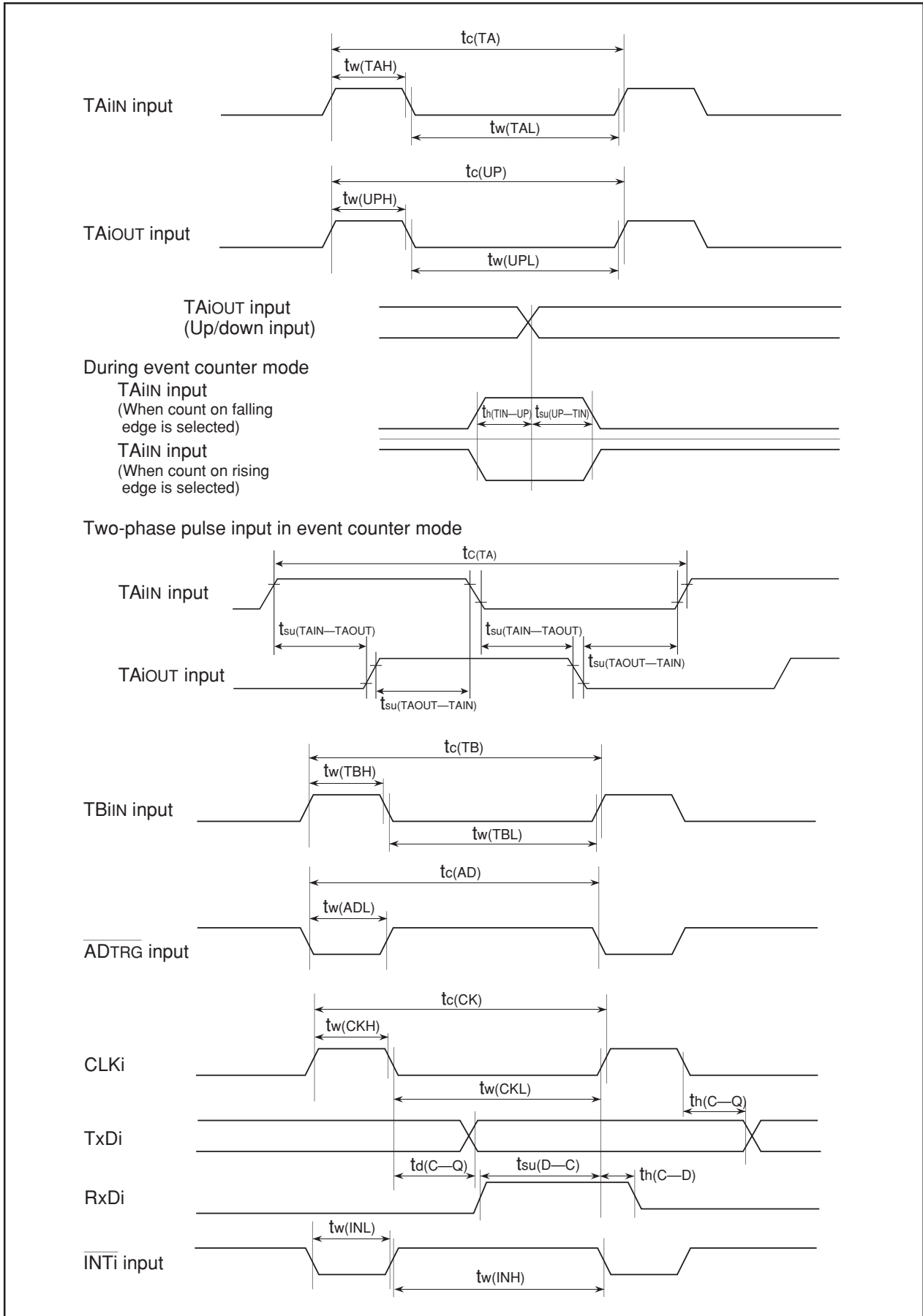
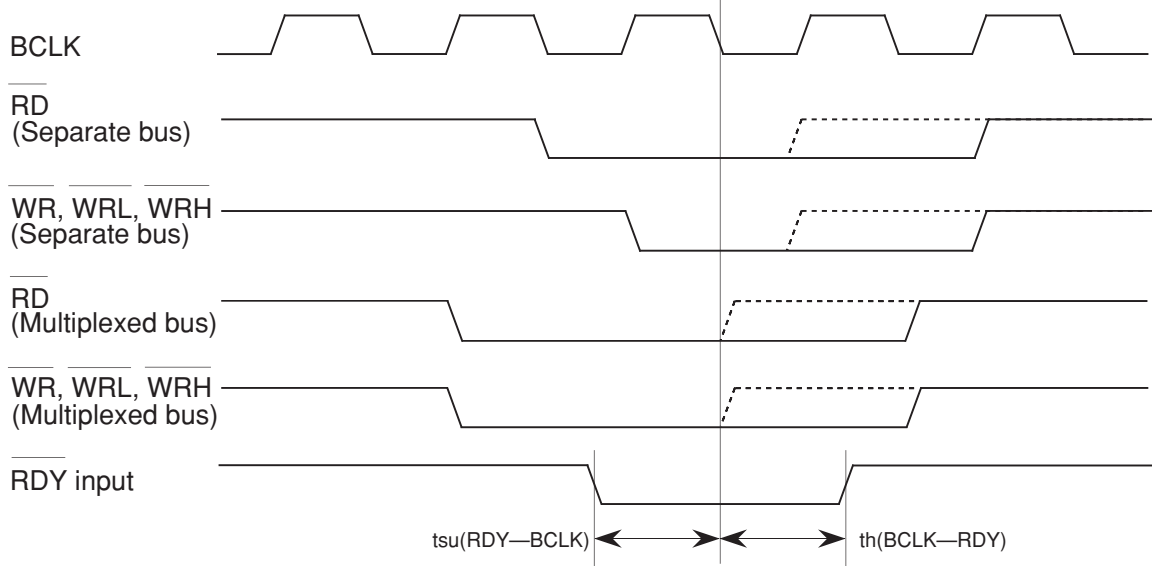


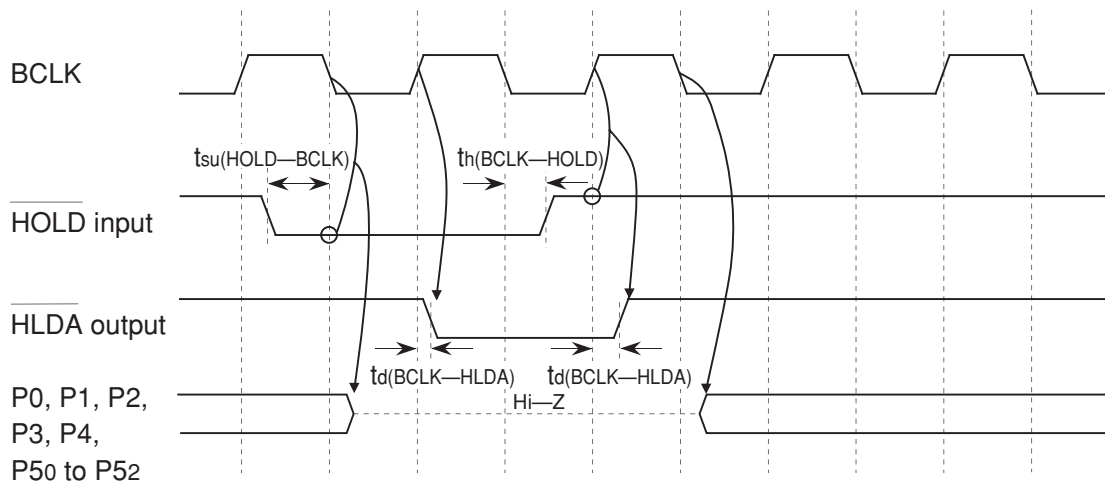
Figure 5.2 Timing Diagram (1)

Memory Expansion Mode and Microprocessor Mode

(Effective for setting with wait)



(Common to setting with wait and setting without wait)



Note: The above pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit of PM0 register and PM11 bit of PM1 register.

Measuring conditions :

- $V_{CC} = 5\text{ V}$
- Input timing voltage : Determined with $V_{IL} = 1.0\text{ V}$, $V_{IH} = 4.0\text{ V}$
- Output timing voltage: Determined with $V_{OL} = 2.5\text{ V}$, $V_{OH} = 2.5\text{ V}$

Figure 5.3 Timing Diagram (2)

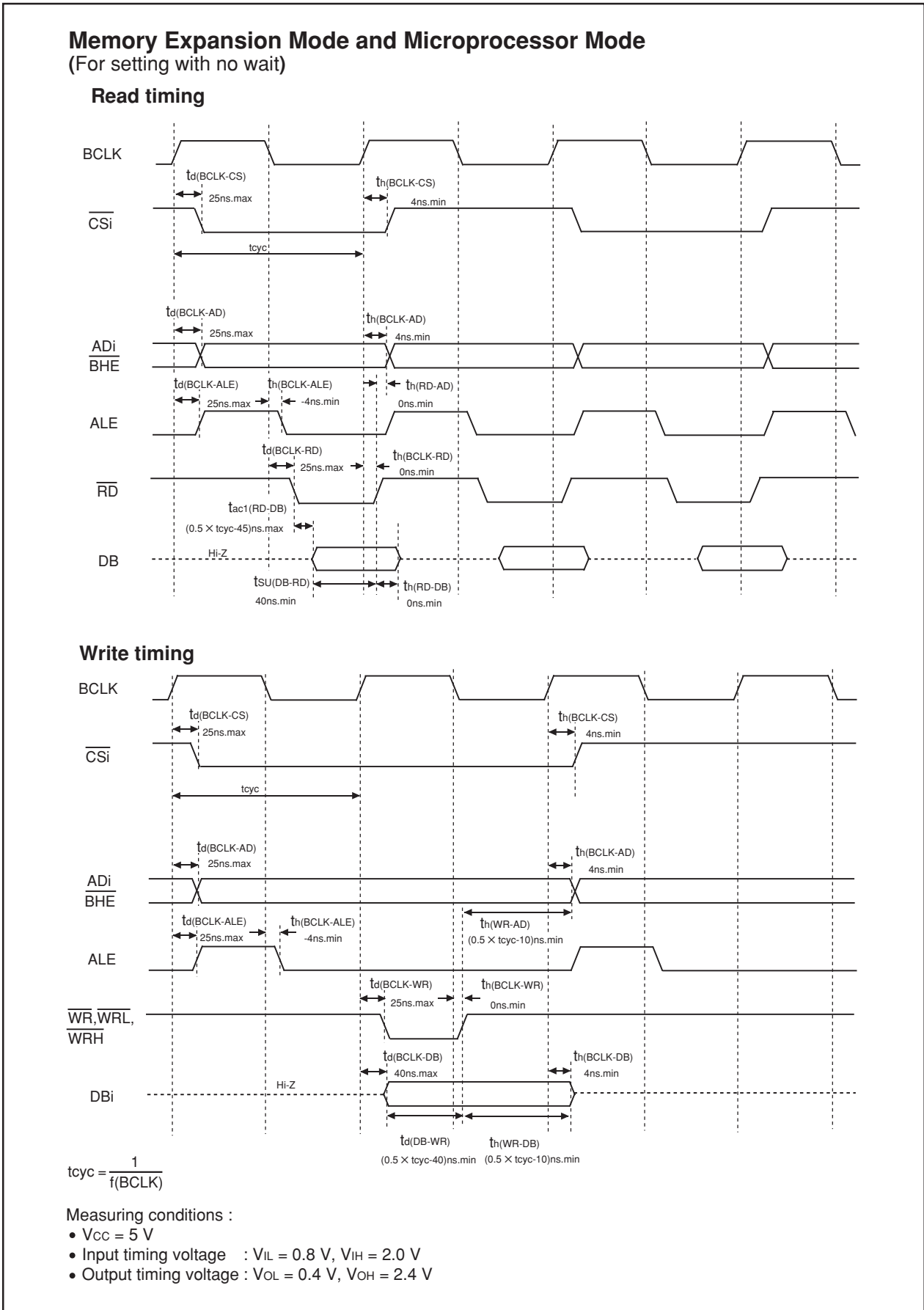


Figure 5.4 Timing Diagram (3)

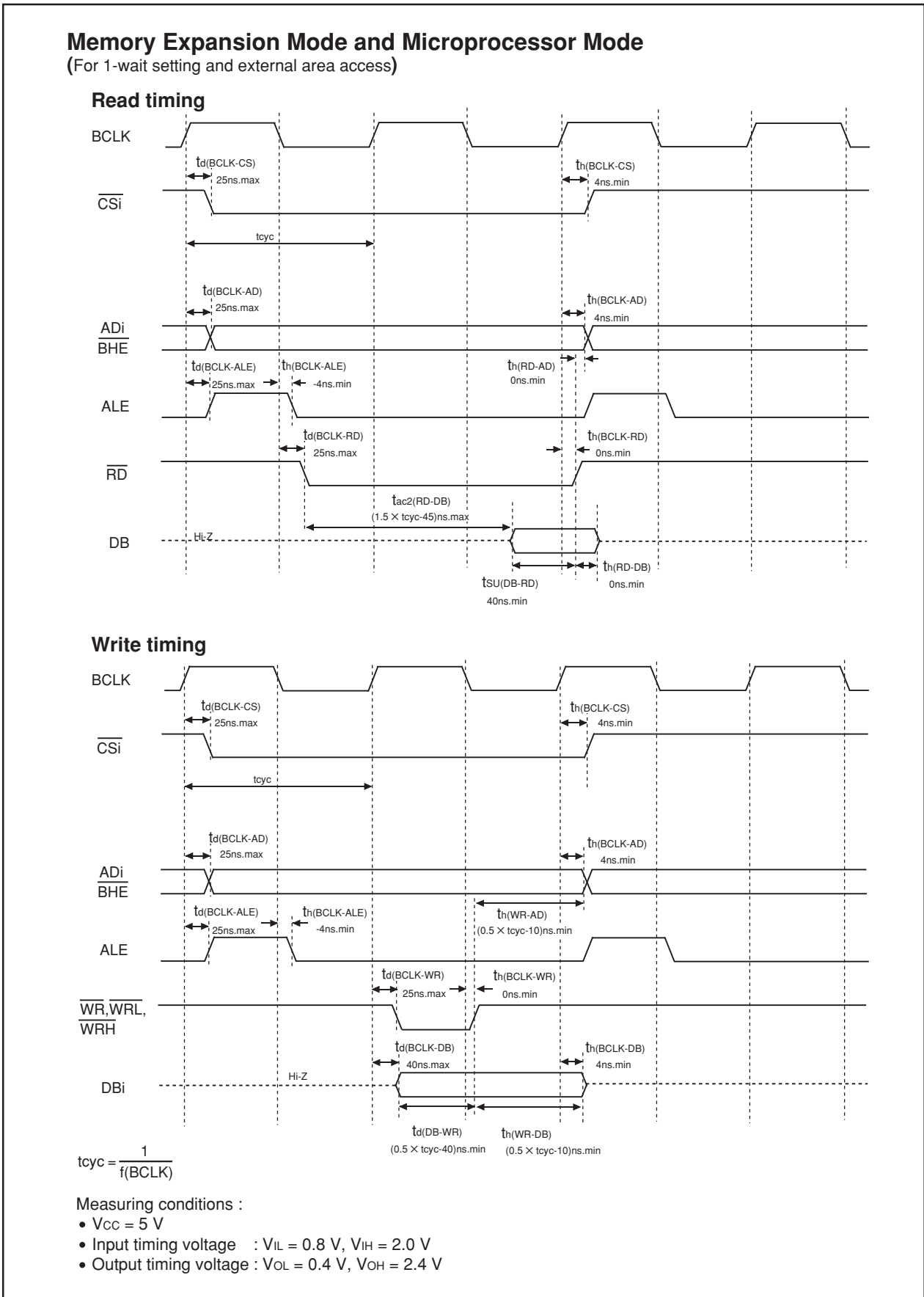


Figure 5.5 Timing Diagram (4)

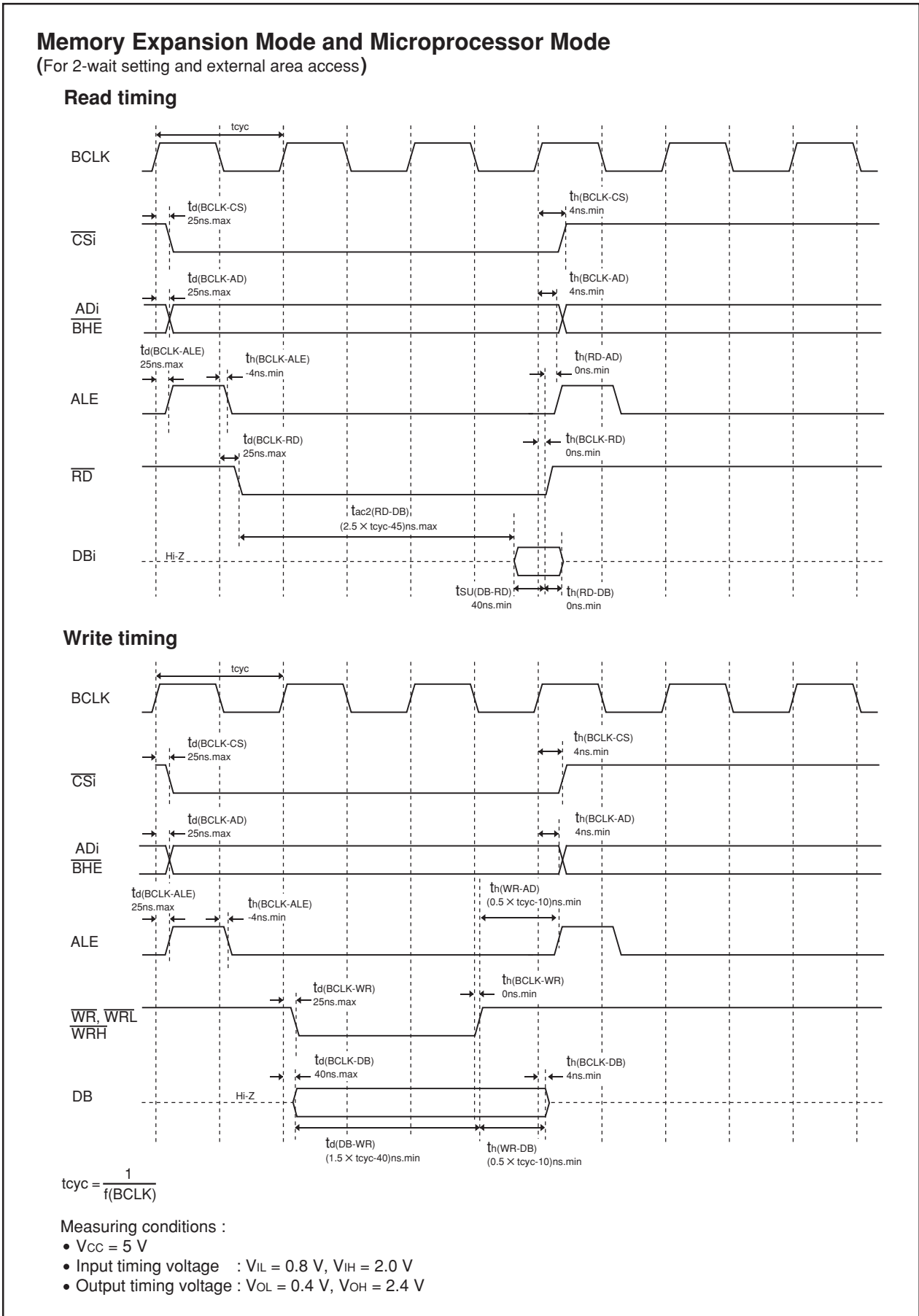


Figure 5.6 Timing Diagram (5)

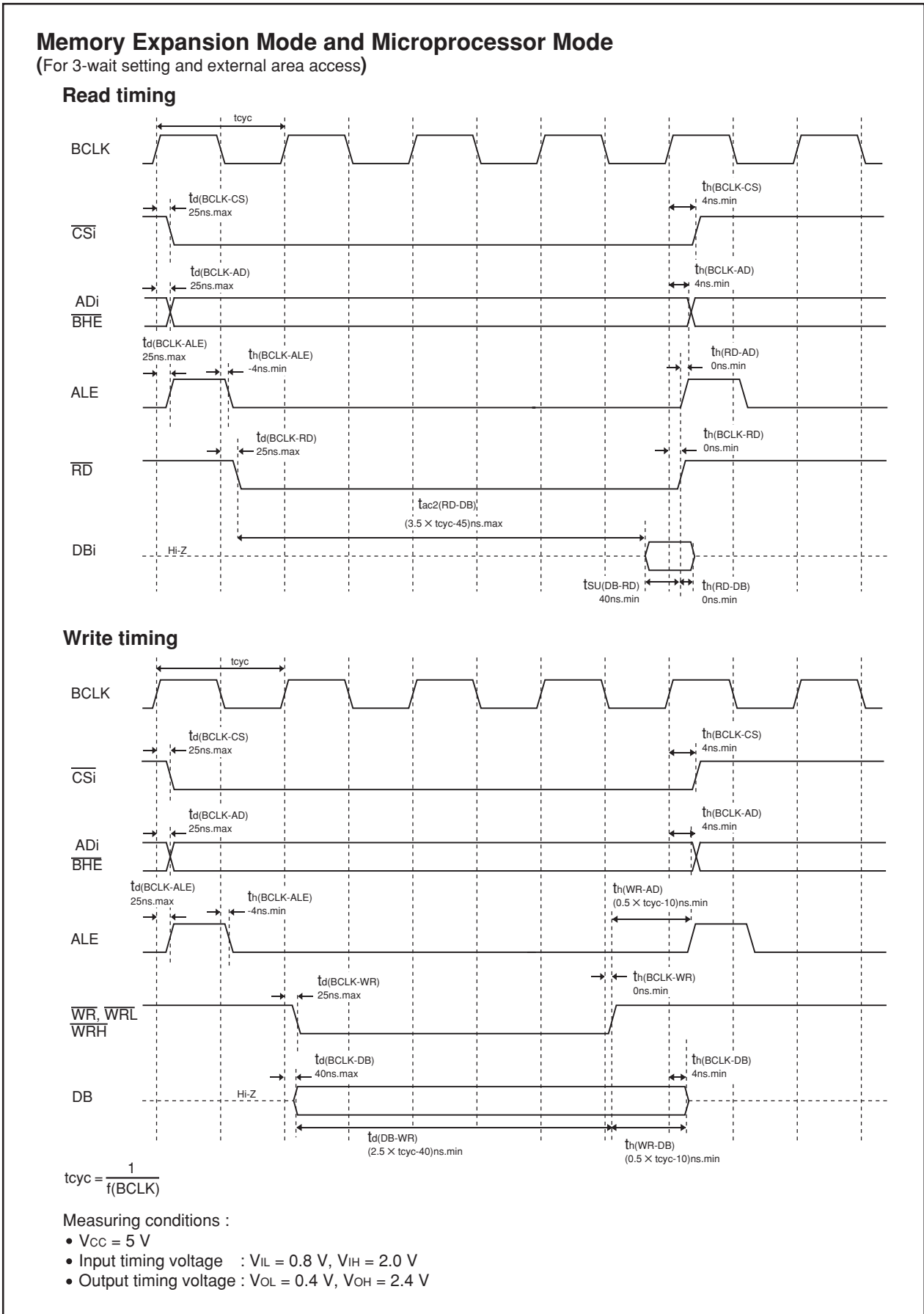
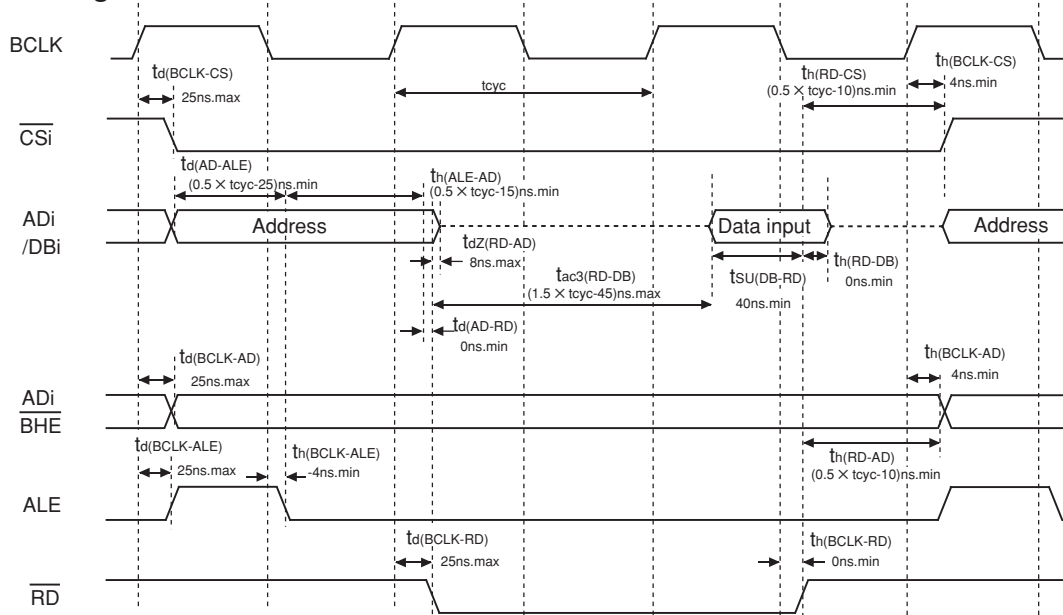


Figure 5.7 Timing Diagram (6)

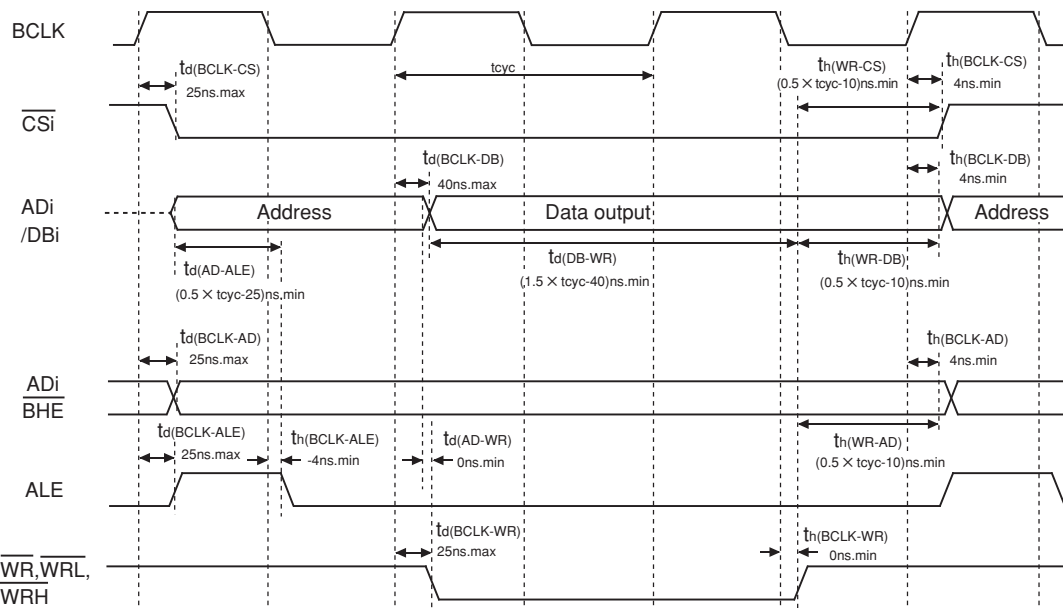
Memory Expansion Mode and Microprocessor Mode

(For 1- or 2-wait setting, external area access and multiplexed bus selection)

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(\text{BCLK})}$$

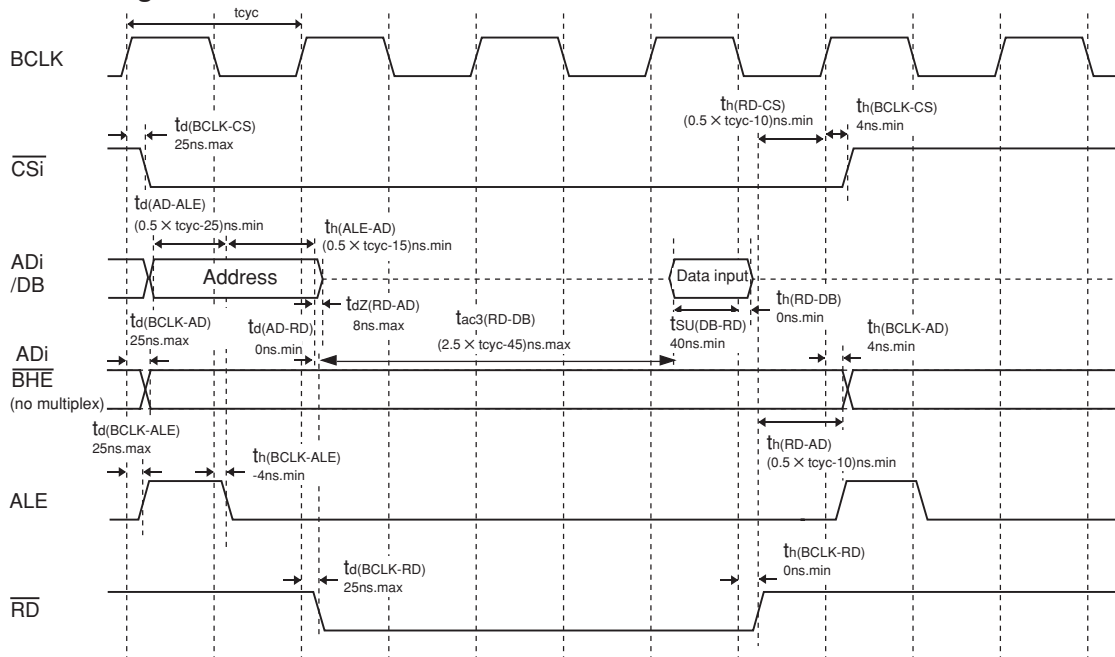
Measuring conditions :

- $V_{CC} = 5\text{ V}$
- Input timing voltage : $V_{IL} = 0.8\text{ V}, V_{IH} = 2.0\text{ V}$
- Output timing voltage : $V_{OL} = 0.4\text{ V}, V_{OH} = 2.4\text{ V}$

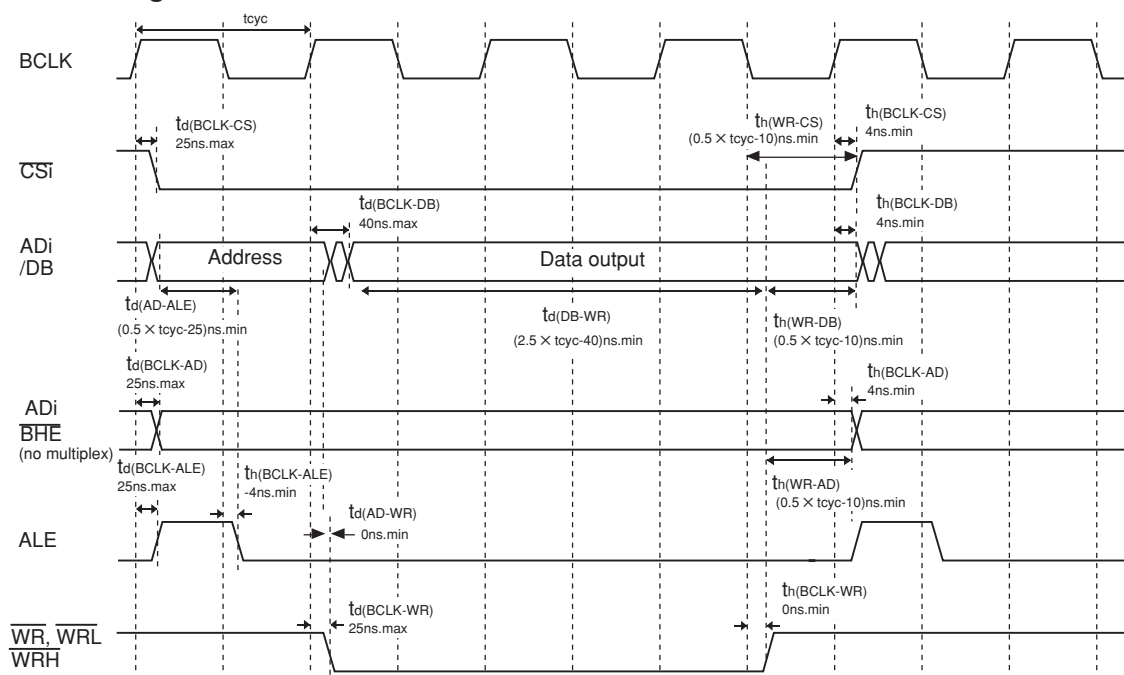
Figure 5.8 Timing Diagram (7)

Memory Expansion Mode and Microprocessor Mode (For 3-wait setting, external area access and multiplexed bus selection)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

- $V_{CC} = 5 V$
- Input timing voltage : $V_{IL} = 0.8 V, V_{IH} = 2.0 V$
- Output timing voltage : $V_{OL} = 0.4 V, V_{OH} = 2.4 V$

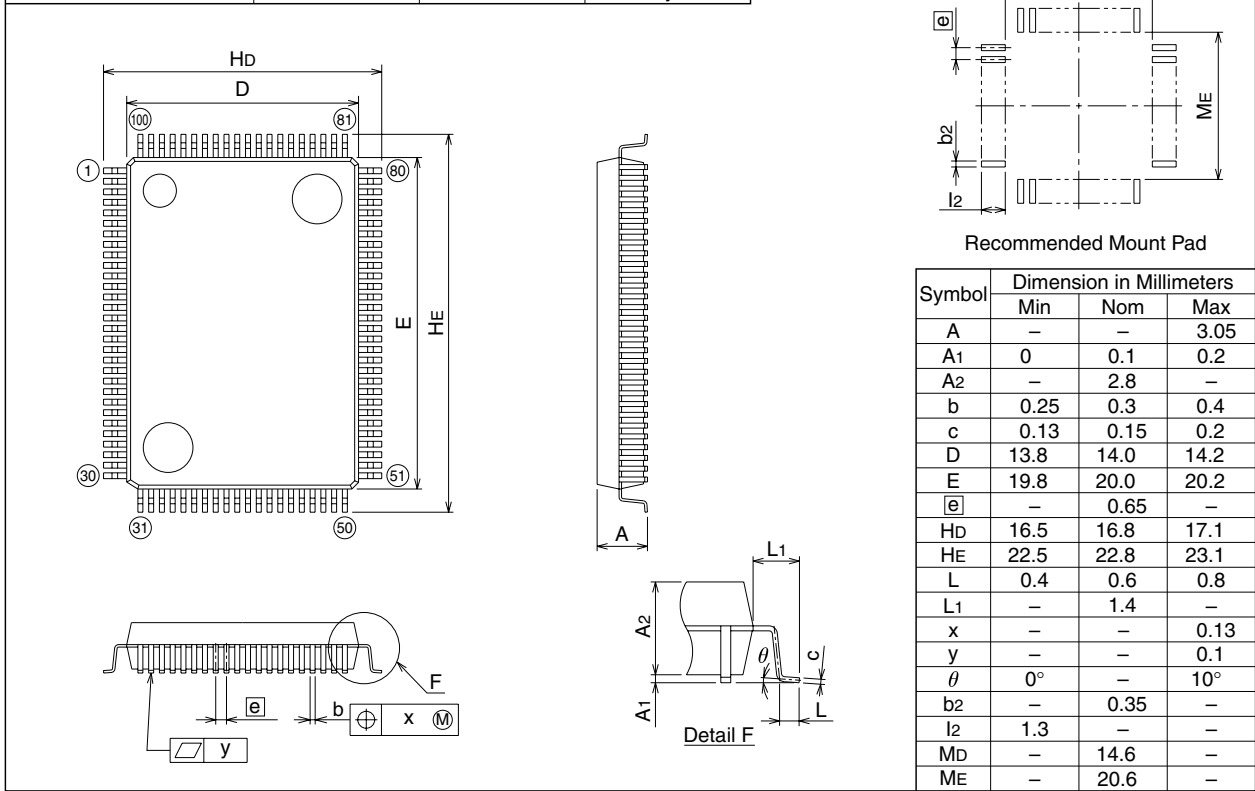
Figure 5.9 Timing Diagram (8)

Package Dimension

100P6S-A (MMP)

Plastic 100pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	-	1.58	Alloy 42



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	3.05
A1	0	0.1	0.2
A2	-	2.8	-
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	-	0.65	-
Hd	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	-	1.4	-
x	-	-	0.13
y	-	-	0.1
θ	0°	-	10°
b2	-	0.35	-
l2	1.3	-	-
MD	-	14.6	-
ME	-	20.6	-

REVISION HISTORY	M16C/6N4 Group Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Jun. 30, 2003	–	First edition issued

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