M16C/6N5 Group

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0004-0100Z
Rev.1.00
Jun 30, 2003

1. Overview

The M16C/6N5 group of single-chip microcomputers are built using the high-performance silicon gate CMOS process using an M16C/60 Series CPU core and are packaged in a 100-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed. Being equipped with one CAN (Controller Area Network) module in M16C/6N5 group, the microcomputer is suited to drive automotive and industrial control systems. The CAN module comply with the 2.0B specification. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Automotive, industrial control systems and other autmobile, other

1.2 Performance Outline

Table 1.1 lists a performance outline of M16C/6N5 group.

Table 1.1 Performance outline of M16C/6N5 Group

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		50.0 ns (f(BCLK)=20MHz, 1/1 prescaler, without software wait)
Memory capacity	ROM	128 Kbytes
	RAM	5 Kbytes
I/O port	P0 to P10 (except $P8_5$)	8 bits × 10, 7 bits × 1
Input port	$P8_5$	1 bit × 1 ($\overline{NMI}$ pin level judgment)
Multifunction timer	TA0, TA1, TA2, TA3, TA4	Output: 16 bits × 5 channels
	TB0, TB1, TB2, TB3, TB4, TB5	Input: 16 bits × 6 channels
Serial I/O	UART0, UART1, UART2	3 channels: UART, clock synchronous, I^2C-bus (Note 1) (option) or IEBus (Note 2) (option)
	SI/O3	1 channel: Clock synchronous
A-D converter		10 bits × (8 × 3 + 2) channels
D-A converter		8 bits × 2 channels
DMAC		2 channels (trigger: 24 sources)
CRC calculation circuit		1 circuit: CRC-CCITT
CAN Module		1 channel with 2.0B specification
Watchdog timer		15 bits × 1 (with prescaler)
Interrupt		29 internal and 9 external sources, 4 software sources, 7 levels
Clock generation circuit		4 circuits · Main clock, · Sub clock } (These circuit contain a built-in feedback resistor; and external ceramic/quartz oscillator) · Ring oscillator · PLL frequency synthesizer Main clock oscillation stop and re-oscillation detection function
Power supply voltage		4.2 to 5.5V (f(BCLK)=20MHz, 1/1 prescaler, without software wait)
Flash memory	Program/erase voltage	5.0 ± 0.5 V
	Number of program/erase	100 times
Power consumption		Mask ROM version: 16 mA (Vcc=5V, (f(BCLK)=20MHz, 1/1 prescaler, without software wait) Flash memory version: 18 mA (Vcc=5V, (f(BCLK)=20MHz, 1/1 prescaler, without software wait)
I/O characteristics	I/O withstand voltage	5.0 V
	Output current	5 mA
Operating ambient temperature		-40 to 85°C (T version) -40 to 125°C (V version) (option)
Memory expansion		Available (to 1 Mbyte)
Device configuration		CMOS high performance silicon gate
Package		100-pin plastic mold QFP

Note 1: I^2C-bus is a registered trademark of Koninklijke Philips Electronics N.V.
Note 2: IEBus is a registered trademark of NEC Electronics Corporation.

option: If you desire this option, please so specify.

1.3 Block Diagram

Figure 1.1 shows a block diagram of M16C/6N5 group.

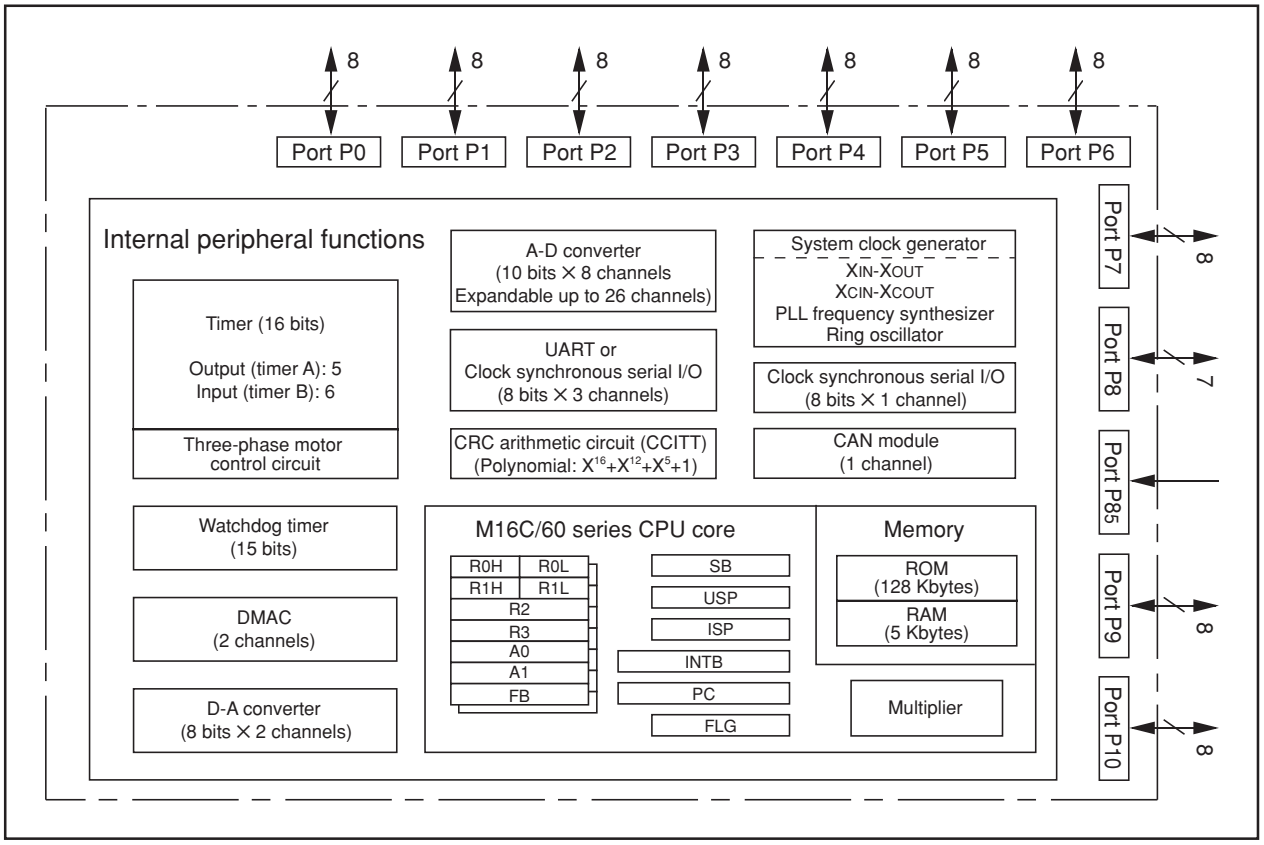


Figure 1.1 Block Diagram

1.4 Product List

Table 1.2 lists the M16C/6N5 group products and Figure 1.2 shows the type numbers, memory sizes and packages.

Table 1.2 Product List As of May 2003

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M306N5MCT-XXXFP **	128 Kbytes	5 Kbytes	100P6S-A	Mask ROM version
M306N5MCV-XXXFP *				
M306N5FCTFP **				Flash memory version
M306N5FCVFP *				

*: Under planning

**: Under development

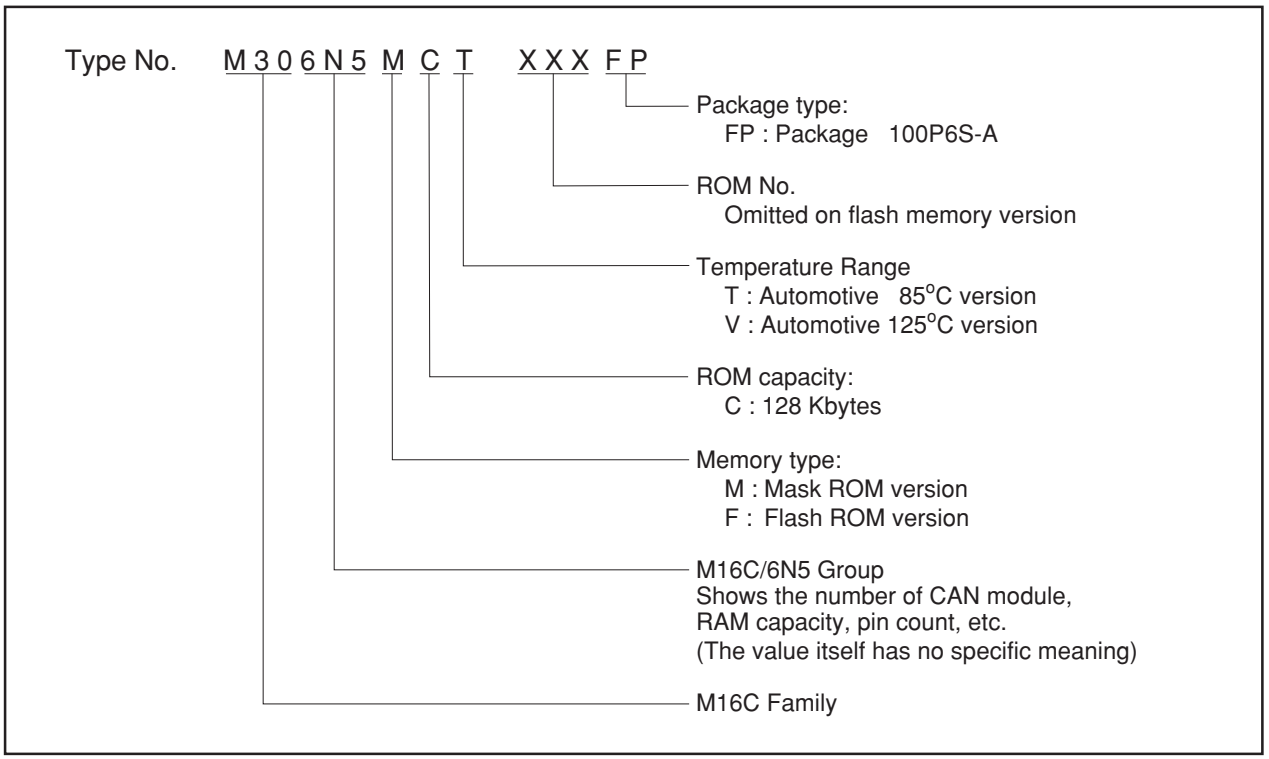


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Configuration

Figure 1.3 shows the pin configuration (top view).

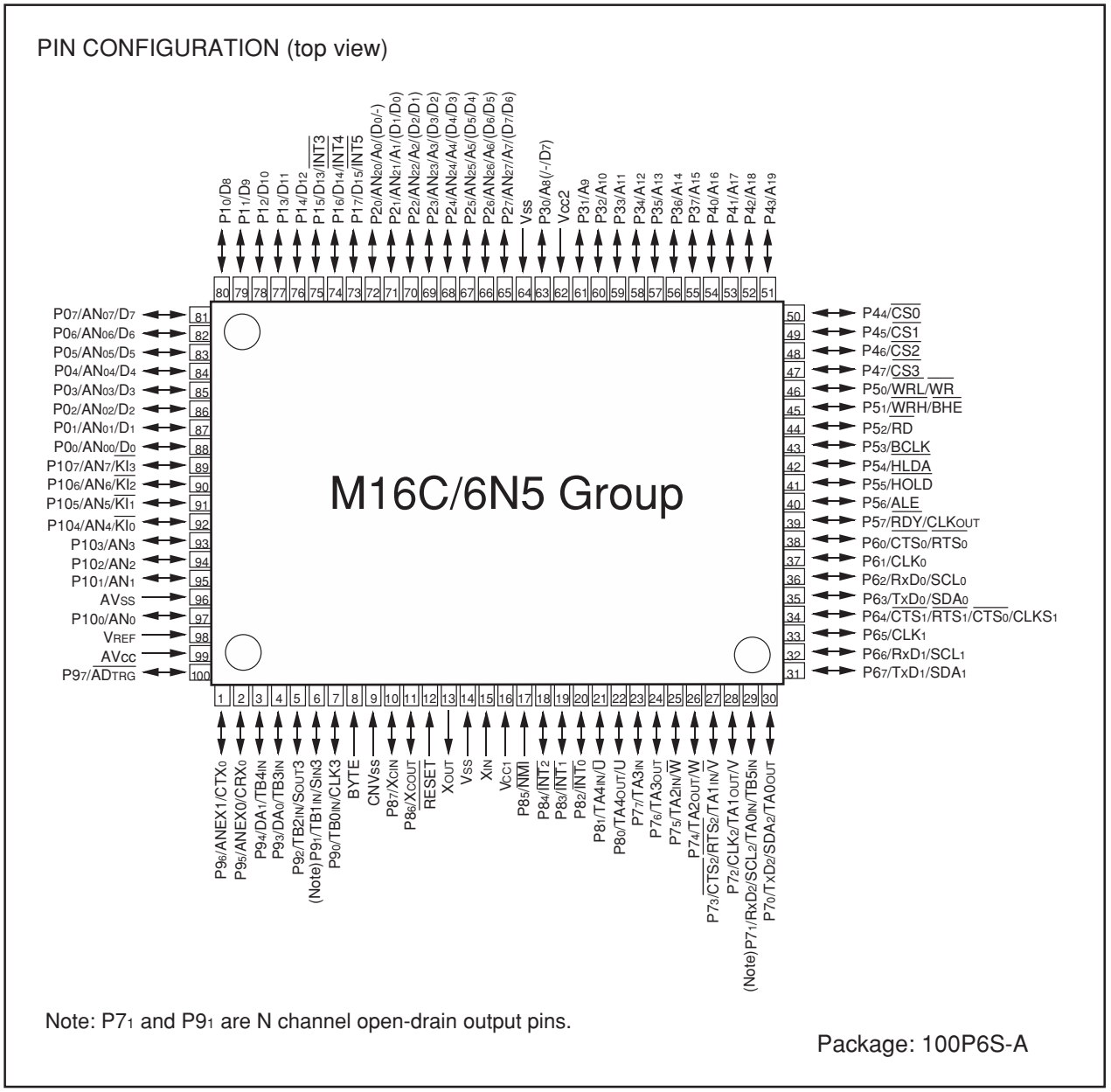


Figure 1.3 Pin Configuration (Top View)

1.6 Pin Description

Tables 1.3 and 1.4 list the pin descriptions.

Table 1.3 Pin Description (1)

Pin name	Signal name	I/O type	Function
V_{CC1}, V_{CC2} V_{SS}	Power supply input		Apply 4.2 to 5.5 V to the V_{CC1} and V_{CC2} pins and 0 V to the V_{SS} pin. The V_{CC} apply condition is that V_{CC2} = V_{CC1}.
CNVSS	CNVSS	Input	This pin switches between processor modes. Connect this pin to the V_{SS} pin when after a reset you want to start operation in single-chip mode (memory expansion mode) or the V_{CC1} pin when starting operation in microprocessor mode.
$\overline{RESET}$	Reset input	Input	"L" on this input resets the microcomputer.
X_{IN}	Clock input	Input	These pins are provided for the main clock oscillation circuit input/output. Connect a ceramic resonator or crystal between the X_{IN} and the X_{OUT} pins. To use an externally derived clock, input it to the X_{IN} pin and leave the X_{OUT} pin open.
X_{OUT}	Clock output	Output	
BYTE	External data bus width select input	Input	This pin selects the width of an external data bus. A 16-bit width is selected when this input is "L"; an 8-bit width is selected when this input is "H". This input must be fixed to either "H" or "L". Connect this pin to the V_{SS} pin when operating in single-chip mode.
AVCC	Analog power supply input		This pin is a power supply input for the A-D converter. Connect this pin to V_{CC1}.
AVSS	Analog power supply input		This pin is a power supply input for the A-D converter. Connect this pin to V_{SS}.
V_{REF}	Reference voltage input	Input	This pin is a reference voltage input for the A-D converter and D-A converter.
$P0_0$ to $P0_7$	I/O port P0	Input/output	This is an 8-bit CMOS I/O port. This port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. If any port is set for input, selection can be made for it in a program whether or not to have a pull-up resistor in 4-bit unit. This selection is unavailable in memory expansion and microprocessor modes. This port can function as input pins for the A-D converter when so selected in a program.
D_0 to D_7		Input/output	When set as a separate bus, these pins input and output data (D_0 to D_7).
$P1_0$ to $P1_7$	I/O port P1	Input/output	This is an 8-bit I/O port equivalent to P0. $P1_5$ to $P1_7$ also function as $\overline{INT}$ interrupt input pins as selected by a program.
D_8 to D_{15}		Input/output	When set as a separate bus, these pins input and output data (D_8 to D_{15}).
$P2_0$ to $P2_7$	I/O port P2	Input/output	This is an 8-bit I/O port equivalent to P0. This port can function as input pins for the A-D converter when so selected in a program.
A_0 to A_7		Output	These pins output 8 low-order address bits (A_0 to A_7).
A_0/D_0 to A_7/D_7		Input/output	If the external bus is set as an 8-bit width multiplexed bus, these pins input and output data (D_0 to D_7) and output 8 low-order address bits (A_0 to A_7) separated in time by multiplexing.
A_0, A_1/D_0 to A_7/D_6		Output Input/output	If the external bus is set as a 16-bit width multiplexed bus, these pins input and output data (D_0 to D_6) and output address (A_1 to A_7) separated in time by multiplexing. They also output address (A_0).
$P3_0$ to $P3_7$	I/O port P3	Input/output	This is an 8-bit I/O port equivalent to P0.
A_8 to A_{15}		Output	These pins output 8 middle-order address bits (A_8 to A_{15}).
A_8/D_7, A_9 to A_{15}		Input/output Output	If the external bus is set as a 16-bit width multiplexed bus, these pins input and output data (D_7) and output address (A_8) separated in time by multiplexing. They also output address (A_9 to A_{15}).
$P4_0$ to $P4_7$	I/O port P4	Input/output	This is an 8-bit I/O port equivalent to P0.
A_{16} to A_{19}, $\overline{CS_0}$ to $\overline{CS_3}$		Output Output	These pins output A_{16} to A_{19} and $\overline{CS_0}$ to $\overline{CS_3}$ signals. A_{16} to A_{19} are 4 high-order address bits. $\overline{CS_0}$ to $\overline{CS_3}$ are chip select signals used to specify an access space.

Table 1.4 Pin Description (2)

Pin name	Signal name	I/O type	Function
P5$_0$ to P5$_7$	I/O port P5	Input/output	This is an 8-bit I/O port equivalent to P0. In single-chip mode, P5$_7$ in this port outputs a divide-by-8 or divide-by-32 clock of XIN or a clock of the same frequency as XCIN as selected by program.
$\overline{WRL}$ / $\overline{WR}$, $\overline{WRH}$ / $\overline{BHE}$, $\overline{RD}$, BCLK, $\overline{HLDA}$, $\overline{HOLD}$, ALE, $\overline{RDY}$		Output Output Output Output Output Input Output Input	Output $\overline{WRL}$/$\overline{WR}$, $\overline{WRH}$/$\overline{BHE}$, $\overline{RD}$, BCLK, $\overline{HLDA}$, and ALE signals. $\overline{WRL}$/$\overline{WR}$ and $\overline{WRH}$/$\overline{BHE}$ are switchable in a program. Note that $\overline{WRL}$ and $\overline{WRH}$ are always used as a pair, so as $\overline{WR}$ and $\overline{BHE}$. ■ $\overline{WRL}$, $\overline{WRH}$, and $\overline{RD}$ selected If the external data bus is a 16-bit width, data are written to even addresses when the $\overline{WRL}$ signal is low, and written to odd addresses when the $\overline{WRH}$ signal is low. Data are read out when the $\overline{RD}$ signal is low. ■ $\overline{WR}$, $\overline{BHE}$, and $\overline{RD}$ selected Data are written when the $\overline{WR}$ signal is low, or read out when the $\overline{RD}$ signal is low. Odd addresses are accessed when the $\overline{BHE}$ signal is low. Use this mode when the external data bus is an 8-bit width. The microcomputer goes to a hold state when input to the $\overline{HOLD}$ pin is held low. While in the hold state, $\overline{HLDA}$ outputs a low level. ALE is used to latch the address. While the input level of the $\overline{RDY}$ pin is low, the bus of the microcomputer goes to a wait state.
P6$_0$ to P6$_7$	I/O port P6	Input/output	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as UART0 and UART1 I/O pins as selected by program.
P7$_0$ to P7$_7$	I/O port P7	Input/output	This is an 8-bit I/O port equivalent to P0 (P7$_1$ is an N channel open-drain output). This port can function as input/output pins for timers A0 to A3 when so selected in a program. Furthermore, P7$_0$ to P7$_3$, P7$_1$, P7$_2$ to P7$_5$ and P7$_6$, P7$_7$ can also function as input/output pins for UART2, an input pin for timer B5, and output pins for the three-phase motor control timer, respectively.
P8$_0$ to P8$_4$, P8$_6$, P8$_7$	I/O port P8	Input/output Input/output Input/output	P8$_0$ to P8$_4$, P8$_6$ and P8$_7$ are I/O ports with the same functions as P0. When so selected in a program, P8$_0$, P8$_1$, and P8$_2$ to P8$_4$ can function as input/output pins for timer A4 or output pins for the three-phase motor control timer and $\overline{INT}$ interrupt input pins, respectively. P8$_6$ and P8$_7$, when so selected in a program, both can function as input/output pins for the sub clock oscillator circuit. In that case, connect a crystal resonator between P8$_6$ (XCOUT pin) and P8$_7$ (XCIN pin).
P8$_5$	Input port P8$_5$	Input	P8$_5$ is an input-only port shared with $\overline{NMI}$. An $\overline{NMI}$ interrupt request is generated when input on this pin changes state from high to low. The $\overline{NMI}$ function cannot be disabled in a program. A pull-up cannot be set for this pin.
P9$_0$ to P9$_7$	I/O port P9	Input/output	This is an 8-bit I/O port equivalent to P0 (P9$_1$ is an N channel open-drain output). Pins in this port also function as input/output pins for SI/O3, input pins for times B0 to B4, output pins for D-A converter, and input pins for A-D converter or input/output pins for CAN0, or input pins for A-D trigger as selected by program.
P10$_0$ to P10$_7$	I/O port P10	Input/output	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as input pins for A-D converter as selected by program. Furthermore, P10$_4$ to P10$_7$ also function as input pins for the key input interrupt function.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

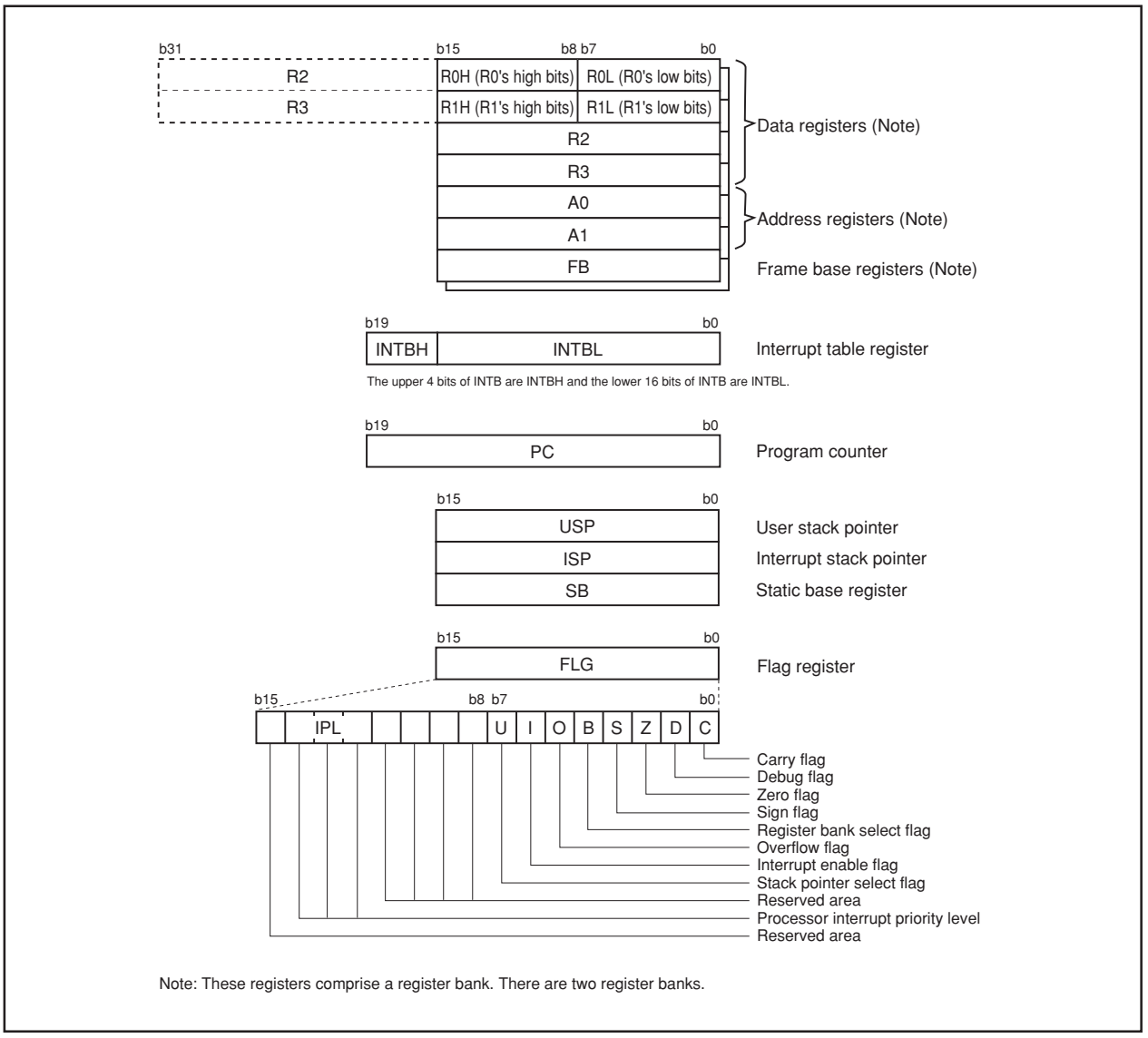


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The A0 register consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.
Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

This flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.

2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.
Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is set to “0” when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0” ; USP is selected when the U flag is “1”.
The U flag is set to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has priority greater than IPL, the interrupt request is enabled.

2.8.10 Reserved Area

When white to this bit, write “0”. When read, its content is indeterminate.

3. Memory

Figure 3.1 shows a memory map of the M16C/6N5 group. The address space extends the 1 Mbyte from address 00000_{16} to $FFFFF_{16}$.

The internal ROM is allocated in a lower address direction beginning with address $FFFFF_{16}$. For example, a 128-Kbyte internal ROM is allocated to the addresses from $E0000_{16}$ to $FFFFF_{16}$.

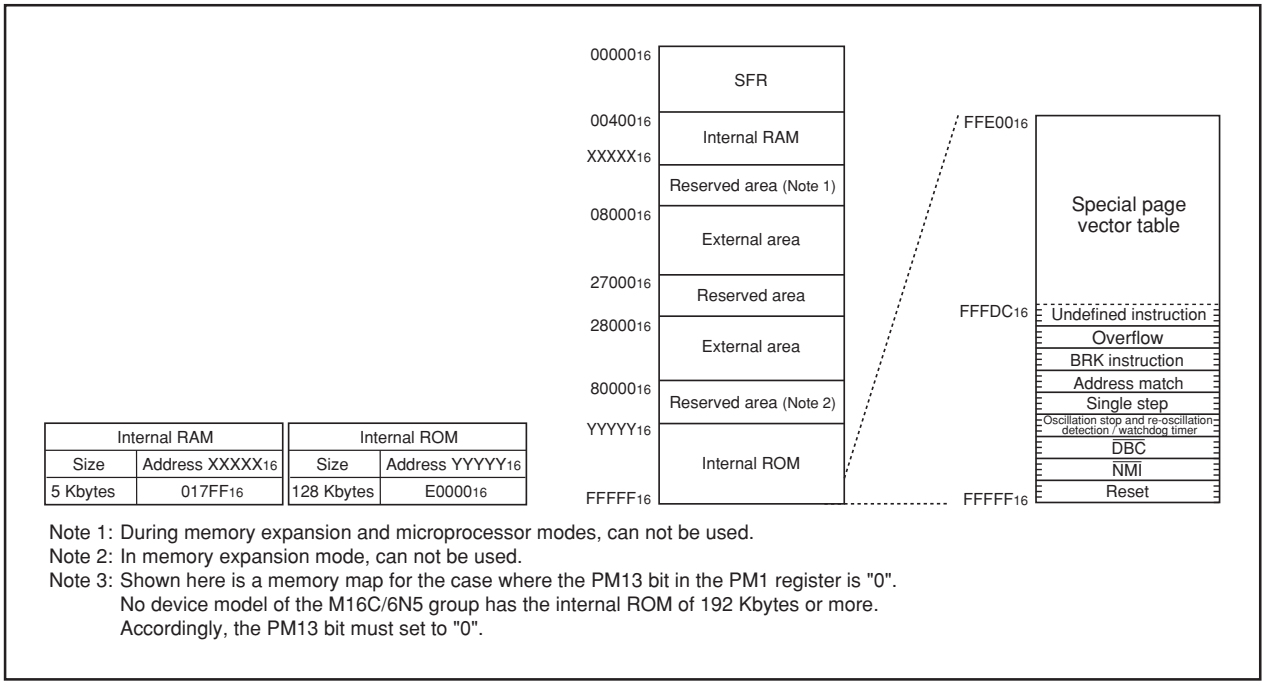
The fixed interrupt vector table is allocated to the addresses from $FFFDC_{16}$ to $FFFFF_{16}$. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400_{16}. For example, a 5-Kbyte internal RAM is allocated to the addresses from 00400_{16} to $017FF_{16}$. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SFR is allocated to the addresses from 00000_{16} to $003FF_{16}$. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.

The special page vector table is allocated to the addresses from $FFE00_{16}$ to $FFFDB_{16}$. This vector is used by the JMPS or JSRS instruction. For details, refer to the “M16C/60 and M16C/20 Series Software Manual”.

In memory expansion and microprocessor modes, some areas are reserved for future use and cannot be used by users.



Internal RAM	
Size	Address XXXXX16
5 Kbytes	017FF16

Internal ROM	
Size	Address YYYYY16
128 Kbytes	E000016

Note 1: During memory expansion and microprocessor modes, can not be used.
Note 2: In memory expansion mode, can not be used.
Note 3: Shown here is a memory map for the case where the PM13 bit in the PM1 register is "0". No device model of the M16C/6N5 group has the internal ROM of 192 Kbytes or more. Accordingly, the PM13 bit must set to "0".

Figure 3.1 Memory Map

4. SFR

Figures 4.1 to 4.12 show the location of peripheral function control registers and the value after reset.

Address	Register	Symbol	After reset
0000_{16}			
0001_{16}			
0002_{16}			
0003_{16}			
0004_{16}	Processor mode register 0 (Note 1)	PM0	00000000_2 (CNV_{SS} pin is "L") 00000011_2 (CNV_{SS} pin is "H")
0005_{16}	Processor mode register 1	PM1	$0XXX1000_2$
0006_{16}	System clock control register 0	CM0	01001000_2
0007_{16}	System clock control register 1	CM1	00100000_2
0008_{16}	Chip select control register	CSR	00000001_2
0009_{16}	Address match interrupt enable register	AIER	$XXXXXX00_2$
$000A_{16}$	Protect register	PRCR	$XX000000_2$
$000B_{16}$			
$000C_{16}$	Oscillation stop detection register (Note 2)	CM2	$0X00X000_2$
$000D_{16}$			
$000E_{16}$	Watchdog timer start register	WDTS	XX_{16}
$000F_{16}$	Watchdog timer control register	WDC	$00XXXXXX_2$
0010_{16}	Address match interrupt register 0	RMAD0	00_{16}
0011_{16}			00_{16}
0012_{16}			$X0_{16}$
0013_{16}			
0014_{16}	Address match interrupt register 1	RMAD1	00_{16}
0015_{16}			00_{16}
0016_{16}			$X0_{16}$
0017_{16}			
0018_{16}			
0019_{16}			
$001A_{16}$			
$001B_{16}$	Chip select expansion control register	CSE	00_{16}
$001C_{16}$	PLL control register 0	PLC0	$0001X010_2$
$001D_{16}$			
$001E_{16}$	Processor mode register 2	PM2	$XXX00000_2$
$001F_{16}$			
0020_{16}	DMA0 source pointer	SAR0	XX_{16}
0021_{16}			XX_{16}
0022_{16}			XX_{16}
0023_{16}			
0024_{16}	DMA0 destination pointer	DAR0	XX_{16}
0025_{16}			XX_{16}
0026_{16}			XX_{16}
0027_{16}			
0028_{16}	DMA0 transfer counter	TCR0	XX_{16}
0029_{16}			XX_{16}
$002A_{16}$			
$002B_{16}$			
$002C_{16}$	DMA0 control register	DM0CON	$00000X00_2$
$002D_{16}$			
$002E_{16}$			
$002F_{16}$			
0030_{16}	DMA1 source pointer	SAR1	XX_{16}
0031_{16}			XX_{16}
0032_{16}			XX_{16}
0033_{16}			
0034_{16}	DMA1 destination pointer	DAR1	XX_{16}
0035_{16}			XX_{16}
0036_{16}			XX_{16}
0037_{16}			
0038_{16}	DMA1 transfer counter	TCR1	XX_{16}
0039_{16}			XX_{16}
$003A_{16}$			
$003B_{16}$			
$003C_{16}$	DMA1 control register	DM1CON	$00000X00_2$
$003D_{16}$			
$003E_{16}$			
$003F_{16}$			

X: Undefined

Note 1: The PM00 and PM01 bits do not change at software reset, watchdog timer reset and oscillation stop detection reset.
Note 2: The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
Note 3: The blank areas are reserved and cannot be accessed by users.

Figure 4.1 Location of Peripheral Function Control Registers and Value at After Reset (1)

Address	Register	Symbol	After reset
0040_{16}			
0041_{16}	CAN0 wake up interrupt control register	C01WKIC	$XXXXX000_2$
0042_{16}	CAN0 successful reception interrupt control register	C0RECIC	$XXXXX000_2$
0043_{16}	CAN0 successful transmission interrupt control register	C0TRMIC	$XXXXX000_2$
0044_{16}	INT3 interrupt control register	INT3IC	$XX00X000_2$
0045_{16}	Timer B5 interrupt control register	TB5IC	$XXXXX000_2$
0046_{16}	Timer B4 interrupt control register	TB4IC	$XXXXX000_2$
	UART1 bus collision detection interrupt control register	U1BCNIC	
0047_{16}	Timer B3 interrupt control register	TB3IC	$XXXXX000_2$
	UART0 bus collision detection interrupt control register	U0BCNIC	
0048_{16}	INT5 interrupt control register	INT5IC	$XX00X000_2$
0049_{16}	SI/O3 interrupt control register	S3IC	$XX00X000_2$
	INT4 interrupt control register	INT4IC	
$004A_{16}$	UART2 bus collision detection interrupt control register	U2BCNIC	$XXXXX000_2$
$004B_{16}$	DMA0 interrupt control register	DM0IC	$XXXXX000_2$
$004C_{16}$	DMA1 interrupt control register	DM1IC	$XXXXX000_2$
$004D_{16}$	CAN0 error interrupt control register	C01ERRIC	$XXXXX000_2$
$004E_{16}$	A-D conversion interrupt control register	ADIC	$XXXXX000_2$
	Key input interrupt control register	KUPIC	
$004F_{16}$	UART2 transmit interrupt control register	S2TIC	$XXXXX000_2$
0050_{16}	UART2 receive interrupt control register	S2RIC	$XXXXX000_2$
0051_{16}	UART0 transmit interrupt control register	S0TIC	$XXXXX000_2$
0052_{16}	UART0 receive interrupt control register	S0RIC	$XXXXX000_2$
0053_{16}	UART1 transmit interrupt control register	S1TIC	$XXXXX000_2$
0054_{16}	UART1 receive interrupt control register	S1RIC	$XXXXX000_2$
0055_{16}	Timer A0 interrupt control register	TA0IC	$XXXXX000_2$
0056_{16}	Timer A1 interrupt control register	TA1IC	$XXXXX000_2$
0057_{16}	Timer A2 interrupt control register	TA2IC	$XXXXX000_2$
0058_{16}	Timer A3 interrupt control register	TA3IC	$XXXXX000_2$
0059_{16}	Timer A4 interrupt control register	TA4IC	$XXXXX000_2$
$005A_{16}$	Timer B0 interrupt control register	TB0IC	$XXXXX000_2$
$005B_{16}$	Timer B1 interrupt control register	TB1IC	$XXXXX000_2$
$005C_{16}$	Timer B2 interrupt control register	TB2IC	$XXXXX000_2$
$005D_{16}$	INT0 interrupt control register	INT0IC	$XX00X000_2$
$005E_{16}$	INT1 interrupt control register	INT1IC	$XX00X000_2$
$005F_{16}$	INT2 interrupt control register	INT2IC	$XX00X000_2$
0060_{16}	CAN0 message box 0: Identifier / DLC		XX_{16}
0061_{16}			XX_{16}
0062_{16}			XX_{16}
0063_{16}			XX_{16}
0064_{16}			XX_{16}
0065_{16}			XX_{16}
0066_{16}	CAN0 message box 0: Data field		XX_{16}
0067_{16}			XX_{16}
0068_{16}			XX_{16}
0069_{16}			XX_{16}
$006A_{16}$			XX_{16}
$006B_{16}$			XX_{16}
$006C_{16}$			XX_{16}
$006D_{16}$			XX_{16}
$006E_{16}$	CAN0 message box 0: Time stamp		XX_{16}
$006F_{16}$			XX_{16}
0070_{16}	CAN0 message box 1: Identifier / DLC		XX_{16}
0071_{16}			XX_{16}
0072_{16}			XX_{16}
0073_{16}			XX_{16}
0074_{16}			XX_{16}
0075_{16}			XX_{16}
0076_{16}	CAN0 message box 1: data Field		XX_{16}
0077_{16}			XX_{16}
0078_{16}			XX_{16}
0079_{16}			XX_{16}
$007A_{16}$			XX_{16}
$007B_{16}$			XX_{16}
$007C_{16}$			XX_{16}
$007D_{16}$			XX_{16}
$007E_{16}$	CAN0 message box 1: Time stamp		XX_{16}
$007F_{16}$			XX_{16}

X: Undefined

Note: The blank area is reserved and cannot be accessed by users.

Figure 4.2 Location of Peripheral Function Control Registers and Value at After Reset (2)

Address	Register	Symbol	After reset
0080₁₆	CAN0 message box 2: Identifier / DLC		XX₁₆
0081₁₆			XX₁₆
0082₁₆			XX₁₆
0083₁₆			XX₁₆
0084₁₆			XX₁₆
0085₁₆			XX₁₆
0086₁₆	CAN0 message box 2: Data field		XX₁₆
0087₁₆			XX₁₆
0088₁₆			XX₁₆
0089₁₆			XX₁₆
008A₁₆			XX₁₆
008B₁₆			XX₁₆
008C₁₆			XX₁₆
008D₁₆			XX₁₆
008E₁₆	CAN0 message box 2: Time stamp		XX₁₆
008F₁₆			XX₁₆
0090₁₆	CAN0 message box 3: Identifier / DLC		XX₁₆
0091₁₆			XX₁₆
0092₁₆			XX₁₆
0093₁₆			XX₁₆
0094₁₆			XX₁₆
0095₁₆			XX₁₆
0096₁₆	CAN0 message box 3: Data field		XX₁₆
0097₁₆			XX₁₆
0098₁₆			XX₁₆
0099₁₆			XX₁₆
009A₁₆			XX₁₆
009B₁₆			XX₁₆
009C₁₆			XX₁₆
009D₁₆			XX₁₆
009E₁₆	CAN0 message box 3: Time stamp		XX₁₆
009F₁₆			XX₁₆
00A0₁₆	CAN0 message box 4: Identifier / DLC		XX₁₆
00A1₁₆			XX₁₆
00A2₁₆			XX₁₆
00A3₁₆			XX₁₆
00A4₁₆			XX₁₆
00A5₁₆			XX₁₆
00A6₁₆	CAN0 message box 4: Data field		XX₁₆
00A7₁₆			XX₁₆
00A8₁₆			XX₁₆
00A9₁₆			XX₁₆
00AA₁₆			XX₁₆
00AB₁₆			XX₁₆
00AC₁₆			XX₁₆
00AD₁₆			XX₁₆
00AE₁₆	CAN0 message box 4: Time stamp		XX₁₆
00AF₁₆			XX₁₆
00B0₁₆	CAN0 message box 5: Identifier / DLC		XX₁₆
00B1₁₆			XX₁₆
00B2₁₆			XX₁₆
00B3₁₆			XX₁₆
00B4₁₆			XX₁₆
00B5₁₆			XX₁₆
00B6₁₆	CAN0 message box 5: Data field		XX₁₆
00B7₁₆			XX₁₆
00B8₁₆			XX₁₆
00B9₁₆			XX₁₆
00BA₁₆			XX₁₆
00BB₁₆			XX₁₆
00BC₁₆			XX₁₆
00BD₁₆			XX₁₆
00BE₁₆	CAN0 message box 5: Time stamp		XX₁₆
00BF₁₆			XX₁₆

X: Undefined

Figure 4.3 Location of Peripheral Function Control Registers and Value at After Reset (3)

Address	Register	Symbol	After reset
00C0$_{16}$	CAN0 message box 6: Identifier / DLC		XX$_{16}$
00C1$_{16}$			XX$_{16}$
00C2$_{16}$			XX$_{16}$
00C3$_{16}$			XX$_{16}$
00C4$_{16}$			XX$_{16}$
00C5$_{16}$			XX$_{16}$
00C6$_{16}$	CAN0 message box 6: Data field		XX$_{16}$
00C7$_{16}$			XX$_{16}$
00C8$_{16}$			XX$_{16}$
00C9$_{16}$			XX$_{16}$
00CA$_{16}$			XX$_{16}$
00CB$_{16}$			XX$_{16}$
00CC$_{16}$			XX$_{16}$
00CD$_{16}$			XX$_{16}$
00CE$_{16}$	CAN0 message box 6: Time stamp		XX$_{16}$
00CF$_{16}$			XX$_{16}$
00D0$_{16}$	CAN0 message box 7: Identifier / DLC		XX$_{16}$
00D1$_{16}$			XX$_{16}$
00D2$_{16}$			XX$_{16}$
00D3$_{16}$			XX$_{16}$
00D4$_{16}$			XX$_{16}$
00D5$_{16}$			XX$_{16}$
00D6$_{16}$	CAN0 message box 7: Data field		XX$_{16}$
00D7$_{16}$			XX$_{16}$
00D8$_{16}$			XX$_{16}$
00D9$_{16}$			XX$_{16}$
00DA$_{16}$			XX$_{16}$
00DB$_{16}$			XX$_{16}$
00DC$_{16}$			XX$_{16}$
00DD$_{16}$			XX$_{16}$
00DE$_{16}$	CAN0 message box 7: Time stamp		XX$_{16}$
00DF$_{16}$			XX$_{16}$
00E0$_{16}$	CAN0 message box 8: Identifier / DLC		XX$_{16}$
00E1$_{16}$			XX$_{16}$
00E2$_{16}$			XX$_{16}$
00E3$_{16}$			XX$_{16}$
00E4$_{16}$			XX$_{16}$
00E5$_{16}$			XX$_{16}$
00E6$_{16}$	CAN0 message box 8: Data field		XX$_{16}$
00E7$_{16}$			XX$_{16}$
00E8$_{16}$			XX$_{16}$
00E9$_{16}$			XX$_{16}$
00EA$_{16}$			XX$_{16}$
00EB$_{16}$			XX$_{16}$
00EC$_{16}$			XX$_{16}$
00ED$_{16}$			XX$_{16}$
00EE$_{16}$	CAN0 message box 8: Time stamp		XX$_{16}$
00EF$_{16}$			XX$_{16}$
00F0$_{16}$	CAN0 message box 9: Identifier / DLC		XX$_{16}$
00F1$_{16}$			XX$_{16}$
00F2$_{16}$			XX$_{16}$
00F3$_{16}$			XX$_{16}$
00F4$_{16}$			XX$_{16}$
00F5$_{16}$			XX$_{16}$
00F6$_{16}$	CAN0 message box 9: Data field		XX$_{16}$
00F7$_{16}$			XX$_{16}$
00F8$_{16}$			XX$_{16}$
00F9$_{16}$			XX$_{16}$
00FA$_{16}$			XX$_{16}$
00FB$_{16}$			XX$_{16}$
00FC$_{16}$			XX$_{16}$
00FD$_{16}$			XX$_{16}$
00FE$_{16}$	CAN0 message box 9: Time stamp		XX$_{16}$
00FF$_{16}$			XX$_{16}$

X: Undefined

Figure 4.4 Location of Peripheral Function Control Registers and Value at After Reset (4)

Address	Register	Symbol	After reset
0100$_{16}$	CAN0 message box 10: Identifier / DLC		XX$_{16}$
0101$_{16}$			XX$_{16}$
0102$_{16}$			XX$_{16}$
0103$_{16}$			XX$_{16}$
0104$_{16}$			XX$_{16}$
0105$_{16}$			XX$_{16}$
0106$_{16}$	CAN0 message box 10: Data field		XX$_{16}$
0107$_{16}$			XX$_{16}$
0108$_{16}$			XX$_{16}$
0109$_{16}$			XX$_{16}$
010A$_{16}$			XX$_{16}$
010B$_{16}$			XX$_{16}$
010C$_{16}$			XX$_{16}$
010D$_{16}$			XX$_{16}$
010E$_{16}$	CAN0 message box 10: Time stamp		XX$_{16}$
010F$_{16}$			XX$_{16}$
0110$_{16}$	CAN0 message box 11: Identifier / DLC		XX$_{16}$
0111$_{16}$			XX$_{16}$
0112$_{16}$			XX$_{16}$
0113$_{16}$			XX$_{16}$
0114$_{16}$			XX$_{16}$
0115$_{16}$			XX$_{16}$
0116$_{16}$	CAN0 message box 11: Data field		XX$_{16}$
0117$_{16}$			XX$_{16}$
0118$_{16}$			XX$_{16}$
0119$_{16}$			XX$_{16}$
011A$_{16}$			XX$_{16}$
011B$_{16}$			XX$_{16}$
011C$_{16}$			XX$_{16}$
011D$_{16}$			XX$_{16}$
011E$_{16}$	CAN0 message box 11: Time stamp		XX$_{16}$
011F$_{16}$			XX$_{16}$
0120$_{16}$	CAN0 message box 12: Identifier / DLC		XX$_{16}$
0121$_{16}$			XX$_{16}$
0122$_{16}$			XX$_{16}$
0123$_{16}$			XX$_{16}$
0124$_{16}$			XX$_{16}$
0125$_{16}$			XX$_{16}$
0126$_{16}$	CAN0 message box 12: Data field		XX$_{16}$
0127$_{16}$			XX$_{16}$
0128$_{16}$			XX$_{16}$
0129$_{16}$			XX$_{16}$
012A$_{16}$			XX$_{16}$
012B$_{16}$			XX$_{16}$
012C$_{16}$			XX$_{16}$
012D$_{16}$			XX$_{16}$
012E$_{16}$	CAN0 message box 12: Time stamp		XX$_{16}$
012F$_{16}$			XX$_{16}$
0130$_{16}$	CAN0 message box 13: Identifier / DLC		XX$_{16}$
0131$_{16}$			XX$_{16}$
0132$_{16}$			XX$_{16}$
0133$_{16}$			XX$_{16}$
0134$_{16}$			XX$_{16}$
0135$_{16}$			XX$_{16}$
0136$_{16}$	CAN0 message box 13: Data field		XX$_{16}$
0137$_{16}$			XX$_{16}$
0138$_{16}$			XX$_{16}$
0139$_{16}$			XX$_{16}$
013A$_{16}$			XX$_{16}$
013B$_{16}$			XX$_{16}$
013C$_{16}$			XX$_{16}$
013D$_{16}$			XX$_{16}$
013E$_{16}$	CAN0 message box 13: Time stamp		XX$_{16}$
013F$_{16}$			XX$_{16}$

X: Undefined

Figure 4.5 Location of Peripheral Function Control Registers and Value at After Reset (5)

Address	Register	Symbol	After reset
0140$_{16}$	CAN0 message box 14: Identifier /DLC		XX$_{16}$
0141$_{16}$			XX$_{16}$
0142$_{16}$			XX$_{16}$
0143$_{16}$			XX$_{16}$
0144$_{16}$			XX$_{16}$
0145$_{16}$			XX$_{16}$
0146$_{16}$	CAN0 message box 14: Data field		XX$_{16}$
0147$_{16}$			XX$_{16}$
0148$_{16}$			XX$_{16}$
0149$_{16}$			XX$_{16}$
014A$_{16}$			XX$_{16}$
014B$_{16}$			XX$_{16}$
014C$_{16}$			XX$_{16}$
014D$_{16}$			XX$_{16}$
014E$_{16}$	CAN0 message box 14: Time stamp		XX$_{16}$
014F$_{16}$			XX$_{16}$
0150$_{16}$	CAN0 message box 15: Identifier /DLC		XX$_{16}$
0151$_{16}$			XX$_{16}$
0152$_{16}$			XX$_{16}$
0153$_{16}$			XX$_{16}$
0154$_{16}$			XX$_{16}$
0155$_{16}$			XX$_{16}$
0156$_{16}$	CAN0 message box 15: Data field		XX$_{16}$
0157$_{16}$			XX$_{16}$
0158$_{16}$			XX$_{16}$
0159$_{16}$			XX$_{16}$
015A$_{16}$			XX$_{16}$
015B$_{16}$			XX$_{16}$
015C$_{16}$			XX$_{16}$
015D$_{16}$			XX$_{16}$
015E$_{16}$	CAN0 message box 15: Time stamp		XX$_{16}$
015F$_{16}$			XX$_{16}$
0160$_{16}$	CAN0 global mask register	C0GMR	XX$_{16}$
0161$_{16}$			XX$_{16}$
0162$_{16}$			XX$_{16}$
0163$_{16}$			XX$_{16}$
0164$_{16}$			XX$_{16}$
0165$_{16}$			XX$_{16}$
0166$_{16}$	CAN0 local mask A register	C0LMAR	XX$_{16}$
0167$_{16}$			XX$_{16}$
0168$_{16}$			XX$_{16}$
0169$_{16}$			XX$_{16}$
016A$_{16}$			XX$_{16}$
016B$_{16}$			XX$_{16}$
016C$_{16}$	CAN0 local mask B register	C0LMBR	XX$_{16}$
016D$_{16}$			XX$_{16}$
016E$_{16}$			XX$_{16}$
016F$_{16}$			XX$_{16}$
0170$_{16}$			XX$_{16}$
0171$_{16}$			XX$_{16}$
0172$_{16}$			
0173$_{16}$			
0174$_{16}$			
0175$_{16}$			
0176$_{16}$			
0177$_{16}$			
0178$_{16}$			
0179$_{16}$			
017A$_{16}$			
017B$_{16}$			
017C$_{16}$			
017D$_{16}$			
017E$_{16}$			
017F$_{16}$			

X: Undefined

Note: The blank areas are reserved and cannot be accessed by users.

Figure 4.6 Location of Peripheral Function Control Registers and Value at After Reset (6)

Address	Register	Symbol	After reset
0180$_{16}$			
0181$_{16}$			
0182$_{16}$			
0183$_{16}$			
0184$_{16}$			
0185$_{16}$			
0186$_{16}$			
0187$_{16}$			
0188$_{16}$			
0189$_{16}$			
018A$_{16}$			
018B$_{16}$			
018C$_{16}$			
018D$_{16}$			
018E$_{16}$			
018F$_{16}$			
0190$_{16}$			
0191$_{16}$			
0192$_{16}$			
0193$_{16}$			
0194$_{16}$			
0195$_{16}$			
0196$_{16}$			
0197$_{16}$			
0198$_{16}$			
0199$_{16}$			
019A$_{16}$			
019B$_{16}$			
019C$_{16}$			
019D$_{16}$			
019E$_{16}$			
019F$_{16}$			
01A0$_{16}$			
01A1$_{16}$			
01A2$_{16}$			
01A3$_{16}$			
01A4$_{16}$			
01A5$_{16}$			
01A6$_{16}$			
01A7$_{16}$			
01A8$_{16}$			
01A9$_{16}$			
01AA$_{16}$			
01AB$_{16}$			
01AC$_{16}$			
01AD$_{16}$			
01AE$_{16}$			
01AF$_{16}$			
01B0$_{16}$			
01B1$_{16}$			
01B2$_{16}$			
01B3$_{16}$			
01B4$_{16}$			
01B5$_{16}$	Flash memory control register 1 (Note 1)	FMR1	0X00XX0X$_2$
01B6$_{16}$			
01B7$_{16}$	Flash memory control register 0 (Note 1)	FMR0	XX000001$_2$
01B8$_{16}$	Address match interrupt register 2	RMAD2	00$_{16}$
01B9$_{16}$			00$_{16}$
01BA$_{16}$			X0$_{16}$
01BB$_{16}$	Address match interrupt enable register 2	AIER2	XXXXXX00$_2$
01BC$_{16}$	Address match interrupt register 3	RMAD3	00$_{16}$
01BD$_{16}$			00$_{16}$
01BE$_{16}$			X0$_{16}$
01BF$_{16}$			

X: Undefined

Note 1: This register is included in flash memory version.
Note 2: The blank areas are reserved and cannot be accessed by users.

Figure 4.7 Location of Peripheral Function Control Registers and Value at After Reset (7)

Address	Register	Symbol	After reset
01C0₁₆	Timer B3,4,5 count start flag	TBSR	000XXXXX₂
01C1₁₆			
01C2₁₆	Timer A1-1 register	TA11	XX₁₆
01C3₁₆			XX₁₆
01C4₁₆	Timer A2-1 register	TA21	XX₁₆
01C5₁₆			XX₁₆
01C6₁₆	Timer A4-1 register	TA41	XX₁₆
01C7₁₆			XX₁₆
01C8₁₆	Three-phase PWM control register 0	INVC0	00₁₆
01C9₁₆	Three-phase PWM control register 1	INVC1	00₁₆
01CA₁₆	Three-phase output buffer register 0	IDB0	00₁₆
01CB₁₆	Three-phase output buffer register 1	IDB1	00₁₆
01CC₁₆	Dead time timer	DTT	XX₁₆
01CD₁₆	Timer B2 interrupt occurrence frequency set counter	ICTB2	XX₁₆
01CE₁₆			
01CF₁₆			
01D0₁₆	Timer B3 register	TB3	XX₁₆
01D1₁₆			XX₁₆
01D2₁₆	Timer B4 register	TB4	XX₁₆
01D3₁₆			XX₁₆
01D4₁₆	Timer B5 register	TB5	XX₁₆
01D5₁₆			XX₁₆
01D6₁₆			
01D7₁₆			
01D8₁₆			
01D9₁₆			
01DA₁₆			
01DB₁₆	Timer B3 mode register	TB3MR	00XX0000₂
01DC₁₆	Timer B4 mode register	TB4MR	00XX0000₂
01DD₁₆	Timer B5 mode register	TB5MR	00XX0000₂
01DE₁₆	Interrupt cause select register 0	IFSR0	00XXX000₂
01DF₁₆	Interrupt cause select register 1	IFSR1	00₁₆
01E0₁₆	SI/O3 transmit/receive register	S3TRR	XX₁₆
01E1₁₆			
01E2₁₆	SI/O3 control register	S3C	01000000₂
01E3₁₆	SI/O3 bit rate generator	S3BRG	XX₁₆
01E4₁₆			
01E5₁₆			
01E6₁₆			
01E7₁₆			
01E8₁₆			
01E9₁₆			
01EA₁₆			
01EB₁₆			
01EC₁₆	UART0 special mode register 4	U0SMR4	00₁₆
01ED₁₆	UART0 special mode register 3	U0SMR3	000X0X0X₂
01EE₁₆	UART0 special mode register 2	U0SMR2	X0000000₂
01EF₁₆	UART0 special mode register	U0SMR	X0000000₂
01F0₁₆	UART1 special mode register 4	U1SMR4	00₁₆
01F1₁₆	UART1 special mode register 3	U1SMR3	000X0X0X₂
01F2₁₆	UART1 special mode register 2	U1SMR2	X0000000₂
01F3₁₆	UART1 special mode register	U1SMR	X0000000₂
01F4₁₆	UART2 special mode register 4	U2SMR4	00₁₆
01F5₁₆	UART2 special mode register 3	U2SMR3	000X0X0X₂
01F6₁₆	UART2 special mode register 2	U2SMR2	X0000000₂
01F7₁₆	UART2 special mode register	U2SMR	X0000000₂
01F8₁₆	UART2 transmit/receive mode register	U2MR	00₁₆
01F9₁₆	UART2 bit rate generator	U2BRG	XX₁₆
01FA₁₆	UART2 transmit buffer register	U2TB	XX₁₆
01FB₁₆			XX₁₆
01FC₁₆	UART2 transmit/receive mode register 0	U2C0	00001000₂
01FD₁₆	UART2 transmit/receive mode register 1	U2C1	00000010₂
01FE₁₆	UART2 receive buffer register	U2RB	XX₁₆
01FF₁₆			XX₁₆

X: Undefined

Note: The blank areas are reserved and cannot be accessed by users.

Figure 4.8 Location of Peripheral Function Control Registers and Value at After Reset (8)

Address	Register	Symbol	After reset
0200_{16}	CAN0 message control register 0	C0MCTL0	00_{16}
0201_{16}	CAN0 message control register 1	C0MCTL1	00_{16}
0202_{16}	CAN0 message control register 2	C0MCTL2	00_{16}
0203_{16}	CAN0 message control register 3	C0MCTL3	00_{16}
0204_{16}	CAN0 message control register 4	C0MCTL4	00_{16}
0205_{16}	CAN0 message control register 5	C0MCTL5	00_{16}
0206_{16}	CAN0 message control register 6	C0MCTL6	00_{16}
0207_{16}	CAN0 message control register 7	C0MCTL7	00_{16}
0208_{16}	CAN0 message control register 8	C0MCTL8	00_{16}
0209_{16}	CAN0 message control register 9	C0MCTL9	00_{16}
$020A_{16}$	CAN0 message control register 10	C0MCTL10	00_{16}
$020B_{16}$	CAN0 message control register 11	C0MCTL11	00_{16}
$020C_{16}$	CAN0 message control register 12	C0MCTL12	00_{16}
$020D_{16}$	CAN0 message control register 13	C0MCTL13	00_{16}
$020E_{16}$	CAN0 message control register 14	C0MCTL14	00_{16}
$020F_{16}$	CAN0 message control register 15	C0MCTL15	00_{16}
0210_{16}	CAN0 control register	C0CTLR	$X0000001_2$
0211_{16}			$XX0X0000_2$
0212_{16}	CAN0 status register	C0STR	00_{16}
0213_{16}			$X0000001_2$
0214_{16}	CAN0 slot status register	C0SSTR	00_{16}
0215_{16}			00_{16}
0216_{16}	CAN0 interrupt control register	C0ICR	00_{16}
0217_{16}			00_{16}
0218_{16}	CAN0 extended register	C0IDR	00_{16}
0219_{16}			00_{16}
$021A_{16}$	CAN0 configuration register	C0CONR	XX_{16}
$021B_{16}$			XX_{16}
$021C_{16}$	CAN0 receive error count register	C0RECR	00_{16}
$021D_{16}$	CAN0 transmit error count register	C0TECR	00_{16}
$021E_{16}$	CAN0 time stamp register	C0TSR	00_{16}
$021F_{16}$			00_{16}
0220_{16}			
0221_{16}			
0222_{16}			
0223_{16}			
0224_{16}			
0225_{16}			
0226_{16}			
0227_{16}			
0228_{16}			
0229_{16}			
$022A_{16}$			
$022B_{16}$			
$022C_{16}$			
$022D_{16}$			
$022E_{16}$			
$022F_{16}$			
0230_{16}	CAN1 control register	C1CTLR	$X0000001_2$
0231_{16}			$XX0X0000_2$
0232_{16}			
0233_{16}			
0234_{16}			
0235_{16}			
0236_{16}			
0237_{16}			
0238_{16}			
0239_{16}			
$023A_{16}$			
$023B_{16}$			
$023C_{16}$			
$023D_{16}$			
$023E_{16}$			
$023F_{16}$			

X: Undefined

Note: The blank areas are reserved and cannot be accessed by users.

Figure 4.9 Location of Peripheral Function Control Registers and Value at After Reset (9)

Address	Register	Symbol	After reset
0240₁₆			
0241₁₆			
0242₁₆	CAN0 acceptance filter support register	C0AFS	XX₁₆
0243₁₆			XX₁₆
0244₁₆			
0245₁₆			
0246₁₆			
0247₁₆			
0248₁₆			
0249₁₆			
024A₁₆			
024B₁₆			
024C₁₆			
024D₁₆			
024E₁₆			
024F₁₆			
0250₁₆			
0251₁₆			
0252₁₆			
0253₁₆			
0254₁₆			
0255₁₆			
0256₁₆			
0257₁₆			
0258₁₆			
0259₁₆			
025A₁₆			
025B₁₆			
025C₁₆			
025D₁₆			
025E₁₆	Peripheral function clock select register	PCLKR	00₁₆
025F₁₆	CAN0 clock select register	CCLKR	00₁₆
0260₁₆			
0261₁₆			
0262₁₆			
0263₁₆			
0264₁₆			
0265₁₆			
0266₁₆			
0267₁₆			
0268₁₆			
0269₁₆			
026A₁₆			
026B₁₆			
026C₁₆			
026D₁₆			
026E₁₆			
026F₁₆			
0270₁₆			
≈			
0372₁₆			
0373₁₆			
0374₁₆			
0375₁₆			
0376₁₆			
0377₁₆			
0378₁₆			
0379₁₆			
037A₁₆			
037B₁₆			
037C₁₆			
037D₁₆			
037E₁₆			
037F₁₆			

X: Undefined

Note: The blank areas are reserved and cannot be accessed by users.

Figure 4.10 Location of Peripheral Function Control Registers and Value at After Reset (10)

Address	Register	Symbol	After reset
0380₁₆	Count start flag	TABSR	00₁₆
0381₁₆	Clock prescaler reset flag	CPSRF	0XXXXXXX₂
0382₁₆	One-shot start flag	ONSF	00₁₆
0383₁₆	Trigger select register	TRGSR	00₁₆
0384₁₆	Up-down flag	UDF	00₁₆
0385₁₆			
0386₁₆	Timer A0 register	TA0	XX₁₆
0387₁₆			XX₁₆
0388₁₆	Timer A1 register	TA1	XX₁₆
0389₁₆			XX₁₆
038A₁₆	Timer A2 register	TA2	XX₁₆
038B₁₆			XX₁₆
038C₁₆	Timer A3 register	TA3	XX₁₆
038D₁₆			XX₁₆
038E₁₆	Timer A4 register	TA4	XX₁₆
038F₁₆			XX₁₆
0390₁₆	Timer B0 register	TB0	XX₁₆
0391₁₆			XX₁₆
0392₁₆	Timer B1 register	TB1	XX₁₆
0393₁₆			XX₁₆
0394₁₆	Timer B2 register	TB2	XX₁₆
0395₁₆			XX₁₆
0396₁₆	Timer A0 mode register	TA0MR	00₁₆
0397₁₆	Timer A1 mode register	TA1MR	00₁₆
0398₁₆	Timer A2 mode register	TA2MR	00₁₆
0399₁₆	Timer A3 mode register	TA3MR	00₁₆
039A₁₆	Timer A4 mode register	TA4MR	00₁₆
039B₁₆	Timer B0 mode register	TB0MR	00XX0000₂
039C₁₆	Timer B1 mode register	TB1MR	00XX0000₂
039D₁₆	Timer B2 mode register	TB2MR	00XX0000₂
039E₁₆	Timer B2 special mode register	TB2SC	XXXXXX00₂
039F₁₆			
03A0₁₆	UART0 transmit/receive mode register	U0MR	00₁₆
03A1₁₆	UART0 bit rate generator	U0BRG	XX₁₆
03A2₁₆	UART0 transmit buffer register	U0TB	XX₁₆
03A3₁₆			XX₁₆
03A4₁₆	UART0 transmit/receive control register 0	U0C0	00001000₂
03A5₁₆	UART0 transmit/receive control register 1	U0C1	00000010₂
03A6₁₆	UART0 receive buffer register	U0RB	XX₁₆
03A7₁₆			XX₁₆
03A8₁₆	UART1 transmit/receive mode register	U1MR	00₁₆
03A9₁₆	UART1 bit rate generator	U1BRG	XX₁₆
03AA₁₆	UART1 transmit buffer register	U1TB	XX₁₆
03AB₁₆			XX₁₆
03AC₁₆	UART1 transmit/receive control register 0	U1C0	00001000₂
03AD₁₆	UART1 transmit/receive control register 1	U1C1	00000010₂
03AE₁₆	UART1 receive buffer register	U1RB	XX₁₆
03AF₁₆			XX₁₆
03B0₁₆	UART transmit/receive control register 2	UCON	X0000000₂
03B1₁₆			
03B2₁₆			
03B3₁₆			
03B4₁₆			
03B5₁₆			
03B6₁₆			
03B7₁₆			
03B8₁₆	DMA0 request cause select register	DM0SL	00₁₆
03B9₁₆			
03BA₁₆	DMA1 request cause select register	DM1SL	00₁₆
03BB₁₆			
03BC₁₆	CRC data register	CRCD	XX₁₆
03BD₁₆			XX₁₆
03BE₁₆	CRC input register	CRCIN	XX₁₆
03BF₁₆			

X: Undefined

Note: The blank areas are reserved and cannot be accessed by users.

Figure 4.11 Location of Peripheral Function Control Registers and Value at After Reset (11)

Address	Register	Symbol	After reset
03C0$_{16}$	A-D register 0	AD0	XX$_{16}$
03C1$_{16}$			XX$_{16}$
03C2$_{16}$	A-D register 1	AD1	XX$_{16}$
03C3$_{16}$			XX$_{16}$
03C4$_{16}$	A-D register 2	AD2	XX$_{16}$
03C5$_{16}$			XX$_{16}$
03C6$_{16}$	A-D register 3	AD3	XX$_{16}$
03C7$_{16}$			XX$_{16}$
03C8$_{16}$	A-D register 4	AD4	XX$_{16}$
03C9$_{16}$			XX$_{16}$
03CA$_{16}$	A-D register 5	AD5	XX$_{16}$
03CB$_{16}$			XX$_{16}$
03CC$_{16}$	A-D register 6	AD6	XX$_{16}$
03CD$_{16}$			XX$_{16}$
03CE$_{16}$	A-D register 7	AD7	XX$_{16}$
03CF$_{16}$			XX$_{16}$
03D0$_{16}$			
03D1$_{16}$			
03D2$_{16}$			
03D3$_{16}$			
03D4$_{16}$	A-D control register 2	ADCON2	00$_{16}$
03D5$_{16}$			
03D6$_{16}$	A-D control register 0	ADCON0	00000XXX$_2$
03D7$_{16}$	A-D control register 1	ADCON1	00$_{16}$
03D8$_{16}$	D-A register 0	DA0	XX$_{16}$
03D9$_{16}$			
03DA$_{16}$	D-A register 1	DA1	XX$_{16}$
03DB$_{16}$			
03DC$_{16}$	D-A control register	DACON	00$_{16}$
03DD$_{16}$			
03DE$_{16}$			
03DF$_{16}$			
03E0$_{16}$	Port P0 register	P0	XX$_{16}$
03E1$_{16}$	Port P1 register	P1	XX$_{16}$
03E2$_{16}$	Port P0 direction register	PD0	00$_{16}$
03E3$_{16}$	Port P1 direction register	PD1	00$_{16}$
03E4$_{16}$	Port P2 register	P2	XX$_{16}$
03E5$_{16}$	Port P3 register	P3	XX$_{16}$
03E6$_{16}$	Port P2 direction register	PD2	00$_{16}$
03E7$_{16}$	Port P3 direction register	PD3	00$_{16}$
03E8$_{16}$	Port P4 register	P4	XX$_{16}$
03E9$_{16}$	Port P5 register	P5	XX$_{16}$
03EA$_{16}$	Port P4 direction register	PD4	00$_{16}$
03EB$_{16}$	Port P5 direction register	PD5	00$_{16}$
03EC$_{16}$	Port P6 register	P6	XX$_{16}$
03ED$_{16}$	Port P7 register	P7	XX$_{16}$
03EE$_{16}$	Port P6 direction register	PD6	00$_{16}$
03EF$_{16}$	Port P7 direction register	PD7	00$_{16}$
03F0$_{16}$	Port P8 register	P8	XX$_{16}$
03F1$_{16}$	Port P9 register	P9	XX$_{16}$
03F2$_{16}$	Port P8 direction register	PD8	00X00000$_2$
03F3$_{16}$	Port P9 direction register	PD9	00$_{16}$
03F4$_{16}$	Port P10 register	P10	XX$_{16}$
03F5$_{16}$			
03F6$_{16}$	Port P10 direction register	PD10	00$_{16}$
03F7$_{16}$			
03F8$_{16}$			
03F9$_{16}$			
03FA$_{16}$			
03FB$_{16}$			
03FC$_{16}$	Pull-up control register 0	PUR0	00$_{16}$
03FD$_{16}$	Pull-up control register 1	PUR1	00000000$_2$ (Note 1) 00000010$_2$
03FE$_{16}$	Pull-up control register 2	PUR2	00$_{16}$
03FF$_{16}$	Port control register	PCR	00$_{16}$

X: Undefined

Note 1: At hardware reset, the register is as follows:
- "00000000$_2$" where "L" is input to the CNVss pin
- "00000010$_2$" where "H" is input to the CNVss pin

At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:
- "00000000$_2$" where the PM01 to PM00 bits in the PM0 register are "00$_2$" (single-chip mode)
- "00000010$_2$" where the PM01 to PM00 bits in the PM0 register are "01$_2$" (memory expansion mode) or "11$_2$" (microprocessor mode)

Note 2: The blank areas are reserved and cannot be accessed by users.

Figure 4.12 Location of Peripheral Function Control Registers and Value at After Reset (12)

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated value	Unit
V_{CC1}	Supply voltage		V_{CC1}=AV_{CC}	–0.3 to 6.5	V
V_{CC2}	Supply voltage		V_{CC2}	–0.3<V_{CC2}=V_{CC1}	V
AV_{CC}	Analog supply voltage		V_{CC1}=AV_{CC}	–0.3 to 6.5	V
V_I	Input voltage	$\overline{RESET}$, CNV_{SS}, BYTE, $P6_0$~$P6_7$, $P7_0$, $P7_2$~$P7_7$, $P8_0$~$P8_7$, $P9_0$, $P9_2$~$P9_7$, $P10_0$~$P10_7$, V_{REF}, X_{IN}		–0.3 to V_{CC1}+0.3	V
		$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$		–0.3 to V_{CC2}+0.3	V
		$P7_1$, $P9_1$		–0.3 to 6.5	V
V_O	Output voltage	$P6_0$~$P6_7$, $P7_0$, $P7_2$~$P7_7$, $P8_0$~$P8_4$, $P8_6$, $P8_7$, $P9_0$, $P9_2$~$P9_7$, $P10_0$~$P10_7$, X_{OUT}		–0.3 to V_{CC1}+0.3	V
		$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$		–0.3 to V_{CC2}+0.3	V
		$P7_1$, $P9_1$		–0.3 to 6.5	V
P_d	Power dissipation		T_{opr}=25°C	700	mW
T_{opr}	Operating ambient temperature			–40 to 85/–40 to 125 (option)	°C
T_{stg}	Storage temperature			–65 to 150	°C

option: If you desire this option, please so specify.

Table 5.2 Recommended Operating Conditions (Note 1)

Symbol	Parameter				Standard			Unit
					Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply voltage (V_{CC1}=V_{CC2})				4.2	5.0	5.5	V
AV_{CC}	Analog supply voltage					V_{CC}		V
V_{SS}	Supply voltage					0		V
AV_{SS}	Analog supply voltage					0		V
V_{IH}	HIGH input voltage	$P3_1$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$, $P7_2$~$P7_7$, $P8_0$~$P8_7$, $P9_0$, $P9_2$~$P9_7$, $P10_0$~$P10_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE			0.8V_{CC}		V_{CC}	V
		$P7_1$, $P9_1$			0.8V_{CC}		6.5	V
		$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$ (During single-chip mode)			0.8V_{CC}		V_{CC}	V
		$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$ (Data input during memory expansion and microprocessor modes)			0.5V_{CC}		V_{CC}	V
V_{IL}	LOW input voltage	$P3_1$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_7$, $P9_0$~$P9_7$, $P10_0$~$P10_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE			0		0.2V_{CC}	V
		$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$ (During single-chip mode)			0		0.2V_{CC}	V
		$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$ (Data input during memory expansion and microprocessor modes)			0		0.16V_{CC}	V
$I_{OH\ (peak)}$	HIGH peak output current	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$, $P7_2$~$P7_7$, $P8_0$~$P8_4$, $P8_6$, $P8_7$, $P9_0$, $P9_2$~$P9_7$, $P10_0$~$P10_7$					–10.0	mA
$I_{OH\ (avg)}$	HIGH average output current	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$, $P7_2$~$P7_7$, $P8_0$~$P8_4$, $P8_6$, $P8_7$, $P9_0$, $P9_2$~$P9_7$, $P10_0$~$P10_7$					–5.0	mA
$I_{OL\ (peak)}$	LOW peak output current	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_4$, $P8_6$, $P8_7$, $P9_0$~$P9_7$, $P10_0$~$P10_7$					10.0	mA
$I_{OL\ (avg)}$	LOW average output current	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_4$, $P8_6$, $P8_7$, $P9_0$~$P9_7$, $P10_0$~$P10_7$					5.0	mA
$f(X_{IN})$	Main clock input oscillation frequency (Notes 4, 5 and 6)	No wait	Mask ROM version Flash memory version	V_{CC}=4.2 to 5.5V	0		16	MHz
$f(X_{CIN})$	Sub clock oscillation frequency					32.768	50	kHz
f(Ring)	Ring oscillation frequency					1		MHz
f(PLL)	PLL clock oscillation frequency						20	MHz
f(BCLK)	CPU operation clock			V_{CC}=4.2 to 5.5V	0		20	MHz
t_{su}(PLL)	PLL frequency synthesizer stabilization wait time						20	ms

Note 1: Referenced to V_{CC} = 4.2 to 5.5 V at Topr = –40 to 85 °C unless otherwise specified.
Note 2: The mean output current is the mean value within 100 ms.
Note 3: The total I_{OL} (peak) for ports P0, P1, P2, $P8_6$, $P8_7$, P9 and P10 must be 80mA max. The total I_{OL} (peak) for ports P3, P4, P5, P6, P7 and $P8_0$ to $P8_4$ must be 80mA max. The total I_{OH} (peak) for ports P0, P1, and P2 must be –40mA max. The total I_{OH} (peak) for ports P3, P4 and P5 must be –40mA max. The total I_{OH} (peak) for ports P6, P7 and $P8_0$ to $P8_4$ must be –40mA max. The total I_{OH} (peak) for ports $P8_6$, $P8_7$, P9 and P10 must be –40mA max.
Note 4: Relationship between main clock oscillation frequency and supply voltage is shown right.
Note 5: Execute program /erase of flash memory by V_{CC} = 5.0 ± 0.5 V.
Note 6: When using 16 MHz or more, use PLL clock.

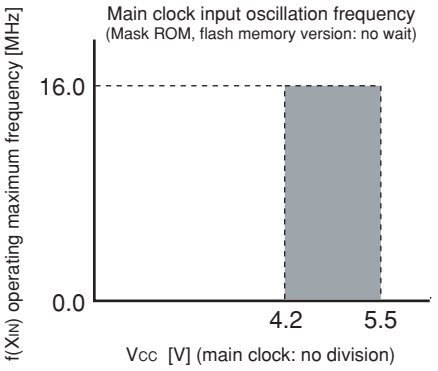


Table 5.3 Electrical Characteristics (Note 1)

Symbol	Parameter			Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
V_{OH}	HIGH output voltage	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$, $P7_2$~$P7_7$, $P8_0$~$P8_4$, $P8_6$, $P8_7$, $P9_0$, $P9_2$~$P9_7$, $P10_0$~$P10_7$		I_{OH}=–5mA		V_{CC}-2.0		V_{CC}	V
V_{OH}	HIGH output voltage	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$, $P7_2$~$P7_7$, $P8_0$~$P8_4$, $P8_6$, $P8_7$, $P9_0$, $P9_2$~$P9_7$, $P10_0$~$P10_7$		I_{OH}=–200µA		V_{CC}-0.3		V_{CC}	V
V_{OH}	HIGH output voltage	X_{OUT}	HIGHPOWER	I_{OH}=–1mA		3.0		V_{CC}	V
			LOWPOWER	I_{OH}=–0.5mA		3.0		V_{CC}	
	HIGH output voltage	X_{COUT}	HIGHPOWER	With no load applied			2.5		V
			LOWPOWER	With no load applied			1.6		
V_{OL}	LOW output voltage	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_4$, $P8_6$, $P8_7$, $P9_0$~$P9_7$, $P10_0$~$P10_7$		I_{OL}=5mA				2.0	V
V_{OL}	LOW output voltage	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_4$, $P8_6$, $P8_7$, $P9_0$~$P9_7$, $P10_0$~$P10_7$		I_{OL}=200µA				0.45	V
V_{OL}	LOW output voltage	X_{OUT}	HIGHPOWER	I_{OL}=1mA				2.0	V
			LOWPOWER	I_{OL}=0.5mA				2.0	
	LOW output voltage	X_{COUT}	HIGHPOWER	With no load applied			0		V
			LOWPOWER	With no load applied			0		
V_{T+}–V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$~$TA4_{IN}$, $TB0_{IN}$~$TB5_{IN}$, $\overline{INT_0}$~$\overline{INT_5}$, NMI, $\overline{ADTRG}$, $\overline{CTS_0}$~$\overline{CTS_2}$, SCL, SDA, CLK_0~CLK_4, $TA2_{OUT}$~$TA4_{OUT}$, KI_0~KI_3, RxD_0~RxD_2, S_{IN3}				0.2		1.0	V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$				0.2		2.2	V
I_{IH}	HIGH input current	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_3$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_7$, $P9_0$~$P9_7$, $P10_0$~$P10_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		V_I=5V				5.0	µA
I_{IL}	LOW input current	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_3$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_7$, $P9_0$~$P9_7$, $P10_0$~$P10_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		V_I=0V				–5.0	µA
R_{PULLUP}	Pull-up resistance	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$, $P7_2$~$P7_7$, $P8_0$~$P8_4$, $P8_6$, $P8_7$, $P9_0$, $P9_2$~$P9_7$, $P10_0$~$P10_7$		V_I=0V		30	50	170	kΩ
R_{fXIN}	Feedback resistance	X_{IN}					1.5		MΩ
R_{fXCIN}	Feedback resistance	X_{CIN}					15		MΩ
V_{RAM}	RAM retention voltage			At stop mode		2.0			V
I_{CC}	Power supply current (V_{CC} = 4.2 to 5.5V)	In single-chip mode, the output pins are open and other pins are V_{SS}.		Mask ROM	f(BCLK)=20MHz, No division, PLL operation		16	28	mA
					No division, Ring oscillation		1		mA
				Flash memory	f(BCLK)=20MHz, No division, PLL operation		18	30	mA
					No division, Ring oscillation		1.8		mA
				Flash memory Program	f(BCLK)=10MHz, V_{CC}=5V		15		mA
				Flash memory Erase	f(BCLK)=10MHz, V_{CC}=5V		25		mA
				Mask ROM	f(X_{CIN})=32kHz, Low power dissipation mode, ROM (Note 2)		25		µA
				Flash memory	f(BCLK)=32kHz, Low power dissipation mode, RAM (Note 2)		25		µA
					f(BCLK)=32kHz, Low power dissipation mode, Flash memory (Note 2)		420		µA
				Mask ROM	Ring oscillation, Wait mode		50		µA
				Flash memory	f(BCLK)=32kHz, Wait mode (Note 3), Oscillation capacity High		8.5		µA
					f(BCLK)=32kHz, Wait mode (Note 3), Oscillation capacity Low		3.0		µA
					Stop mode, T_{opr} = 25 °C		0.8	3.0	µA

Note 1: Referenced to V_{CC} = 4.2 to 5.5 V, Vss = 0 V at Topr = –40 to 85 °C, f(BCLK) = 20 MHz unless otherwise specified.

Note 2: This indicates the memory in which the program to be executed exists.

Note 3: With one timer operated using f_{C32}.

Table 5.4 A-D Conversion Characteristics (Note 1)

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		$V_{REF}=V_{CC}$				10	Bits
INL	Integral non-linearity error	10 bits	$V_{REF}=V_{CC}$ =5V	ANEX0, ANEX1 input, AN_0 to AN_7 input, AN_{00} to AN_{07} input, AN_{20} to AN_{27} input			±3	LSB
				External operation amp connection mode			±7	LSB
		8 bits	$V_{REF}=AV_{CC}=V_{CC}$=5V				±2	LSB
–	Absolute accuracy	10 bits	$V_{REF}=V_{CC}$ =5V	ANEX0, ANEX1 input, AN_0 to AN_7 input, AN_{00} to AN_{07} input, AN_{20} to AN_{27} input			±3	LSB
				External operation amp connection mode			±7	LSB
		8 bits	$V_{REF}=AV_{CC}=V_{CC}$=5V				±2	LSB
DNL	Differential non-linearity error						±1	LSB
–	Offset error						±3	LSB
–	Gain error						±3	LSB
R_{LADDER}	Ladder resistance		$V_{REF}=V_{CC}$		10		40	kΩ
t_{CONV}	Conversion time (10 bits), Sample & hold function available		$V_{REF}=V_{CC}$=5V, ϕ_{AD}=10MHz		3.3			µs
	Conversion time (8 bits), Sample & hold function available		$V_{REF}=V_{CC}$=5V, ϕ_{AD}=10MHz		2.8			µs
t_{SAMP}	Sampling time				0.3			µs
V_{REF}	Reference voltage				2.0		V_{CC}	V
V_{IA}	Analog input voltage				0		V_{REF}	V

Note 1: Referenced to V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V, –40 to 85 °C unless otherwise specified.
Note 2: AD operation clock frequency (ϕ_{AD} frequency) must be 10 MHz or less.
Note 3: A case without sample & hold function turn ϕ_{AD} frequency into 250 kHz or more in addition to a limit of Note 2.
A case with sample & hold function turn ϕ_{AD} frequency into 1 MHz or more in addition to a limit of Note 2.

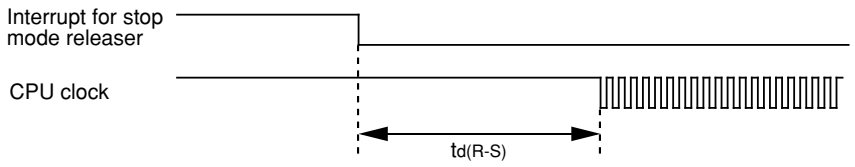
Table 5.5 D-A conversion Characteristics (Note 1)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
t_{su}	Setup time				3	µs
R_O	Output resistance		4	10	20	kΩ
I_{VREF}	Reference power supply input current	(Note 2)			1.5	mA

Note 1: Referenced to V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V, –40 to 85 °C unless otherwise specified.
Note 2: This applies when using one D-A converter, with the DAi register (i = 0, 1) for the unused D-A converter set to "00_{16}". The A-D converter's ladder resistance is not included. Also, the current I_{VREF} always flows even though V_{REF} may have been set to be unconnected by the ADCON1 register.

Table 5.6 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on	V_{CC} = 4.2 to 5.5 V			2	ms
$t_{d(R-S)}$	STOP release time				150	µs
$t_{d(W-S)}$	Low power dissipation mode wait mode release time				150	µs
$t_{d(M-L)}$	Time for internal power supply stabilization when main clock oscillation status				50	µs



Timing Requirements

(Referenced to V_{CC} = 5 V, V_{SS} = 0 V, at Topr = –40 to 85 °C unless otherwise specified)

Table 5.7 External Clock Input (X_{IN} Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	62.5		ns
$t_{w(H)}$	External clock input HIGH pulse width	25		ns
$t_{w(L)}$	External clock input LOW pulse width	25		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

Table 5.8 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data input access time (for setting with wait)		(Note 2)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplexed bus area)		(Note 3)	ns
$t_{su(DB-RD)}$	Data input setup time	40		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	30		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ input setup time	40		ns
$t_{h(RD-DB)}$	Data input hold time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time		40	ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45 \text{ [ns]}$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 45 \text{ [ns]}$$

n is “2” for 1-wait setting, “3” for 2-wait setting and “4” for 3-wait setting.

Note 3: Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 45 \text{ [ns]}$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

Timing Requirements

(Referenced to V_{CC} = 5 V, V_{SS} = 0 V, at Topr = –40 to 85 °C unless otherwise specified)

Table 5.9 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	100		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	40		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	40		ns

Table 5.10 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	400		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	200		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	200		ns

Table 5.11 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	200		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	100		ns

Table 5.12 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	100		ns

Table 5.13 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} input cycle time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} input HIGH pulse width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} input LOW pulse width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} input setup time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} input hold time	400		ns

Table 5.14 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAi_{OUT} input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAi_{IN} input setup time	200		ns

Timing Requirements

(Referenced to V_{CC} = 5 V, V_{SS} = 0 V, at Topr = –40 to 85 °C unless otherwise specified)

Table 5.15 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width (counted on both edges)	80		ns

Table 5.16 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	400		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width	200		ns

Table 5.17 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	400		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width	200		ns

Table 5.18 A-D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(AD)}$	$\overline{ADTRG}$ input cycle time (trigger able minimum)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW pulse width	125		ns

Table 5.19 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK_i input cycle time	200		ns
$t_{w(CKH)}$	CLK_i input HIGH pulse width	100		ns
$t_{w(CKL)}$	CLK_i input LOW pulse width	100		ns
$t_{d(C-Q)}$	TxD_i output delay time		80	ns
$t_{h(C-Q)}$	TxD_i hold time	0		ns
$t_{su(D-C)}$	RxD_i input setup time	30		ns
$t_{h(C-D)}$	RxD_i input hold time	90		ns

Table 5.20 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input HIGH pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input LOW pulse width	250		ns

Switching Characteristics

(Referenced to V_{CC} = 5 V, V_{SS} = 0 V, at Topr = –40 to 85 °C unless otherwise specified)

Table 5.21 Memory Expansion Mode and Microprocessor Mode (for setting with no wait)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 5.1		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK) (Note 3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR) (Note 3)		(Note 1)		ns

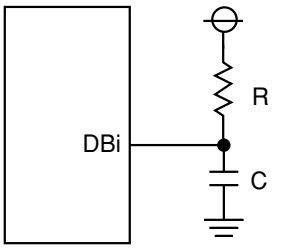
Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \text{ [ns]}$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 \text{ [ns]}$$ f(BCLK) is 12.5 MHz or less.

Note 3: This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln (1 - V_{OL} / V_{CC})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2\ V_{CC}$, C = 30 pF,
R = 1 kΩ, hold time of output "L" level is
$t = -30\ pF \times 1\ k\Omega \times \ln (1 - 0.2\ V_{CC} / V_{CC}) = 6.7$ ns.



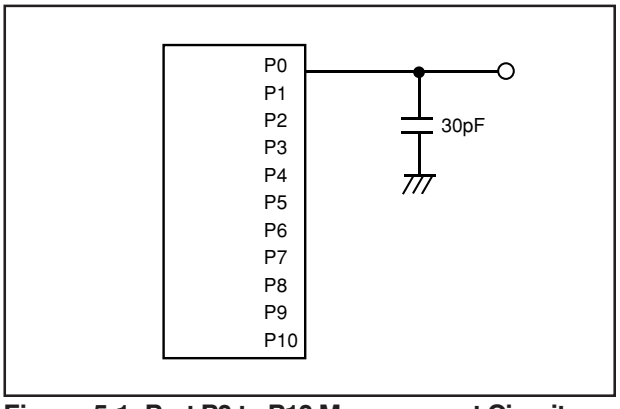


Figure 5.1 Port P0 to P10 Measurement Circuit

Switching Characteristics

(Referenced to V_{CC} = 5 V, V_{SS} = 0 V, at Topr = –40 to 85 °C unless otherwise specified)

Table 5.22 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 5.1		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK) (Note 3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR) (Note 3)		(Note 1)		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \text{ [ns]}$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 40 \text{ [ns]}$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
When n = 1, f(BCLK) is 12.5 MHz or less.

Note 3: This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in

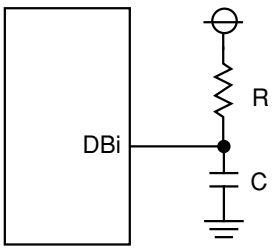
$t = -CR \times \ln (1 - V_{OL} / V_{CC})$

by a circuit of the right figure.

For example, when V_{OL} = 0.2 V_{CC}, C = 30 pF,

R =1 kΩ, hold time of output “L” level is

$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln (1 - 0.2 V_{CC} / V_{CC}) = 6.7 \text{ ns}$.



Switching Characteristics

(Referenced to V_{CC} = 5 V, V_{SS} = 0 V, at Topr = –40 to 85 °C unless otherwise specified)

Table 5.23 Memory Expansion Mode and Microprocessor Mode (for 2- to 3-wait setting, external area access and multiplexed bus selection)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 5.1		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{h(RD-CS)}$	Chip select output hold time (refers to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (refers to BCLK)			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (refers to BCLK)		–4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (refers to Address)		(Note 3)		ns
$t_{h(ALE-AD)}$	ALE signal output hold time (refers to Address)		(Note 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of Address		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of Address		0		ns
$t_{dZ(RD-AD)}$	Address output floating start time			8	ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \text{ [ns]}$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 40 \text{ [ns]}$$ n is “2” for 2-wait setting, “3” for 3-wait setting.

Note 3: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 25 \text{ [ns]}$$

Note 4: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 15 \text{ [ns]}$$

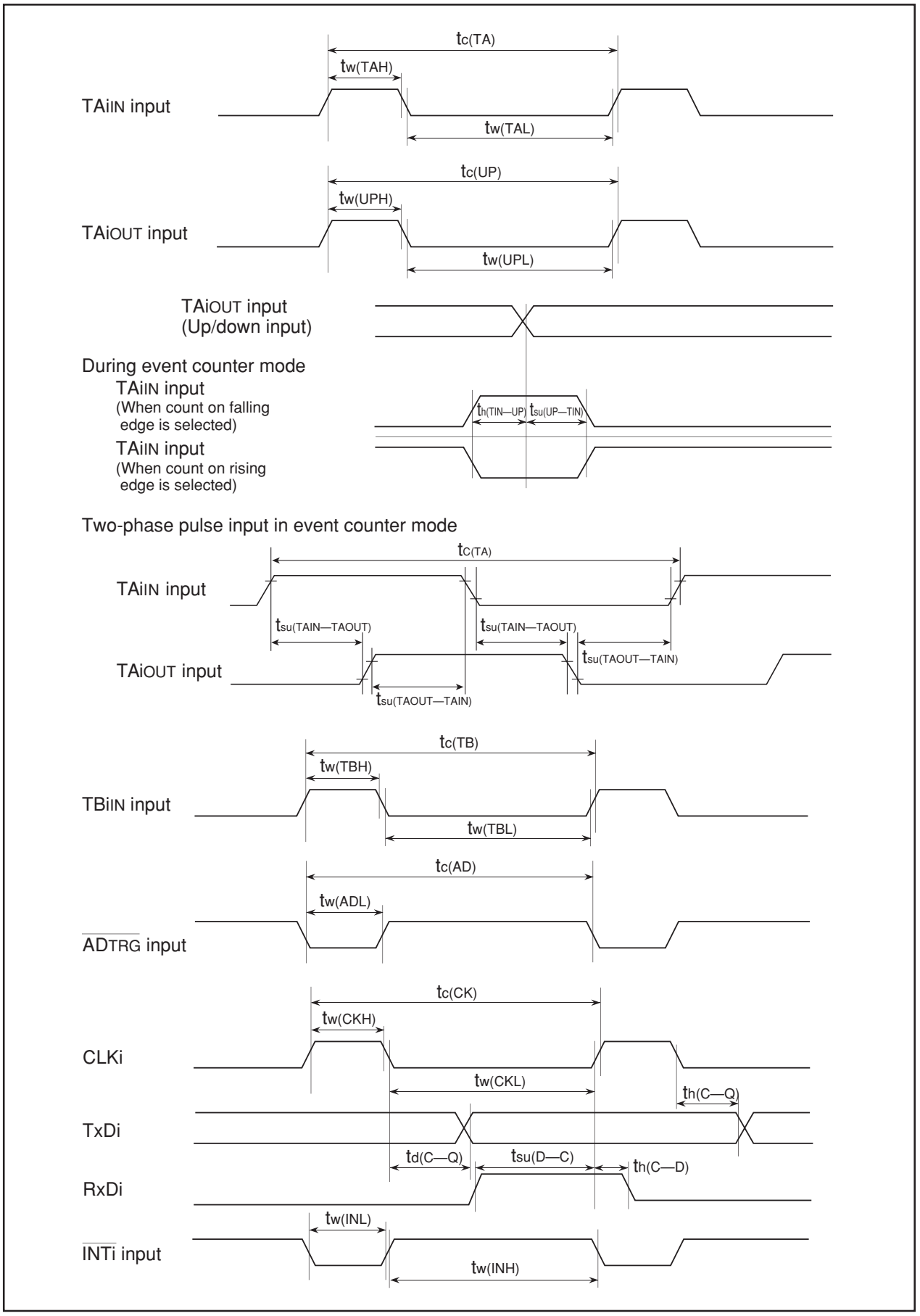
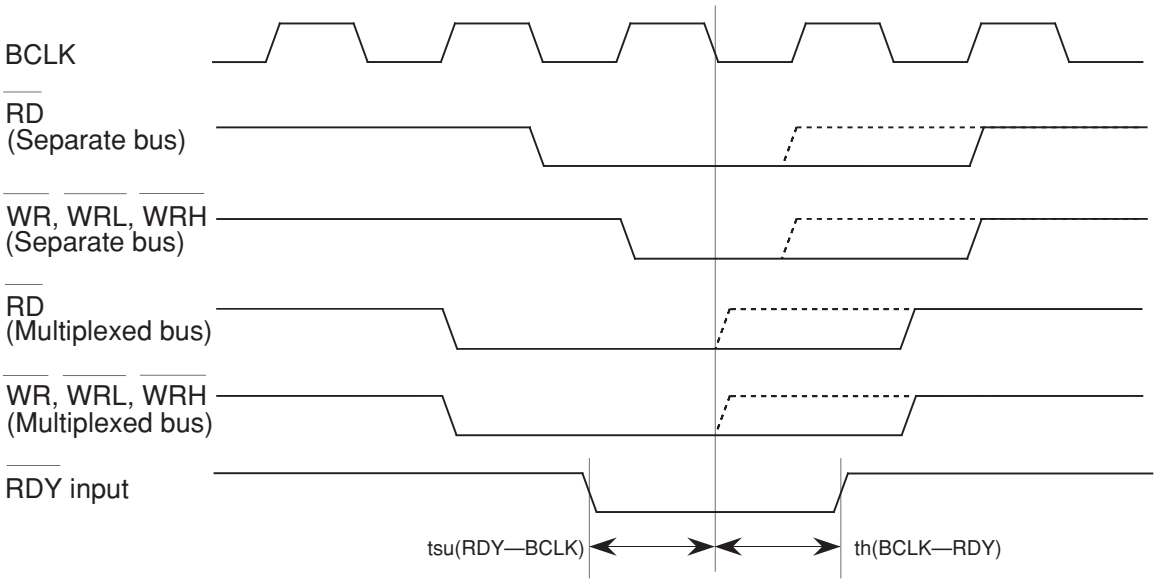


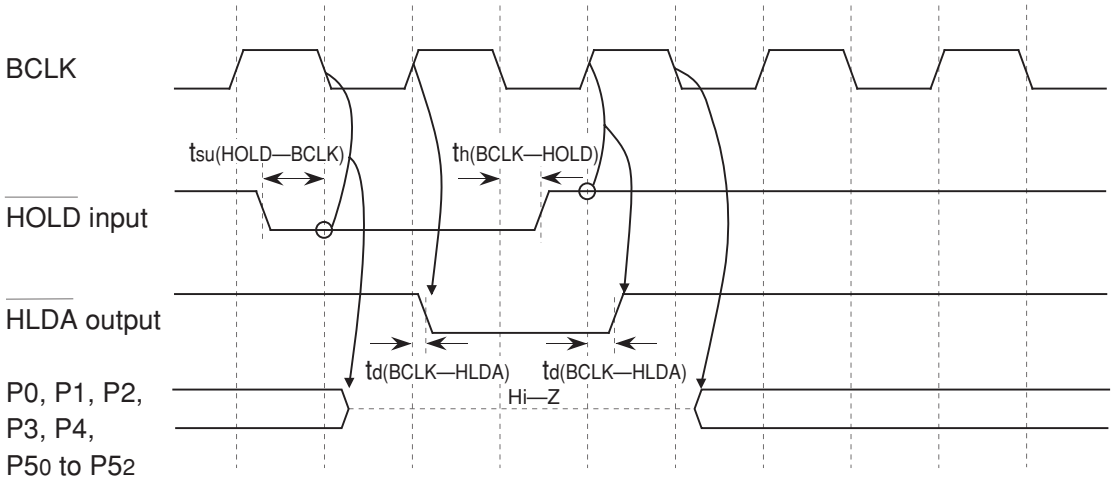
Figure 5.2 Timing Diagram (1)

Memory Expansion Mode and Microprocessor Mode

(Effective for setting with wait)



(Common to setting with wait and setting without wait)



Note: The above pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit of PM0 register and PM11 bit of PM1 register.

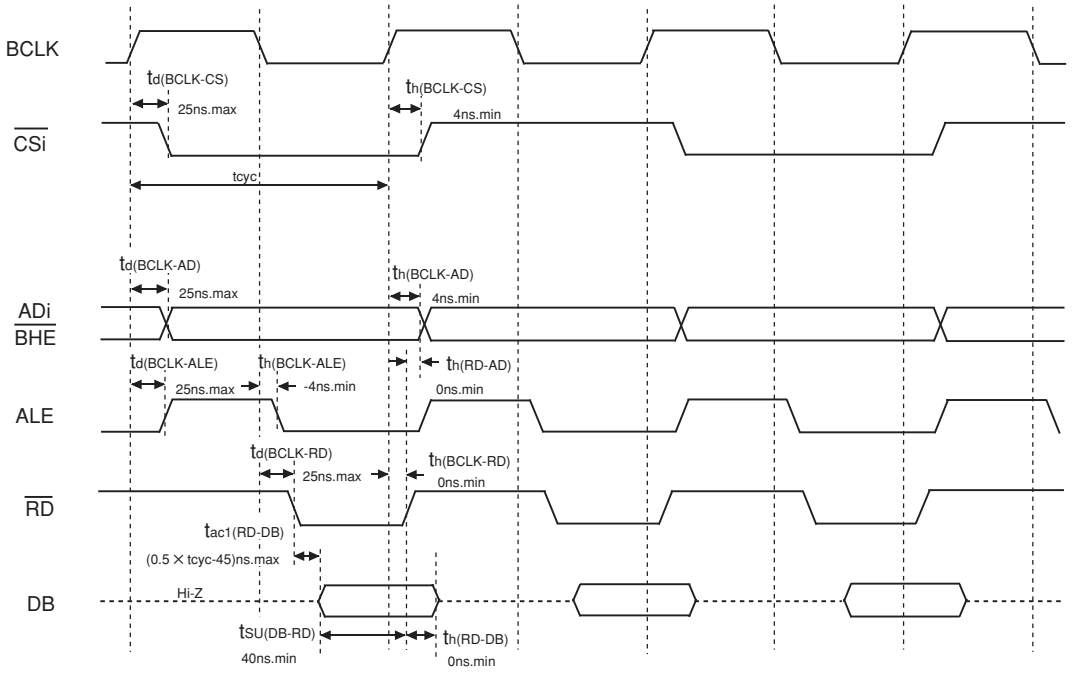
Measuring conditions :
- V_{CC} = 5 V
- Input timing voltage : Determined with V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage: Determined with V_{OL} = 2.5 V, V_{OH} = 2.5 V

Figure 5.3 Timing Diagram (2)

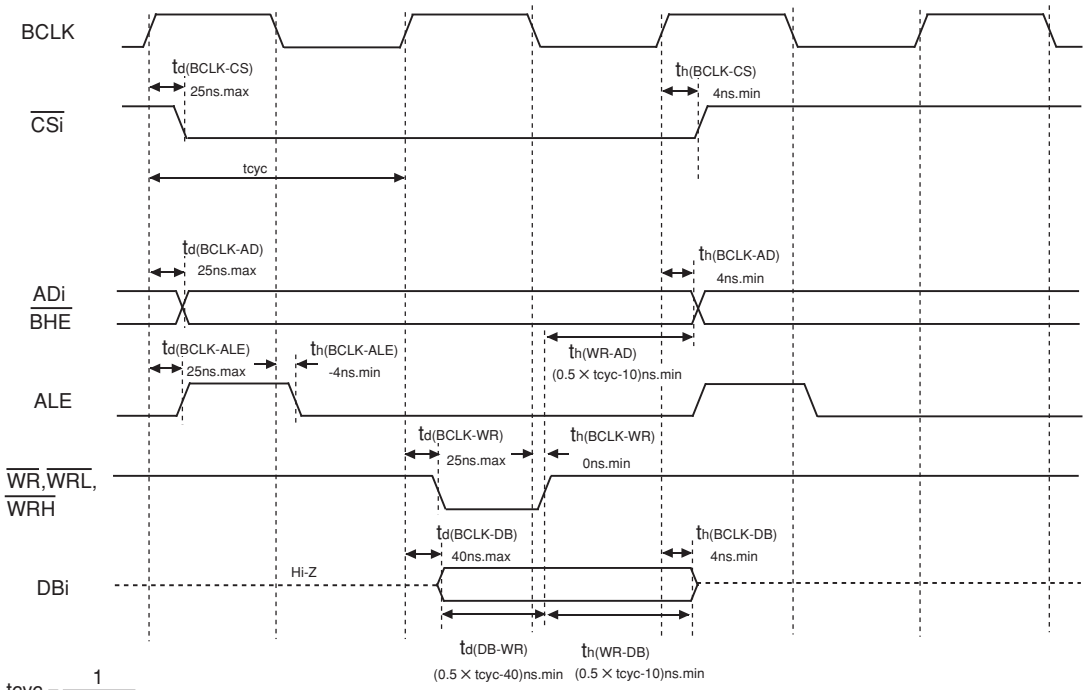
Memory Expansion Mode and Microprocessor Mode

(For setting with no wait)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

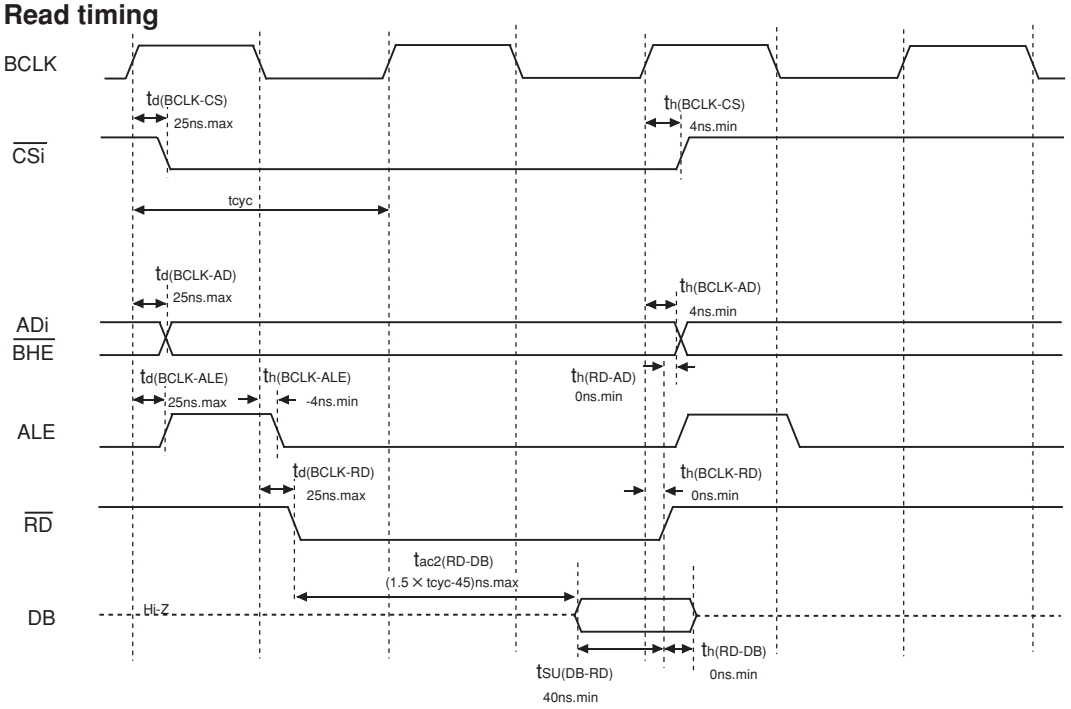
- V_{CC} = 5 V
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Output timing voltage : V_{OL} = 0.4 V, V_{OH} = 2.4 V

Figure 5.4 Timing Diagram (3)

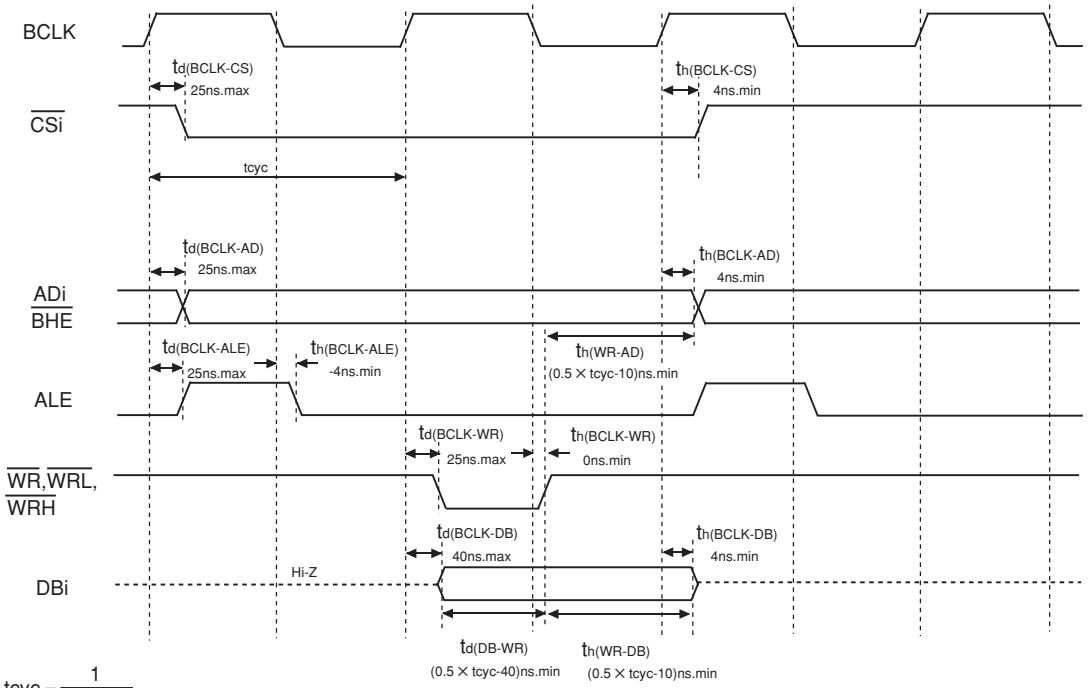
Memory Expansion Mode and Microprocessor Mode

(For 1-wait setting and external area access)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

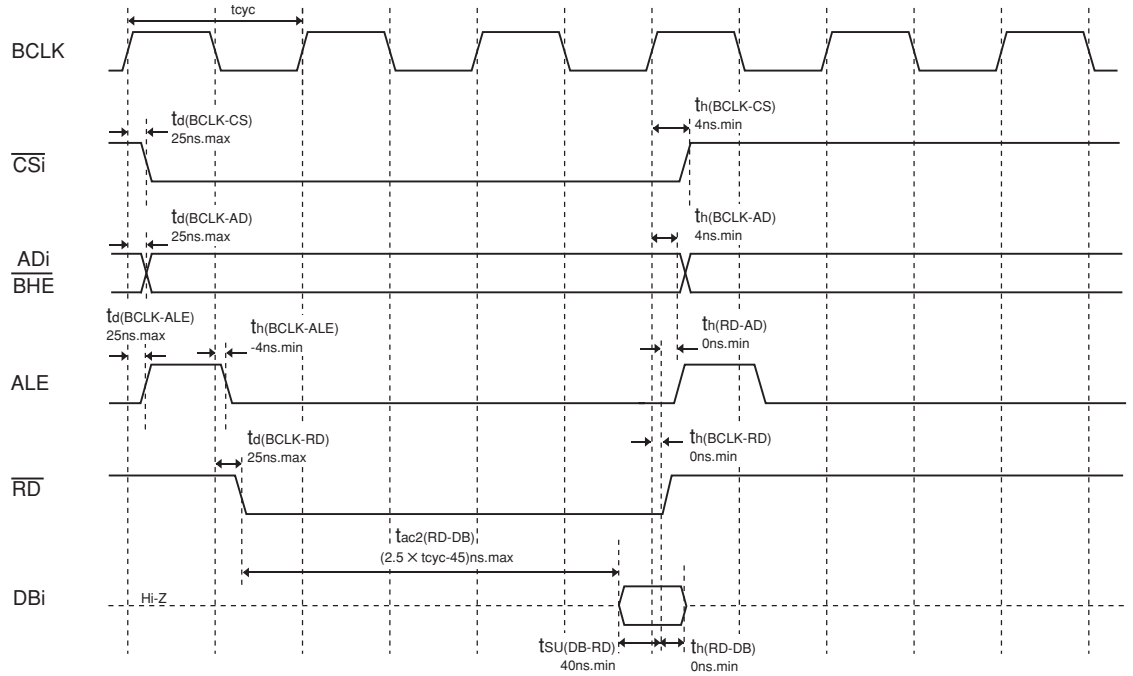
- V_{CC} = 5 V
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Output timing voltage : V_{OL} = 0.4 V, V_{OH} = 2.4 V

Figure 5.5 Timing Diagram (4)

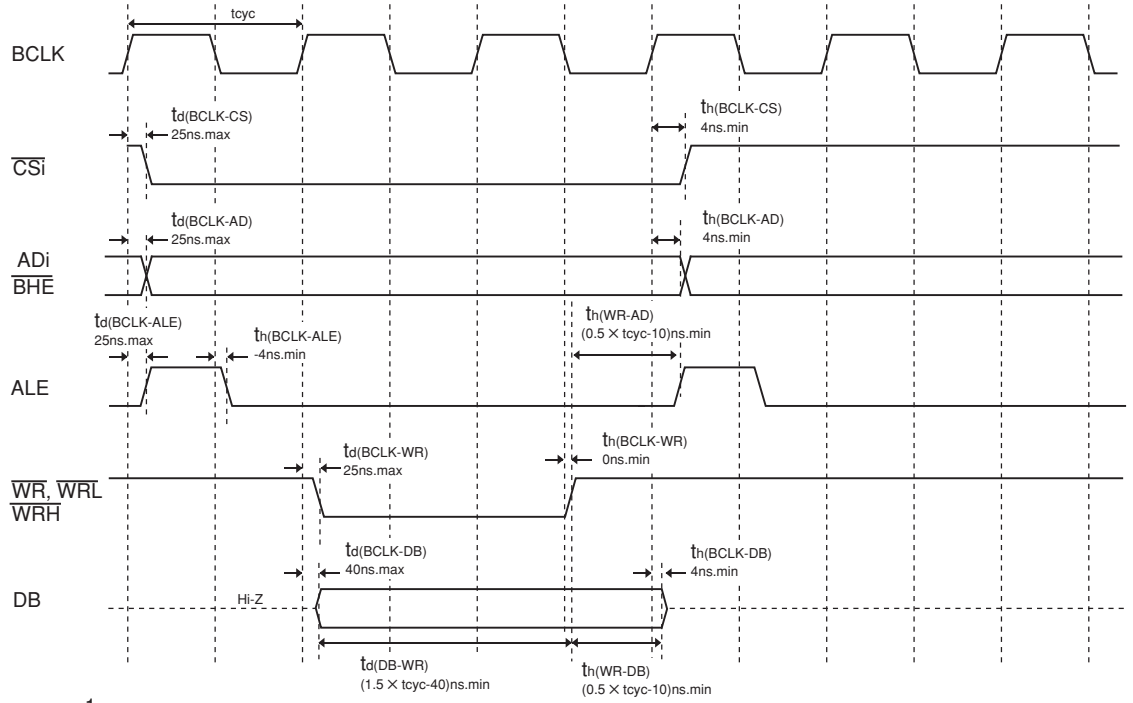
Memory Expansion Mode and Microprocessor Mode

(For 2-wait setting and external area access)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

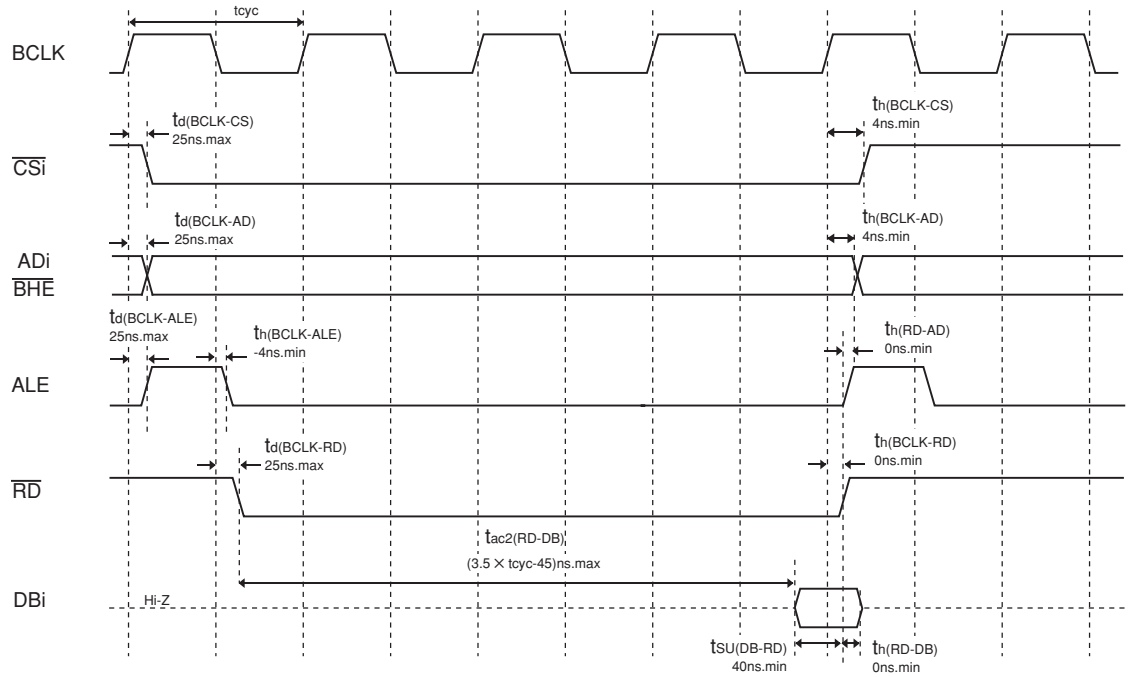
- V_{CC} = 5 V
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Output timing voltage : V_{OL} = 0.4 V, V_{OH} = 2.4 V

Figure 5.6 Timing Diagram (5)

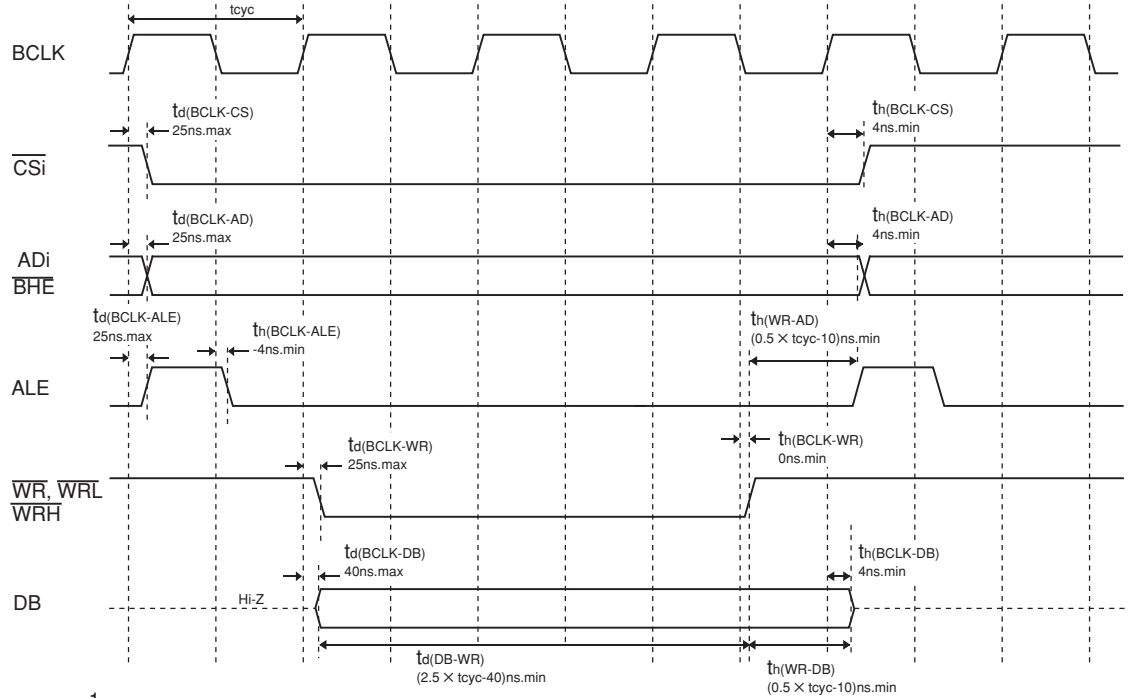
Memory Expansion Mode and Microprocessor Mode

(For 3-wait setting and external area access)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

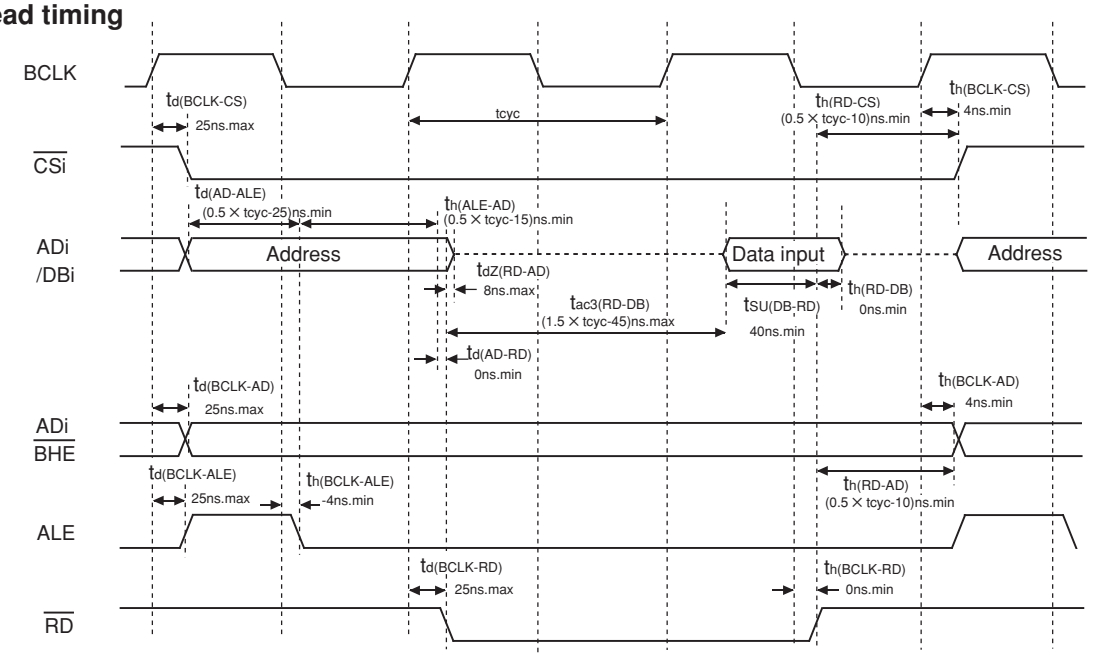
- V_{CC} = 5 V
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Output timing voltage : V_{OL} = 0.4 V, V_{OH} = 2.4 V

Figure 5.7 Timing Diagram (6)

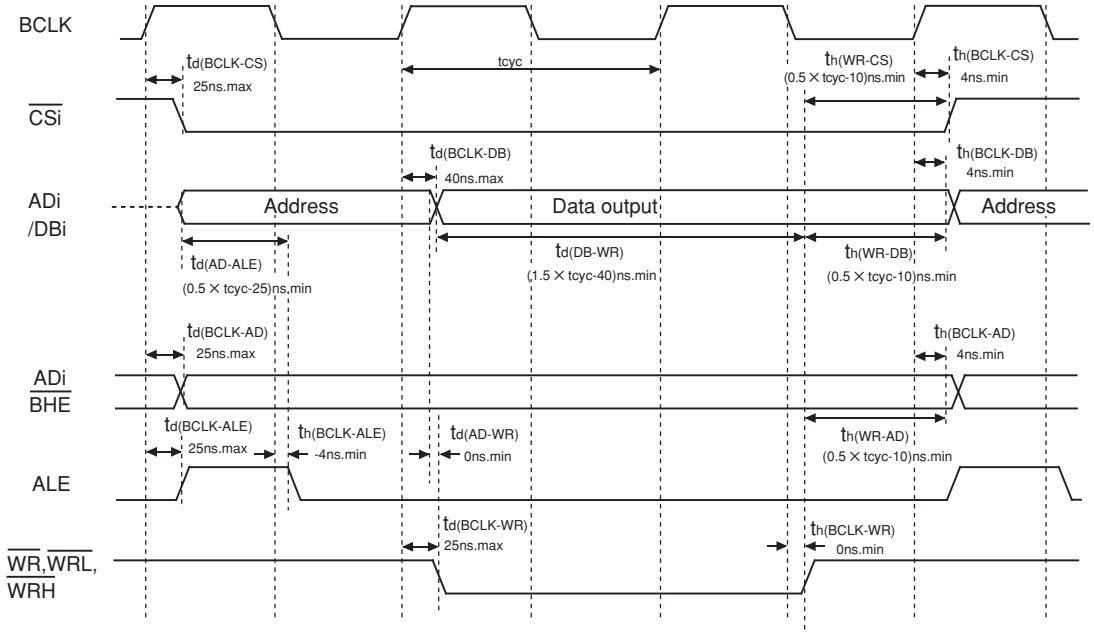
Memory Expansion Mode and Microprocessor Mode

(For 1- or 2-wait setting, external area access and multiplexed bus selection)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

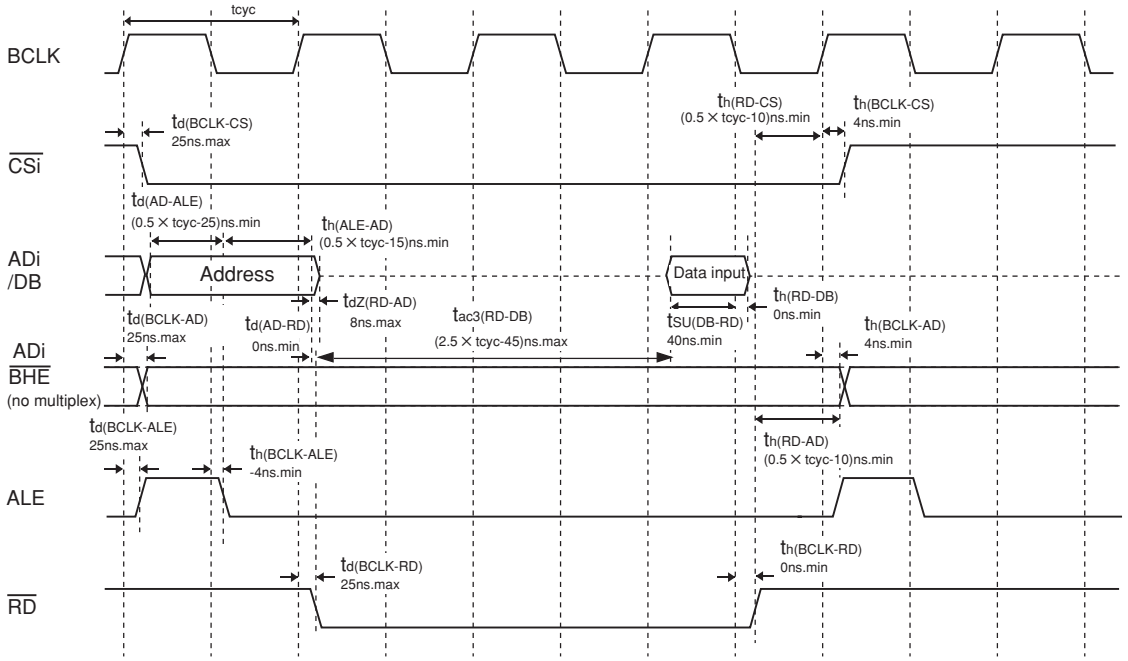
- V_{CC} = 5 V
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Output timing voltage : V_{OL} = 0.4 V, V_{OH} = 2.4 V

Figure 5.8 Timing Diagram (7)

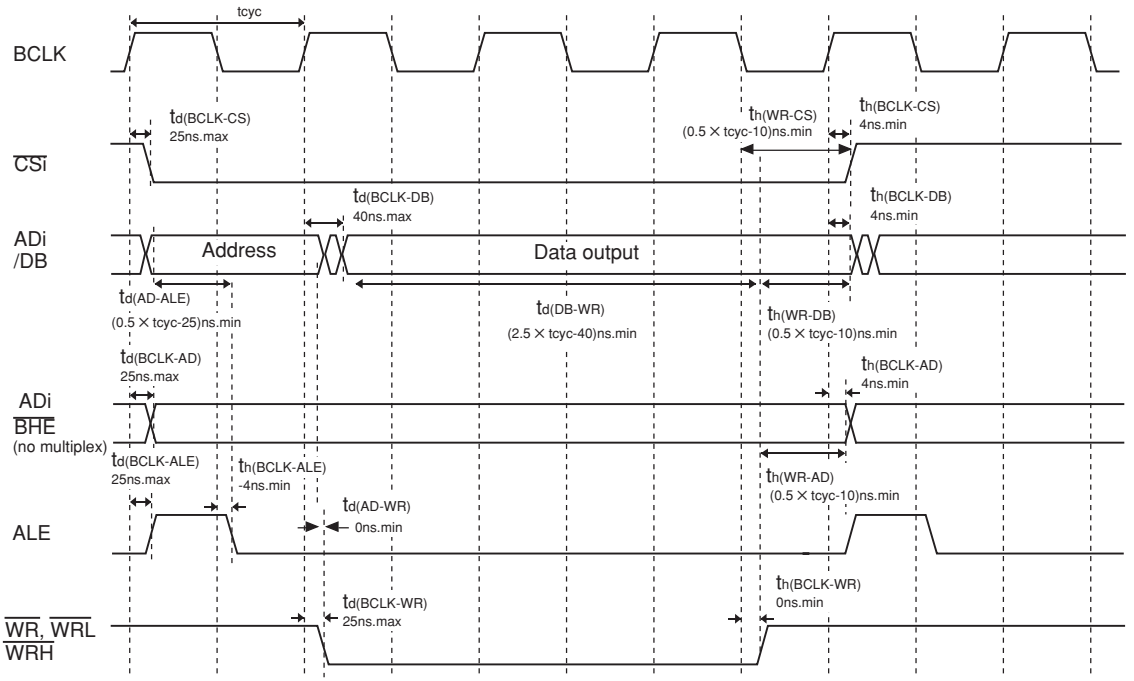
Memory Expansion Mode and Microprocessor Mode

(For 3-wait setting, external area access and multiplexed bus selection)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

- V_{CC} = 5 V
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Output timing voltage : V_{OL} = 0.4 V, V_{OH} = 2.4 V

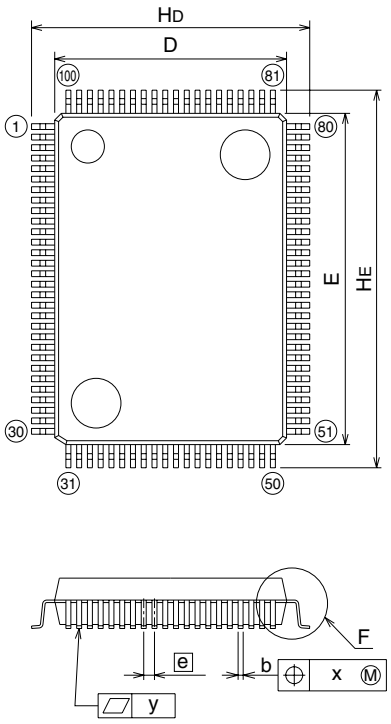
Figure 5.9 Timing Diagram (8)

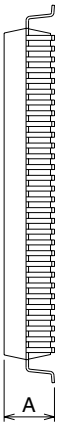
Package Dimension

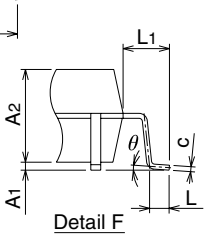
100P6S-A (MMP)

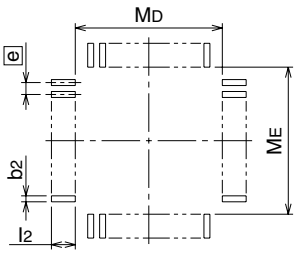
Plastic 100pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	–	1.58	Alloy 42









Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A_1	0	0.1	0.2
A_2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L_1	–	1.4	–
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.35	–
l_2	1.3	–	–
MD	–	14.6	–
ME	–	20.6	–

REVISION HISTORY	M16C/6N5 Group Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 30, 2003	–	First edition issued

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