

## 1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

### 1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

## 1.2 Performance Outline

Table 1.1. lists the performance outline of this MCU.

**Table 1.1 Performance outline**

Item		Performance
CPU	Number of basic instructions	89 instructions
	Shortest instruction execution time	50 ns ( $f(X_{IN}) = 20$ MHz, $V_{CC} = 3.0$ to 5.5 V) 100 ns ( $f(X_{IN}) = 10$ MHz, $V_{CC} = 2.7$ to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2.
Peripheral function	Interrupt	Internal: 10 sources, External: 5 sources, Software: 4 sources, Priority level: 7 levels
	Watchdog timer	15 bits x 1 (with prescaler)
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel Circuits of input capture and output compare.
	Serial I/O	•1 channel Clock synchronous, UART •1 channel UART
	A-D converter	10-bit A-D converter: 1 circuit, 12 channels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •Ring oscillator (high speed, low speed) On High-speed ring oscillator the frequency adjustment function is usable.
	Oscillation stop detection function	Stop detection of main clock oscillation
	Voltage detection circuit	Included
	Power on reset circuit	Included
	Port	Input/Output: 22 (including LED drive port), Input: 2 (LED drive I/O port: 8, max. 20 mA)
Electrical characteristics	Power supply voltage	$V_{CC} = 3.0$ to 5.5 V ( $f(X_{IN}) = 20$ MHz) $V_{CC} = 2.7$ to 5.5 V ( $f(X_{IN}) = 10$ MHz)
	Power consumption	Typ. 9 mA ( $V_{CC} = 5.0$ V, ( $f(X_{IN}) = 20$ MHz, High-speed mode) Typ. 5 mA ( $V_{CC} = 3.0$ V, ( $f(X_{IN}) = 10$ MHz, High-speed mode) Typ. 35 $\mu$ A ( $V_{CC} = 3.0$ V, Wait mode, Peripheral clock off) Typ. 0.7 $\mu$ A ( $V_{CC} = 3.0$ V, Stop mode)
Flash memory	Program/erase voltage	$V_{CC} = 2.7$ to 5.5 V
	Number of program/erase	100 times
Operating ambient temperature		-20 to 85 °C -40 to 85 °C (option)
Package		32-pin plastic mold LQFP

Option: If you require this option, please specify so.

### 1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

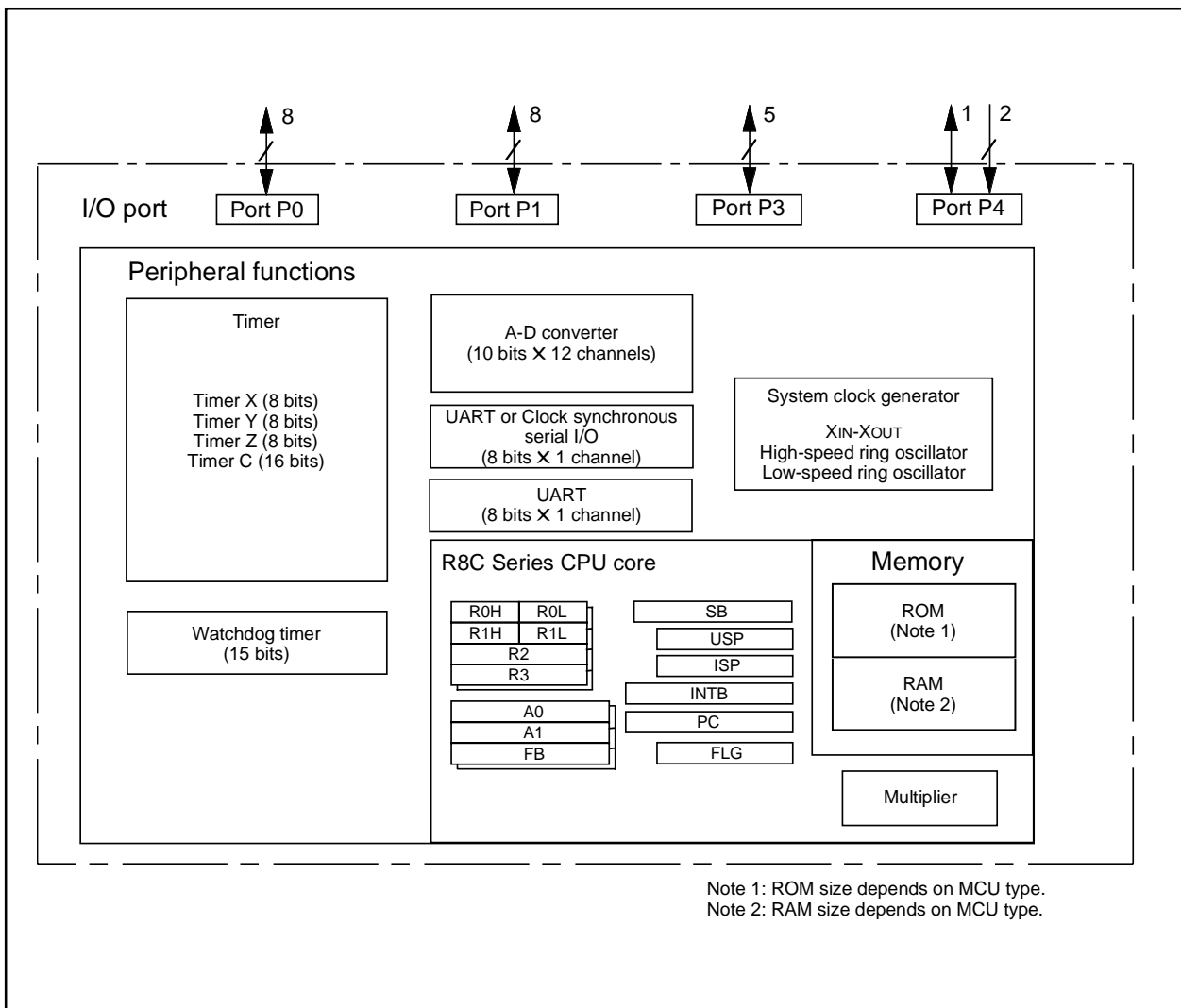


Figure 1.1 Block Diagram

### 1.4 Product List

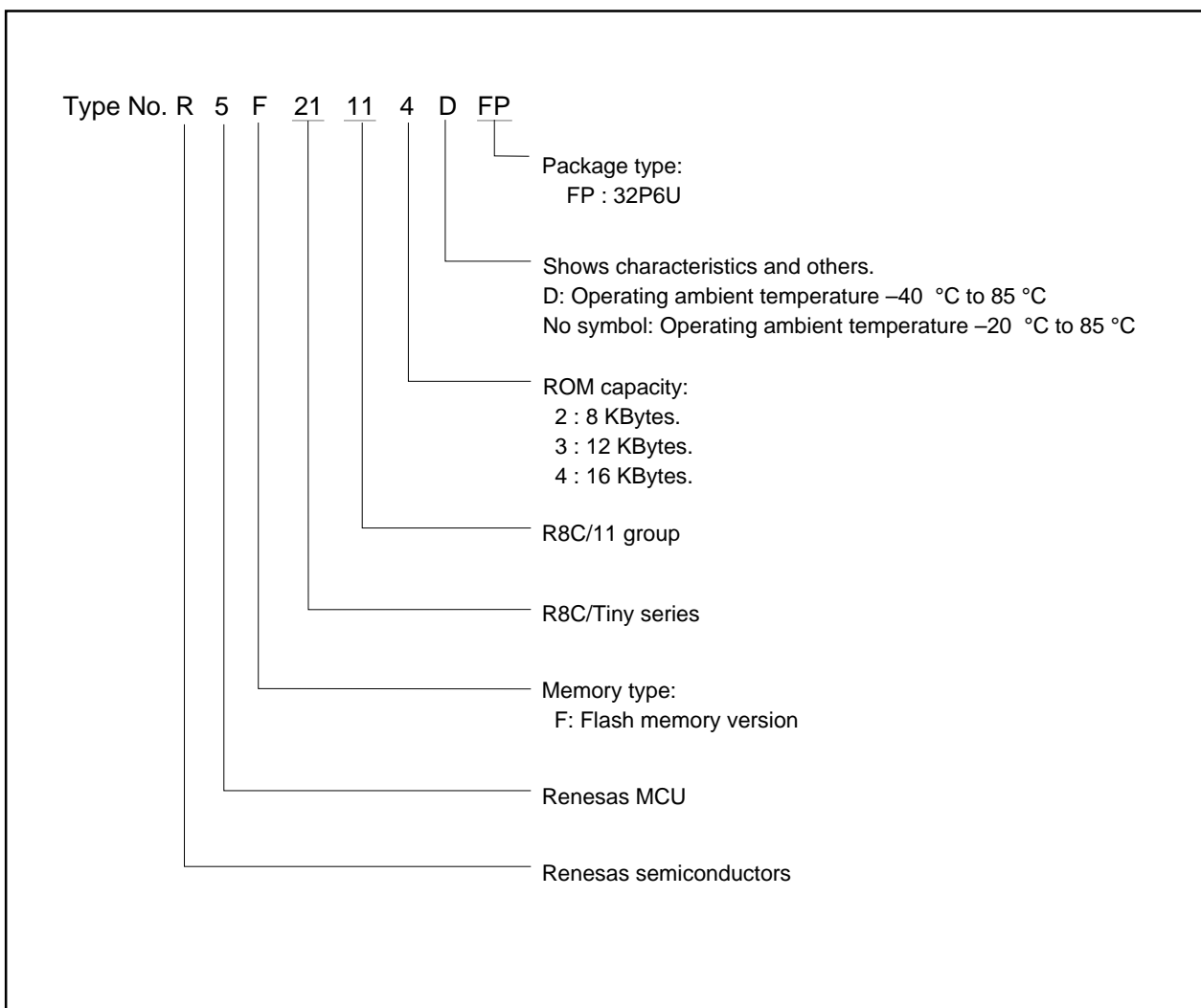
Table 1.2 lists the products.

**Table 1.2 Product List**

As of Oct. 2003

Type No.		ROM capacity	RAM capacity	Package type	Remarks
R5F21112FP	**	8K bytes	512 bytes	32P6U-A	Flash memory version
R5F21113FP	**	12K bytes	768 bytes	32P6U-A	
R5F21114FP	**	16K bytes	1K bytes	32P6U-A	
R5F21112DFP	**	8K bytes	512 bytes	32P6U-A	D version
R5F21113DFP	**	12K bytes	768 bytes	32P6U-A	
R5F21114DFP	**	16K bytes	1K bytes	32P6U-A	

\*\* : Under development



**Figure 1.2 Type No., Memory Size, and Package**

## 1.5 Pin Configuration

Figure 1.3 shows the pin configuration (top view).

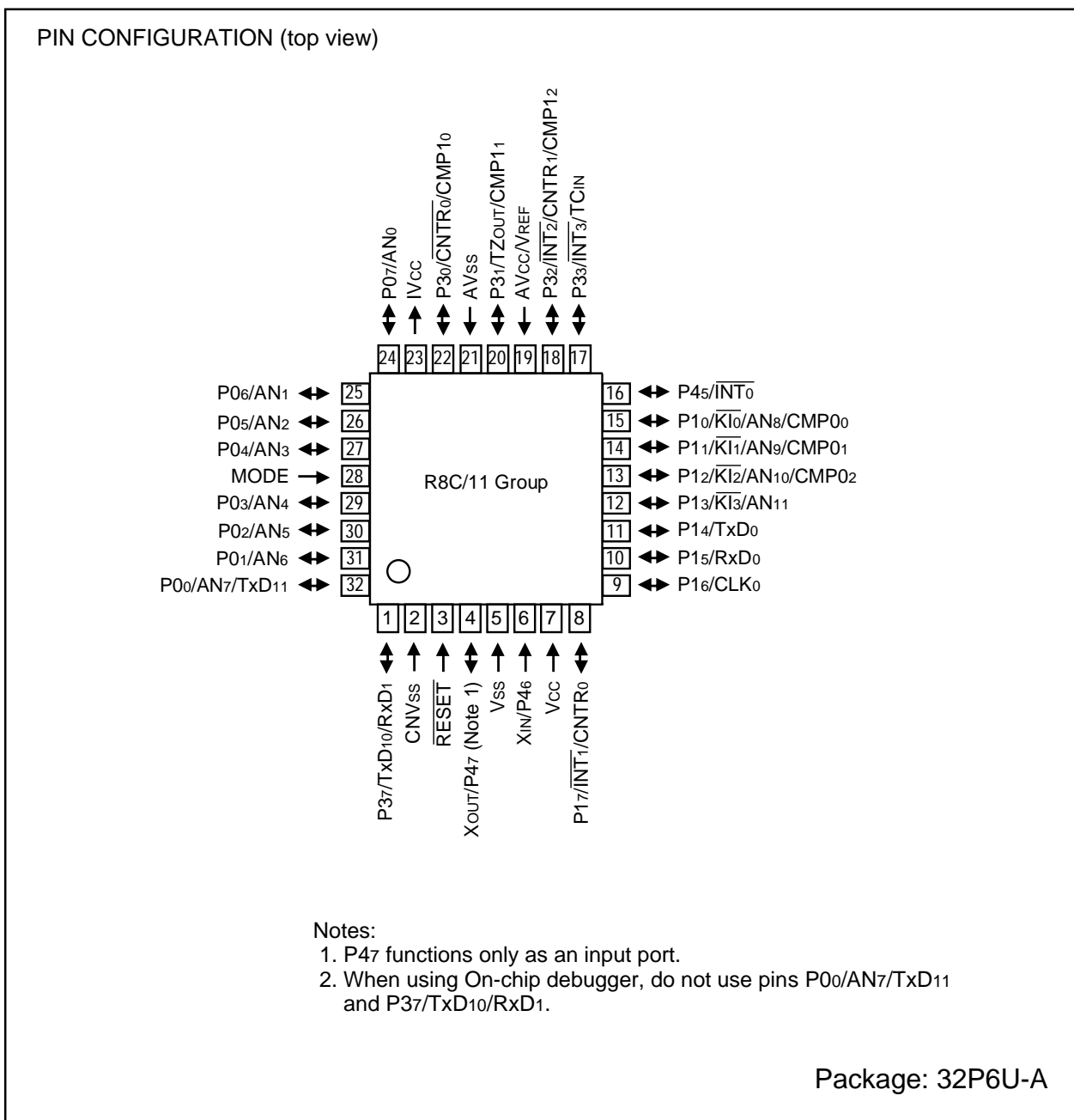


Figure 1.3 Pin Configuration (Top View)

Notes:

1. P47 functions only as an input port.
2. When using On-chip debugger, do not use pins P00/AN7/TxD11 and P37/TxD10/RxD1.

## 1.6 Pin Description

Table 1.3 shows the pin description

**Table 1.3 Pin description**

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	Input	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	Output	Connect this pin to Vss via a capacitor (0.1 $\mu$ F).
Analog power supply input	AVcc, AVss	Input	These are power supply input pins for A-D converter. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	RESET	Input	"L" on this input resets the MCU.
CNVss	CNVss	Input	Connect this pin to Vss via a resistor.
MODE	MODE	Input	Connect this pin to Vcc via a resistor.
Main clock input	XIN	Input	These pins are provided for the main clock generating circuit input/output. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	Output	
INT interrupt input	INT $\bar{0}$ to INT $\bar{3}$	Input	These are INT interrupt input pins.
Key input interrupt input	KI $\bar{0}$ to KI $\bar{3}$	Input	These are key input interrupt input pins.
Timer X	CNTR $\bar{0}$	Input/Output	This is the timer X I/O pin.
	CNTR $\bar{0}$	Output	This is the timer X output pin.
Timer Y	CNTR $\bar{1}$	Input/Output	This is the timer Y I/O pin.
Timer Z	TZOUT	Output	This is the timer Z output pin.
Timer C	TCIN	Input	This is the timer C input pin.
	CMP $\bar{0}$ to CMP $\bar{0}$ $\bar{3}$ , CMP $\bar{1}$ $\bar{0}$ to CMP $\bar{1}$ $\bar{3}$	Output	These are the timer C output pins.
Serial interface	CLK $\bar{0}$	Input/Output	This is a transfer clock I/O pin.
	RxD $\bar{0}$ , RxD $\bar{1}$	Input	These are serial data input pins.
	TxD $\bar{0}$ , TxD $\bar{1}$ $\bar{0}$ , TxD $\bar{1}$ $\bar{1}$	Output	These are serial data output pins.
Reference voltage input	VREF	Input	This is a reference voltage input pin for A-D converter.
A-D converter	AN $\bar{0}$ to AN $\bar{1}$ $\bar{1}$	Input	These are analog input pins for A-D converter.
I/O port	P $\bar{0}$ to P $\bar{0}$ $\bar{7}$ , P $\bar{1}$ $\bar{0}$ to P $\bar{1}$ $\bar{7}$ , P $\bar{3}$ $\bar{0}$ to P $\bar{3}$ $\bar{3}$ , P $\bar{3}$ $\bar{7}$ , P $\bar{4}$ $\bar{5}$	Input/Output	These are 8-bit CMOS I/O ports. Each port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P $\bar{1}$ $\bar{0}$ to P $\bar{1}$ $\bar{7}$ also function as LED drive ports.
Input port	P $\bar{4}$ $\bar{6}$ , P $\bar{4}$ $\bar{7}$	Input	These are input only pins.

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

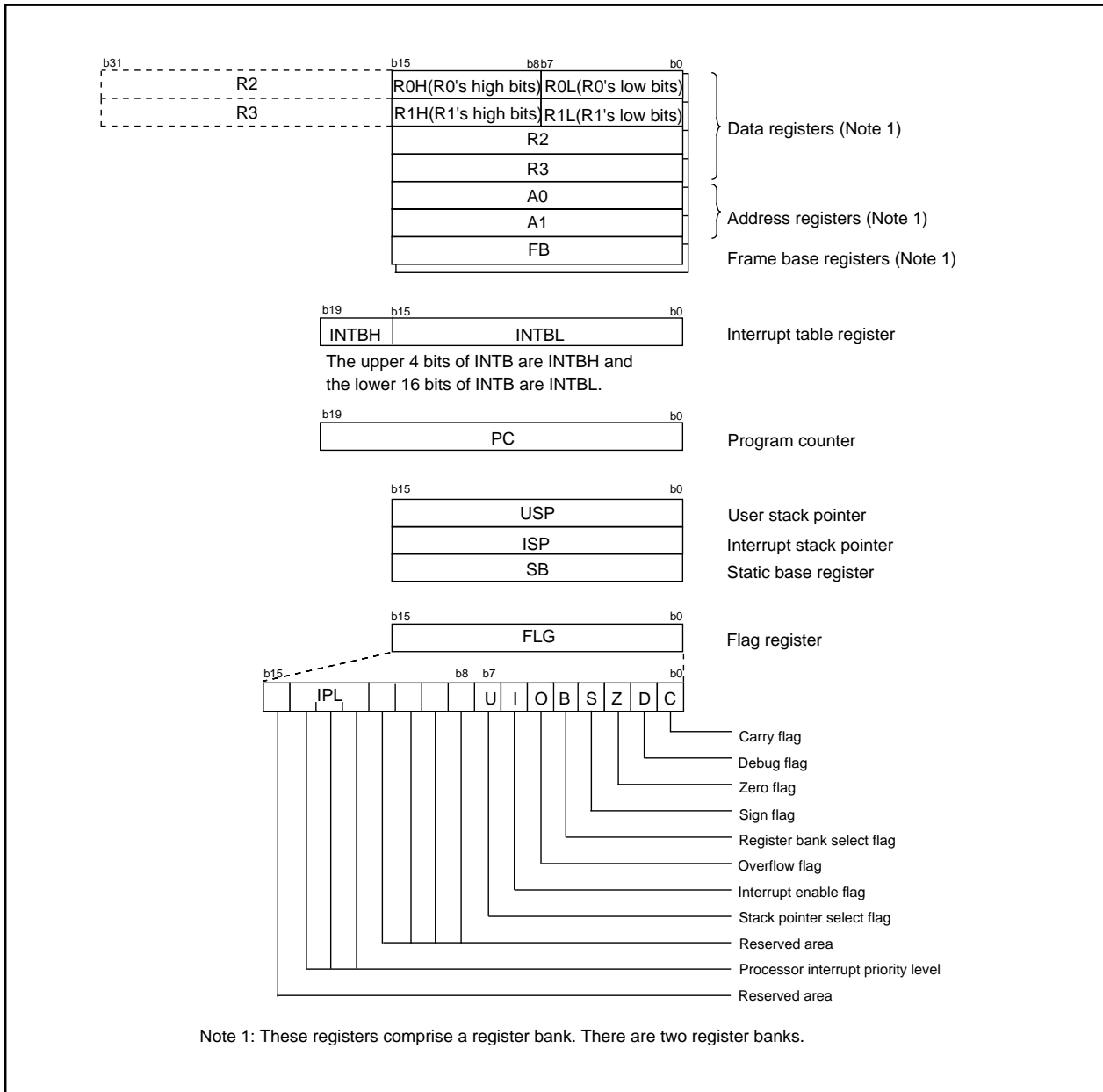


Figure 2.1. Central Processing Unit Register

### 2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

## 2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

## 2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

### 2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

### 2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

### 2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

### 2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

### 2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

### 2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

### 2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

### 2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

### 2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.



### 3. Memory

Figure 3.1 is a memory map of this MCU. The address space extends the 1M bytes from address 00000<sub>16</sub> to FFFFF<sub>16</sub>.

The internal ROM is allocated in a lower address direction beginning with address 0FFFF<sub>16</sub>. For example, a 16-Kbyte internal ROM is allocated to the addresses from 0C000<sub>16</sub> to 0FFFF<sub>16</sub>.

The fixed interrupt vector table is allocated to the addresses from 0FFDC<sub>16</sub> to 0FFFF<sub>16</sub>. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400<sub>16</sub>. For example, a 1-Kbyte internal RAM is allocated to the addresses from 00400<sub>16</sub> to 007FF<sub>16</sub>. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated. Special function registers (SFR) are allocated to the addresses from 00000<sub>16</sub> to 002FF<sub>16</sub>. Peripheral function control registers are located here. Of the SFR, any space which has no functions allocated is reserved for future use and cannot be used by users.

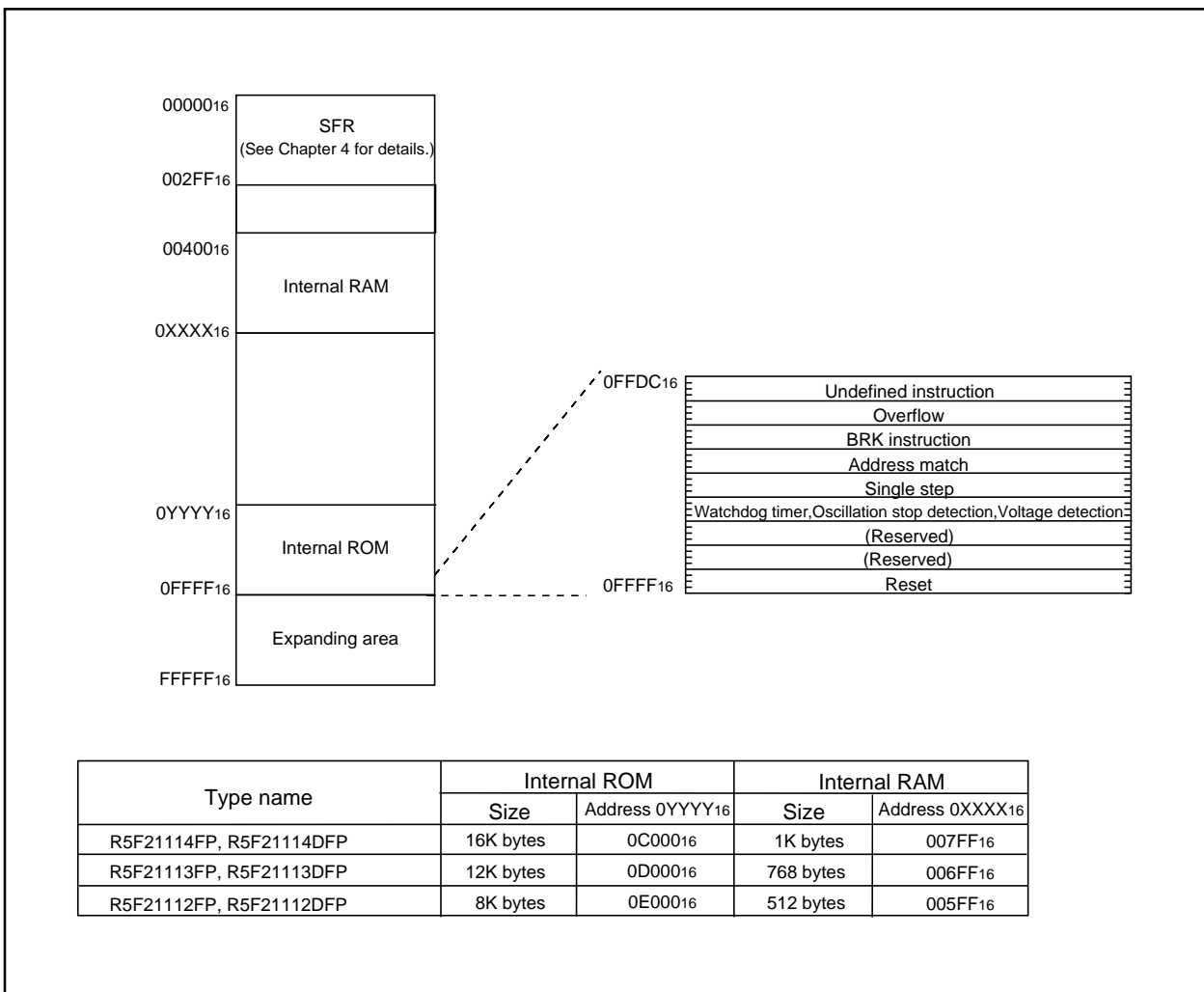


Figure 3.1 Memory Map

## 4. Special Function Register (SFR)

Address	Register	Symbol	After reset
0000 <sub>16</sub>			
0001 <sub>16</sub>			
0002 <sub>16</sub>			
0003 <sub>16</sub>			
0004 <sub>16</sub>	Processor mode register 0 <sup>1</sup>	PM0	00 <sub>16</sub>
0005 <sub>16</sub>	Processor mode register 1	PM1	00 <sub>16</sub>
0006 <sub>16</sub>	System clock control register 0	CM0	01101000 <sub>2</sub>
0007 <sub>16</sub>	System clock control register 1	CM1	00100000 <sub>2</sub>
0008 <sub>16</sub>	High-speed ring control register 0	HR0	00 <sub>16</sub>
0009 <sub>16</sub>	Address match interrupt enable register	AIER	XXXXXX00 <sub>2</sub>
000A <sub>16</sub>	Protect register	PRCR	00XXXX00 <sub>2</sub>
000B <sub>16</sub>	High-speed ring control register 1	HR1	40 <sub>16</sub>
000C <sub>16</sub>	Oscillation stop detection register	OCD	00000100 <sub>2</sub>
000D <sub>16</sub>	Watchdog timer reset register	WDTR	XX <sub>16</sub>
000E <sub>16</sub>	Watchdog timer start register	WDTS	XX <sub>16</sub>
000F <sub>16</sub>	Watchdog timer control register	WDC	000XXXXX <sub>2</sub>
0010 <sub>16</sub>	Address match interrupt register 0	RMAD0	00 <sub>16</sub>
0011 <sub>16</sub>			00 <sub>16</sub>
0012 <sub>16</sub>			X0 <sub>16</sub>
0013 <sub>16</sub>			
0014 <sub>16</sub>	Address match interrupt register 1	RMAD1	00 <sub>16</sub>
0015 <sub>16</sub>			00 <sub>16</sub>
0016 <sub>16</sub>			X0 <sub>16</sub>
0017 <sub>16</sub>			
0018 <sub>16</sub>			
0019 <sub>16</sub>	Voltage detection register 1 <sup>2</sup>	VCR1	00 <sub>16</sub>
001A <sub>16</sub>	Voltage detection register 2 <sup>2</sup>	VCR2	XXX00000 <sub>16</sub>
001B <sub>16</sub>			
001C <sub>16</sub>			
001D <sub>16</sub>			
001E <sub>16</sub>	INT0 input filter select register	INT0F	XXXXX000 <sub>2</sub>
001F <sub>16</sub>	Voltage detection interrupt register 2	D4INT	00 <sub>16</sub> <sup>3</sup>
0020 <sub>16</sub>			
0021 <sub>16</sub>			
0022 <sub>16</sub>			
0023 <sub>16</sub>			
0024 <sub>16</sub>			
0025 <sub>16</sub>			
0026 <sub>16</sub>			
0027 <sub>16</sub>			
0028 <sub>16</sub>			
0029 <sub>16</sub>			
002A <sub>16</sub>			
002B <sub>16</sub>			
002C <sub>16</sub>			
002D <sub>16</sub>			
002E <sub>16</sub>			
002F <sub>16</sub>			
0030 <sub>16</sub>			
0031 <sub>16</sub>			
0032 <sub>16</sub>			
0033 <sub>16</sub>			
0034 <sub>16</sub>			
0035 <sub>16</sub>			
0036 <sub>16</sub>			
0037 <sub>16</sub>			
0038 <sub>16</sub>			
0039 <sub>16</sub>			
003A <sub>16</sub>			
003B <sub>16</sub>			
003C <sub>16</sub>			
003D <sub>16</sub>			
003E <sub>16</sub>			
003F <sub>16</sub>			

010000012 <sup>4</sup>

X : Undefined  
 Blank columns are all reserved space. No access is allowed.  
 Notes:

1. Software reset or the watchdog timer reset does not affect bits 0 to 1 of PM0 register.
2. Software reset or the watchdog timer reset does not affect this register.
3. Owing to Reset input.
4. In the case of RESET pin = "H" retaining.

Address	Register	Symbol	After reset
0040 <sub>16</sub>			
0041 <sub>16</sub>			
0042 <sub>16</sub>			
0043 <sub>16</sub>			
0044 <sub>16</sub>			
0045 <sub>16</sub>			
0046 <sub>16</sub>			
0047 <sub>16</sub>			
0048 <sub>16</sub>			
0049 <sub>16</sub>			
004A <sub>16</sub>			
004B <sub>16</sub>			
004C <sub>16</sub>			
004D <sub>16</sub>	Key input interrupt control register	KUPIC	XXXXX0002
004E <sub>16</sub>	A-D conversion interrupt control register	ADIC	XXXXX0002
004F <sub>16</sub>			
0050 <sub>16</sub>	Compare 1 interrupt control register	CMP1IC	XXXXX0002
0051 <sub>16</sub>	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052 <sub>16</sub>	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053 <sub>16</sub>	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054 <sub>16</sub>	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055 <sub>16</sub>	INT2 interrupt control register	INT2IC	XXXXX0002
0056 <sub>16</sub>	Timer X interrupt control register	TXIC	XXXXX0002
0057 <sub>16</sub>	Timer Y interrupt control register	TYIC	XXXXX0002
0058 <sub>16</sub>	Timer Z interrupt control register	TZIC	XXXXX0002
0059 <sub>16</sub>	INT1 interrupt control register	INT1IC	XXXXX0002
005A <sub>16</sub>	INT3 interrupt control register	INT3IC	XXXXX0002
005B <sub>16</sub>	Timer C interrupt control register	TCIC	XXXXX0002
005C <sub>16</sub>	Compare 0 interrupt control register	CMPOIC	XXXXX0002
005D <sub>16</sub>	INT0 interrupt control register	INT0IC	XX00X0002
005E <sub>16</sub>			
005F <sub>16</sub>			
0060 <sub>16</sub>			
0061 <sub>16</sub>			
0062 <sub>16</sub>			
0063 <sub>16</sub>			
0064 <sub>16</sub>			
0065 <sub>16</sub>			
0066 <sub>16</sub>			
0067 <sub>16</sub>			
0068 <sub>16</sub>			
0069 <sub>16</sub>			
006A <sub>16</sub>			
006B <sub>16</sub>			
006C <sub>16</sub>			
006D <sub>16</sub>			
006E <sub>16</sub>			
006F <sub>16</sub>			
0070 <sub>16</sub>			
0071 <sub>16</sub>			
0072 <sub>16</sub>			
0073 <sub>16</sub>			
0074 <sub>16</sub>			
0075 <sub>16</sub>			
0076 <sub>16</sub>			
0077 <sub>16</sub>			
0078 <sub>16</sub>			
0079 <sub>16</sub>			
007A <sub>16</sub>			
007B <sub>16</sub>			
007C <sub>16</sub>			
007D <sub>16</sub>			
007E <sub>16</sub>			
007F <sub>16</sub>			

X : Undefined  
 Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	After reset
0080 <sub>16</sub>	Timer Y, Z mode register	TYZMR	0016
0081 <sub>16</sub>	Prescaler Y	PREY	FF16
0082 <sub>16</sub>	Timer Y secondary	TYSC	FF16
0083 <sub>16</sub>	Timer Y primary	TYPR	FF16
0084 <sub>16</sub>	Timer Y, Z waveform output control register	PUM	0016
0085 <sub>16</sub>	Prescaler Z	PREZ	FF16
0086 <sub>16</sub>	Timer Z secondary	TZSC	FF16
0087 <sub>16</sub>	Timer Z primary	TZPR	FF16
0088 <sub>16</sub>			
0089 <sub>16</sub>			
008A <sub>16</sub>	Timer Y, Z output control register	TYZOC	0016
008B <sub>16</sub>	Timer X mode register	TXMR	0016
008C <sub>16</sub>	Prescaler X	PREX	FF16
008D <sub>16</sub>	Timer X register	TX	FF16
008E <sub>16</sub>	Count source set register	TCSS	0016
008F <sub>16</sub>			
0090 <sub>16</sub>	Timer C register	TC	0016
0091 <sub>16</sub>			0016
0092 <sub>16</sub>			
0093 <sub>16</sub>			
0094 <sub>16</sub>			
0095 <sub>16</sub>			
0096 <sub>16</sub>	External input enable register	INTEN	0016
0097 <sub>16</sub>			
0098 <sub>16</sub>	Key input enable register	KIEN	0016
0099 <sub>16</sub>			
009A <sub>16</sub>	Timer C control register 0	TCC0	0016
009B <sub>16</sub>	Timer C control register 1	TCC1	0016
009C <sub>16</sub>	Capture, compare 0 register	TM0	XX16
009D <sub>16</sub>			XX16
009E <sub>16</sub>	Compare 1 register	TM1	XX16
009F <sub>16</sub>			XX16
00A0 <sub>16</sub>	UART0 transmit/receive mode register	U0MR	0016
00A1 <sub>16</sub>	UART0 bit rate generator	U0BRG	XX16
00A2 <sub>16</sub>	UART0 transmit buffer register	U0TB	XX16
00A3 <sub>16</sub>			XX16
00A4 <sub>16</sub>	UART0 transmit/receive control register 0	U0C0	000010002
00A5 <sub>16</sub>	UART0 transmit/receive control register 1	U0C1	000000102
00A6 <sub>16</sub>	UART0 receive buffer register	U0RB	XX16
00A7 <sub>16</sub>			XX16
00A8 <sub>16</sub>	UART1 transmit/receive mode register	U1MR	0016
00A9 <sub>16</sub>	UART1 bit rate generator	U1BRG	XX16
00AA <sub>16</sub>	UART1 transmit buffer register	U1TB	XX16
00AB <sub>16</sub>			XX16
00AC <sub>16</sub>	UART1 transmit/receive control register 0	U1C0	000010002
00AD <sub>16</sub>	UART1 transmit/receive control register 1	U1C1	000000102
00AE <sub>16</sub>	UART1 receive buffer register	U1RB	XX16
00AF <sub>16</sub>			XX16
00B0 <sub>16</sub>	UART transmit/receive control register 2	UCON	0016
00B1 <sub>16</sub>			
00B2 <sub>16</sub>			
00B3 <sub>16</sub>			
00B4 <sub>16</sub>			
00B5 <sub>16</sub>			
00B6 <sub>16</sub>			
00B7 <sub>16</sub>			
00B8 <sub>16</sub>			
00B9 <sub>16</sub>			
00BA <sub>16</sub>			
00BB <sub>16</sub>			
00BC <sub>16</sub>			
00BD <sub>16</sub>			
00BE <sub>16</sub>			
00BF <sub>16</sub>			

X : Undefined  
 Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	After reset
00C0 <sub>16</sub>	A-D register	AD	XX16
00C1 <sub>16</sub>			XX16
00C2 <sub>16</sub>			
00C3 <sub>16</sub>			
00C4 <sub>16</sub>			
00C5 <sub>16</sub>			
00C6 <sub>16</sub>			
00C7 <sub>16</sub>			
00C8 <sub>16</sub>			
00C9 <sub>16</sub>			
00CA <sub>16</sub>			
00CB <sub>16</sub>			
00CC <sub>16</sub>			
00CD <sub>16</sub>			
00CE <sub>16</sub>			
00CF <sub>16</sub>			
00D0 <sub>16</sub>			
00D1 <sub>16</sub>			
00D2 <sub>16</sub>			
00D3 <sub>16</sub>			
00D4 <sub>16</sub>	A-D control register 2	ADCON2	0016
00D5 <sub>16</sub>			
00D6 <sub>16</sub>	A-D control register 0	ADCON0	00000XX2
00D7 <sub>16</sub>	A-D control register 1	ADCON1	0016
00D8 <sub>16</sub>			
00D9 <sub>16</sub>			
00DA <sub>16</sub>			
00DB <sub>16</sub>			
00DC <sub>16</sub>			
00DD <sub>16</sub>			
00DE <sub>16</sub>			
00DF <sub>16</sub>			
00E0 <sub>16</sub>	Port P0 register	P0	XX16
00E1 <sub>16</sub>	Port P1 register	P1	XX16
00E2 <sub>16</sub>	Port P0 direction register	PD0	0016
00E3 <sub>16</sub>	Port P1 direction register	PD1	0016
00E4 <sub>16</sub>			
00E5 <sub>16</sub>	Port P3 register	P3	XX16
00E6 <sub>16</sub>			
00E7 <sub>16</sub>	Port P3 direction register	PD3	0016
00E8 <sub>16</sub>	Port P4 register	P4	XX16
00E9 <sub>16</sub>			
00EA <sub>16</sub>	Port P4 direction register	PD4	0016
00EB <sub>16</sub>			
00EC <sub>16</sub>			
00ED <sub>16</sub>			
00EE <sub>16</sub>			
00EF <sub>16</sub>			
00F0 <sub>16</sub>			
00F1 <sub>16</sub>			
00F2 <sub>16</sub>			
00F3 <sub>16</sub>			
00F4 <sub>16</sub>			
00F5 <sub>16</sub>			
00F6 <sub>16</sub>			
00F7 <sub>16</sub>			
00F8 <sub>16</sub>			
00F9 <sub>16</sub>			
03FA <sub>16</sub>			
00FB <sub>16</sub>			
00FC <sub>16</sub>	Pull-up control register 0	PUR0	00XX0002
00FD <sub>16</sub>	Pull-up control register 1	PUR1	XXXXXX0X2
00FE <sub>16</sub>	Port P1 drivability control register	DRR	0016
00FF <sub>16</sub>	Timer C output control register	TCOUT	0016
≈ ≈			
01B3 <sub>16</sub>	Flash memory control register 4	FMR4	0100000X2
01B4 <sub>16</sub>			
01B5 <sub>16</sub>	Flash memory control register 1	FMR1	0100XX0X2
01B6 <sub>16</sub>			
01B7 <sub>16</sub>	Flash memory control register 0	FMR0	XX0000012

X : Undefined  
 Blank columns are all reserved space. No access is allowed.

## 5. Electrical Characteristics

**Table 5.1 Absolute Maximum Ratings**

Symbol	Parameter	Condition	Rated value	Unit
V <sub>CC</sub>	Supply voltage	V <sub>CC</sub> =AV <sub>CC</sub>	-0.3 to 6.5	V
AV <sub>CC</sub>	Analog supply voltage	V <sub>CC</sub> =AV <sub>CC</sub>	-0.3 to 6.5	V
V <sub>I</sub>	Input voltage		-0.3 to V <sub>CC</sub> +0.3	V
V <sub>O</sub>	Output voltage		-0.3 to V <sub>CC</sub> +0.3	V
P <sub>d</sub>	Power dissipation	T <sub>opr</sub> =25 °C	300	mW
T <sub>opr</sub>	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T <sub>stg</sub>	Storage temperature		-65 to 150	°C

**Table 5.2 Recommended Operating Conditions**

Symbol	Parameter	Conditions	Standard			Unit	
			Min.	Typ.	Max.		
V <sub>CC</sub>	Supply voltage		2.7	5.0	5.5	V	
AV <sub>CC</sub>	Analog supply voltage		—	V <sub>CC</sub>	—	V	
V <sub>SS</sub>	Supply voltage		—	0	—	V	
AV <sub>SS</sub>	Analog supply voltage		—	0	—	V	
V <sub>IH</sub>	"H" input voltage		0.8V <sub>CC</sub>	—	V <sub>CC</sub>	V	
V <sub>IL</sub>	"L" input voltage		0	—	0.2V <sub>CC</sub>	V	
I <sub>OH (sum)</sub>	"H" peak all output currents	Sum of all pins' IOH (peak)	—	—	-60.0	mA	
I <sub>OH (peak)</sub>	"H" peak output current		—	—	-10.0	mA	
I <sub>OH (avg)</sub>	"H" average output current		—	—	-5.0	mA	
I <sub>OL (sum)</sub>	"L" peak all output currents	Sum of all pins' IOL (peak)	—	—	60	mA	
I <sub>OL (peak)</sub>	"L" peak output current	Except P10 to P17	—	—	10	mA	
		P10 to P17	Drive ability HIGH	—	—	30	mA
			Drive ability LOW	—	—	10	mA
I <sub>OL (avg)</sub>	"L" average output current	Except P10 to P17	—	—	5	mA	
		P10 to P17	Drive ability HIGH	—	—	15	mA
			Drive ability LOW	—	—	5	mA
f (XIN)	Main clock input oscillation frequency	3.0V ≤ V <sub>CC</sub> ≤ 5.5V	0	—	20	MHz	
		2.7V ≤ V <sub>CC</sub> < 3.0V	0	—	10	MHz	

**Note**

- 1: Referenced to V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 to 5.5V at T<sub>opr</sub> = -20 to 85 °C / -40 to 85 °C unless otherwise specified.  
 2: The mean output current is the mean value within 100ms.

**Table 5.3 A-D Conversion Characteristics**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
—	Resolution		Vref =VCC			10	Bit
—	Absolute accuracy	10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V			±3	LSB
		8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V			±2	LSB
		10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=3.3V			±5	LSB
		8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=3.3V			±2	LSB
RLADDER	Ladder resistance		VREF=VCC	10		40	kΩ
tCONV	Conversion time		10 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V	3.3		μs
			8 bit mode	f(XIN)=øAD=10 MHz, Vref=Vcc=5.0V	2.8		μs
VREF	Reference voltage			2.0		Vcc	V
VIA	Analog input voltage			0		Vref	V
—	A-D operation clock frequency <sup>2</sup>	Without sample & hold		0.25		10	MHz
		With sample & hold		1.0		10	MHz

Note

- 1: Referenced to Vcc=AVcc=2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
- 2: When fAD is 10 MHz more, divide the fAD and make A-D operation clock frequency (øAD) lower than 10 MHz.
- 3: When the Vcc is less than 4.2V, divide the fAD and make A-D operation clock frequency (øAD) lower than fAD/2.

**Table 5.4 Flash Memory Version Electrical Characteristics**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
—	Byte program time		—	75	TBD	μs
—	Block erase time		—	400	TBD	ms
—	Program, Erase Voltage		2.7	—	5.5	V
—	Read Voltage		2.7	—	5.5	V
—	Program, Erase Temperature		0	—	60	°C

Note

- 1: Referenced to Vcc1=AVcc=2.7 to 5.5V at Topr = 0 to 60 °C unless otherwise specified.

**Table 5.5 Voltage Detection Circuit Electrical Characteristics**

Symbol	Parameter	Measuring condition	Min.	Standard		Unit
				Typ.	Max.	
Vdet4	Voltage detection level		3.3	3.8	4.3	V
	Voltage detection interrupt request generating time <sup>2</sup>			40		V
	Voltage detection circuit self consumption current	VC27="1"			TBD	V
td(E-A)	Waiting time till voltage detection circuit operation starts <sup>3</sup>				20	V

Note

- 1: The measuring condition is Vcc=AVcc=5.0 V and Topr=25 °C.
- 2: This shows the time till the voltage detection interrupt request is generated since the voltage passes Vdet.
- 3: This shows the required time till the voltage detection circuit operates when setting to "1" again.

**Table 5.6 Power-on Reset Circuit Electrical Characteristics**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
	Power-on reset start time <sup>2</sup>	V <sub>cc</sub> <0.5V	TBD			ms
	Power-on reset cancel operation start voltage		3.3	3.8	4.3	V
	Hardware reset 2 cancel operation start voltage		3.3	3.8	4.3	V
	Supply start up condition when using power-on reset circuit	Intergradation time to 0V<2.7V			TBD	ms

Note

- 1: The measuring condition is V<sub>cc</sub>=AV<sub>cc</sub>=5.0 V and Topr=25 °C.
- 2: Keep V<sub>cc</sub><0.5V for over regulated time to execute the reset operation.

**Table 5.7 High-speed Ring Oscillator Circuit Electrical Characteristics**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
	Settable high-speed ring oscillator minimum period	Set "0016" in the HR1 register		TBD		ns
	High-speed ring oscillator adjusted unit	Differences when setting "0116" and "0016" in the HR register		1		ns

Note

- 1: The measuring condition is V<sub>cc</sub>=AV<sub>cc</sub>=5.0 V and Topr=25 °C.

**Table 5.8 Power Circuit Timing Characteristics**

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on <sup>2</sup>				2	ms
td(R-S)	STOP release time <sup>3</sup>				150	μs

Note

- 1: The measuring condition is V<sub>cc</sub>=AV<sub>cc</sub>=2.7 to 5.0 V and Topr=25 °C.
- 2: This shows the wait time until the internal power supply generating circuit is stabilized during power-on.
- 3: This shows the time till BCLK starts from the interrupt acknowledgement to cancel stop mode.



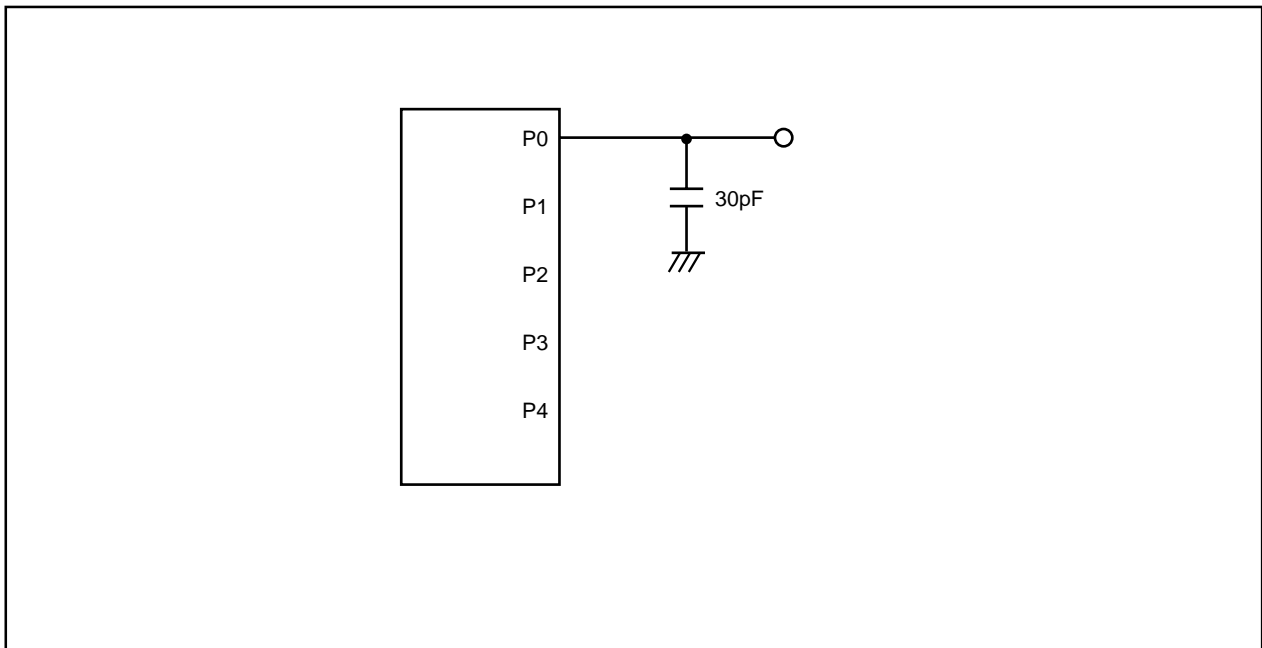


Figure 5.1 Port P0 to P4 measurement circuit

**Table 5.9 Electrical Characteristics (1) [Vcc=5V]**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V <sub>OH</sub>	"H" output voltage	Except X <sub>OUT</sub>	I <sub>OH</sub> =-5mA	V <sub>CC</sub> -2.0		V <sub>CC</sub>	V
			I <sub>OH</sub> =-200μA	V <sub>CC</sub> -0.3		V <sub>CC</sub>	V
		X <sub>OUT</sub>	Drive ability HIGH I <sub>OH</sub> =-1 mA	V <sub>CC</sub> -2.0		V <sub>CC</sub>	V
			Drive ability LOW I <sub>OH</sub> =-500μA	V <sub>CC</sub> -2.0		V <sub>CC</sub>	V
V <sub>OL</sub>	"L" output voltage	P10 to P17 Except X <sub>OUT</sub>	I <sub>OH</sub> = 5 mA			2.0	V
			I <sub>OH</sub> = 200 μA			0.45	V
		P10 to P17	Drive ability HIGH I <sub>OH</sub> = 10 mA			2.0	V
			Drive ability LOW I <sub>OH</sub> = 5 mA			2.0	V
		X <sub>OUT</sub>	Drive ability HIGH I <sub>OH</sub> = 1 mA			2.0	V
			Drive ability LOW I <sub>OH</sub> =500μA			2.0	V
V <sub>T+</sub> -V <sub>T-</sub>	Hysteresis	INT0, INT1, INT2, INT3, K10, K11, K12, K13, CNTR0, CNTR1, TCIN, RxD0, RxD1		0.2		1.0	V
		RESET		0.2		2.2	V
I <sub>IH</sub>	"H" input current		V <sub>I</sub> =5V			5.0	μA
I <sub>IL</sub>	"L" input current		V <sub>I</sub> =0V			-5.0	μA
R <sub>PULLUP</sub>	Pull-up resistance		V <sub>I</sub> =0V	30	50	167	kΩ
R <sub>FXIN</sub>	Feedback resistance	X <sub>IN</sub>				1.0	MΩ
f <sub>RING-S</sub>	Low-speed ring oscillator frequency			40	125	250	kHz
V <sub>RAM</sub>	RAM retention voltage		At stop mode	2.0			V

Note

1 : Referenced to V<sub>CC</sub>=AV<sub>CC</sub>=4.2 to 5.5V at T<sub>opr</sub> = -20 to 85 °C / -40 to 85 °C, f(BCLK)=20MHz unless otherwise specified.

**Table 5.10 Electrical Characteristics (2) [Vcc=5V]**

Symbol	Parameter	Measuring condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are Vss	High-speed mode	XIN=20 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		9	15	mA
			XIN=16 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		8	14	mA
			XIN=10 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		5		mA
		Medium-speed mode	XIN=20 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		4		mA
			XIN=16 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		3		mA
			XIN=10 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		2		mA
		High-speed ring oscillator mode	Main clock off High-speed ring oscillator on=8 MHz Low-speed ring oscillator on=125 kHz No division		4	8	mA
			Main clock off High-speed ring oscillator on=8 MHz Low-speed ring oscillator on=125 kHz Division by 8		1.5		mA
		Low-speed ring oscillator mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		0.4	2.0	mA
		Wait mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz When a WAIT instruction is executed <sup>2</sup> Peripheral clock operation		40	80	μA
		Wait mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz When a WAIT instruction is executed <sup>2</sup> Peripheral clock off		38	76	μA
		Stop mode	Main clock off High-speed ring oscillator off Low-speed ring oscillator off CM10="1" Peripheral clock off VC27="0"		0.8	3.0	μA

Note

- 1: The power supply current measuring is executed using the measuring program on frash memory.
- 2: Timer Y is operated with timer mode.

**Timing requirements (Unless otherwise noted: VCC = 5V, VSS = 0V at Ta = 25 °C) [VCC=5V]**

**Table 5.11 XIN input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	62.5		ns
tWH(XIN)	XIN input HIGH pulse width	30		ns
tWL(XIN)	XIN input LOW pulse width	30		ns

**Table 5.12 CNTR0 input, CNTR1 input, INT2 input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	100		ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	40		ns
tWL(CNTR0)	CNTR0 input LOW pulse width	40		ns

**Table 5.13 TCIN input, INT3 input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	400 <sup>1</sup>		ns
tWH(TCIN)	TCIN input HIGH pulse width	200 <sup>2</sup>		ns
tWL(TCIN)	TCIN input LOW pulse width	200 <sup>2</sup>		ns

Note

- 1 : Use the greater value, either ( 1 / digital filter clock frequency x 6 ) or min. value.  
 2 : Use the greater value, either ( 1 / digital filter clock frequency x 3 ) or min. value.

**Table 5.14 Serial I/O**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CLK)	CLKi input cycle time	200		ns
tW(CLKH)	CLKi input HIGH pulse width	100		ns
tW(CLKL)	CLKi input LOW pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	35		ns
th(C-D)	RxDi input hold time	90		ns

**Table 5.15 External interrupt INT0 input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	INT0 input HIGH pulse width	250 <sup>1</sup>		ns
tW(INL)	INT0 input LOW pulse width	250 <sup>2</sup>		ns

Note

- 1 : When the INT0 input filter select bit selects the digital filter, use the INT0 input HIGH pulse width to the greater value, either ( 1 / digital filter clock frequency x 3 ) or min. value.  
 2 : When the INT0 input filter select bit selects the digital filter, use the INT0 input LOW pulse width to the greater value, either ( 1 / digital filter clock frequency x 3 ) or min. value.

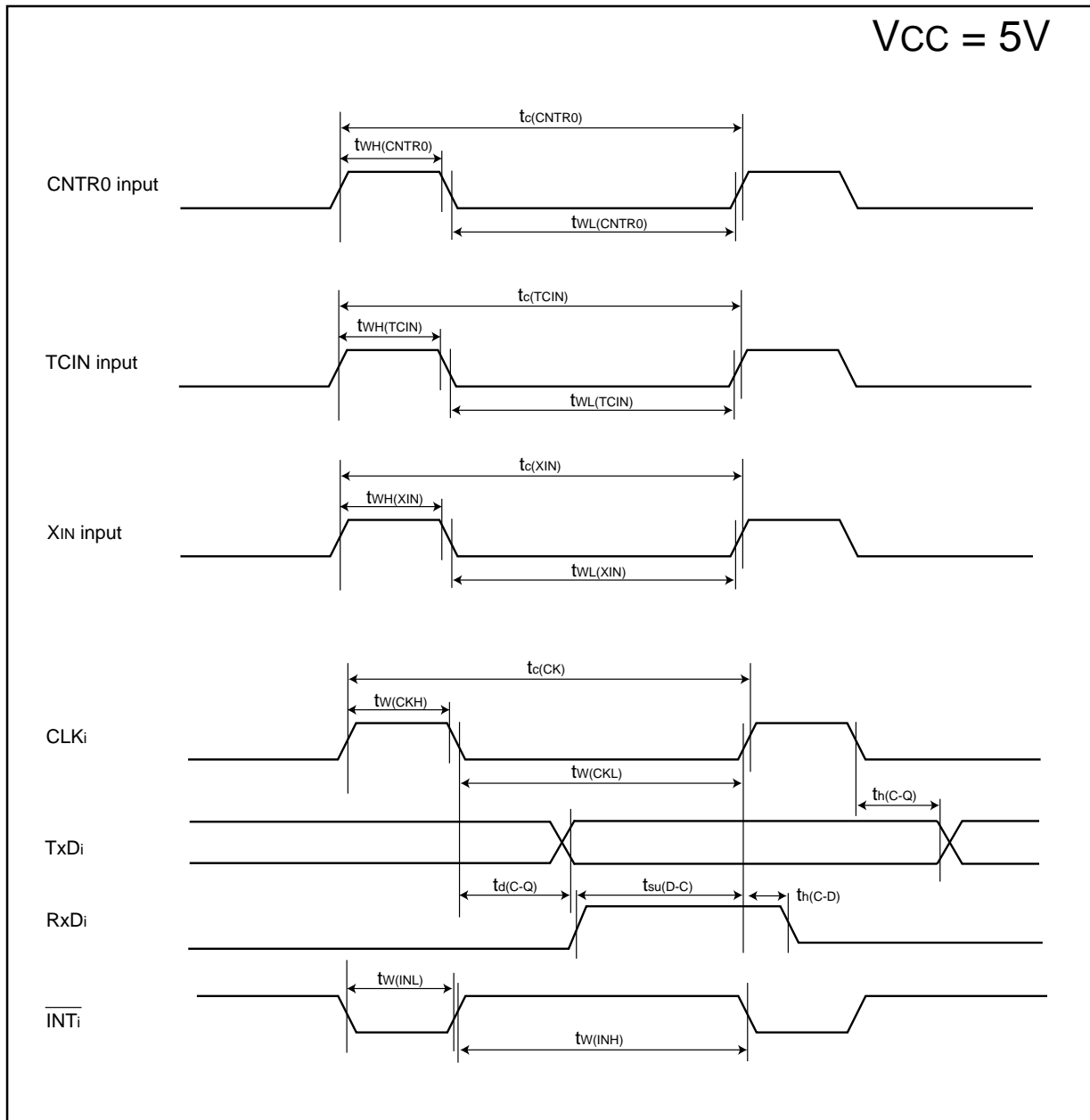


Figure 5.2  $V_{CC}=5V$  timing diagram

**Table 5.16 Electrical Characteristics (3) [Vcc=3V]**

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	"H" output voltage	Except XOUT	IOH=-1mA	Vcc-0.5		Vcc	V
		XOUT	Drive ability HIGH IOH=-0.1 mA	Vcc-0.5		Vcc	V
			Drive ability LOW IOH=-50 μA	Vcc-0.5		Vcc	V
VOL	"L" output voltage	P10 to P17 Except XOUT	IOH= 1 mA			0.5	V
		P10 to P17	Drive ability HIGH IOH= 2 mA			0.5	V
			Drive ability LOW IOH= 1 mA			0.5	V
			XOUT	Drive ability HIGH IOH= 0.1 mA			0.5
			Drive ability LOW IOH=50 μA			0.5	V
VT+·VT-	Hysteresis	INT0, INT1, INT2, INT3, K10, K11, K12, K13, CNTR0, CNTR1, TCIN, RxD0, RxD1		0.2		0.8	V
		RESET		0.2		1.8	V
IiH	"H" input current		Vi=3V			4.0	μA
IiL	"L" input current		Vi=0V			-4.0	μA
RPULLUP	Pull-up resistance		Vi=0V	66	160	500	kΩ
R <sub>MIN</sub>	Feedback resistance	XIN			3.0		MΩ
fRING-S	Low-speed ring oscillator frequency			40	125	250	kHz
V <sub>RAM</sub>	RAM retention voltage		At stop mode	2.0			V

Note

1 : Referenced to Vcc=AVcc=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.

**Table 5.17 Electrical Characteristics (4) [Vcc=3V]**

Symbol	Parameter	Measuring condition	Standard			Unit	
			Min.	Typ.	Max.		
I <sub>CC</sub>	Power supply current (V <sub>CC</sub> =2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V <sub>SS</sub>	High-speed mode X <sub>IN</sub> =20 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz No division		8	13	mA	
				7	12	mA	
				5		mA	
		Medium-speed mode X <sub>IN</sub> =16 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		3		mA	
			X <sub>IN</sub> =16 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		2.5		mA
			X <sub>IN</sub> =10 MHz (square wave) High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8		1.6		mA
		High-speed ring oscillator mode Main clock off High-speed ring oscillator on=8 MHz Low-speed ring oscillator on=125 kHz No division			3.5	7.5	mA
			Main clock off High-speed ring oscillator on=8 MHz Low-speed ring oscillator on=125 kHz Division by 8		1.5		mA
		Low-speed ring oscillator mode Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz Division by 8			0.4	2.0	mA
		Wait mode Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz When a WAIT instruction is executed <sup>2</sup> Peripheral clock operation			37	74	μA
		Wait mode Main clock off High-speed ring oscillator off Low-speed ring oscillator on=125 kHz When a WAIT instruction is executed <sup>2</sup> Peripheral clock off			35	70	μA
Stop mode Main clock off High-speed ring oscillator off Low-speed ring oscillator off CM10="1" Peripheral clock off VC27="0"			0.7	3.0	μA		

Note

- 1: The power supply current measuring is executed using the measuring program on flash memory.
- 2: Timer Y is operated with timer mode.

**Timing requirements (Unless otherwise noted: Vcc = 3V, Vss = 0V at Ta = 25 °C) [Vcc=3V]**

**Table 5.18 XIN input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	143		ns
tWH(XIN)	XIN input HIGH pulse width	70		ns
tWL(XIN)	XIN input LOW pulse width	70		ns

**Table 5.19 CNTR0 input, CNTR1 input, INT2 input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	300		ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	120		ns
tWL(CNTR0)	CNTR0 input LOW pulse width	120		ns

**Table 5.20 TCIN input, INT3 input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	1200 <sup>1</sup>		ns
tWH(TCIN)	TCIN input HIGH pulse width	600 <sup>2</sup>		ns
tWL(TCIN)	TCIN input LOW pulse width	600 <sup>2</sup>		ns

Note

- 1 : Use the greater value, either ( 1/ digital filter clock frequency x 6) or min. value.  
 2 : Use the greater value, either ( 1/ digital filter clock frequency x 3) or min. value.

**Table 5.21 Serial I/O**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	300		ns
tW(CKH)	CLKi input HIGH pulse width	150		ns
tW(CKL)	CLKi input LOW pulse width	150		ns
td(C-Q)	TxDi output delay time		160	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	55		ns
th(C-D)	RxDi input hold time	90		ns

**Table 5.22 External interrupt INT0 input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	INT0 input HIGH pulse width	380 <sup>1</sup>		ns
tW(INL)	INT0 input LOW pulse width	380 <sup>2</sup>		ns

Note

- 1 : When the INT0 input filter select bit selects the digital filter, use the INT0 input HIGH pulse width to the greater value, either ( 1/ digital filter clock frequency x 3) or min. value.  
 2 : When the INT0 input filter select bit selects the digital filter, use the INT0 input LOW pulse width to the greater value, either ( 1/ digital filter clock frequency x 3) or min. value.



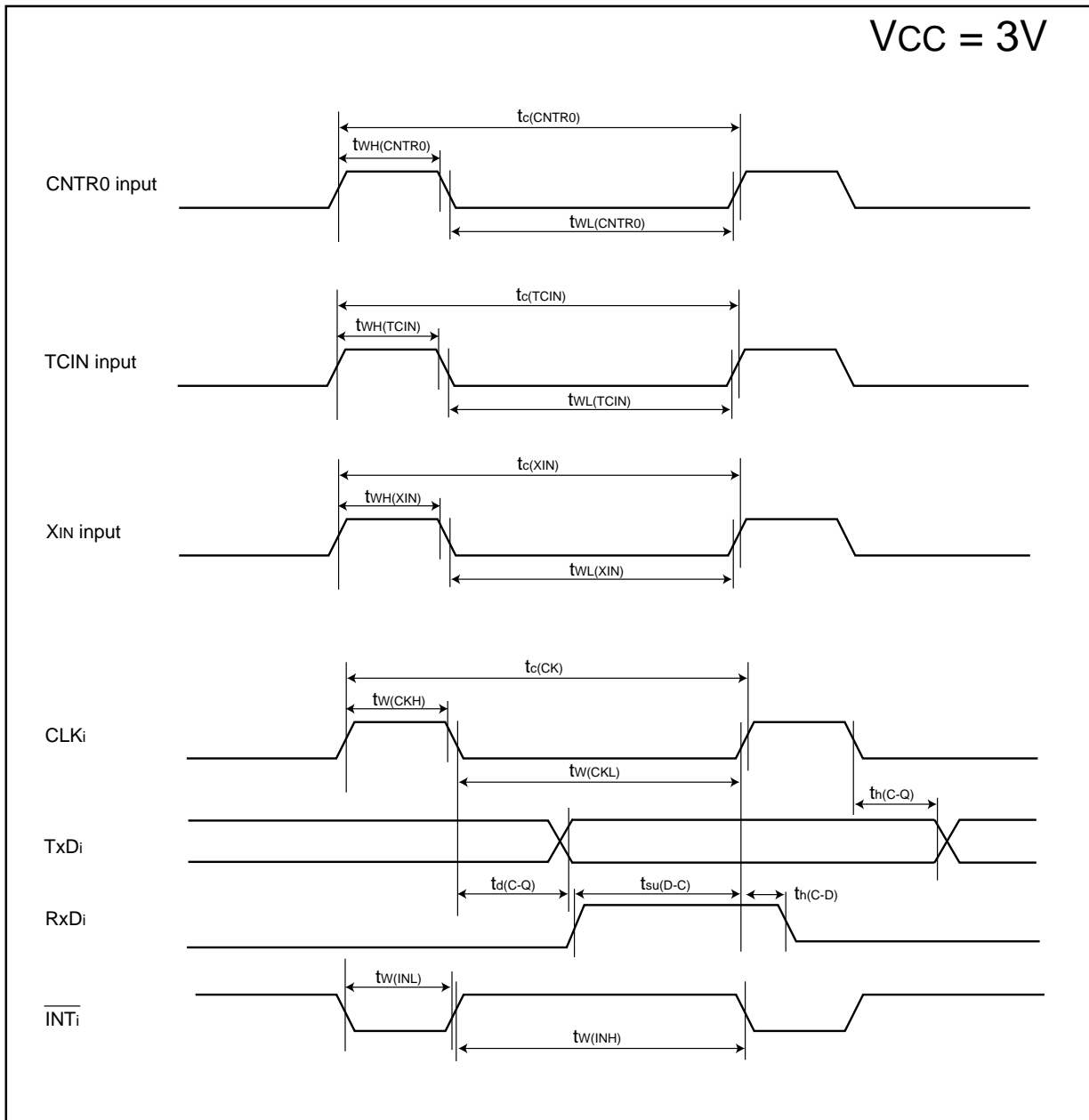


Figure 5.3  $V_{CC}=3V$  timing diagram

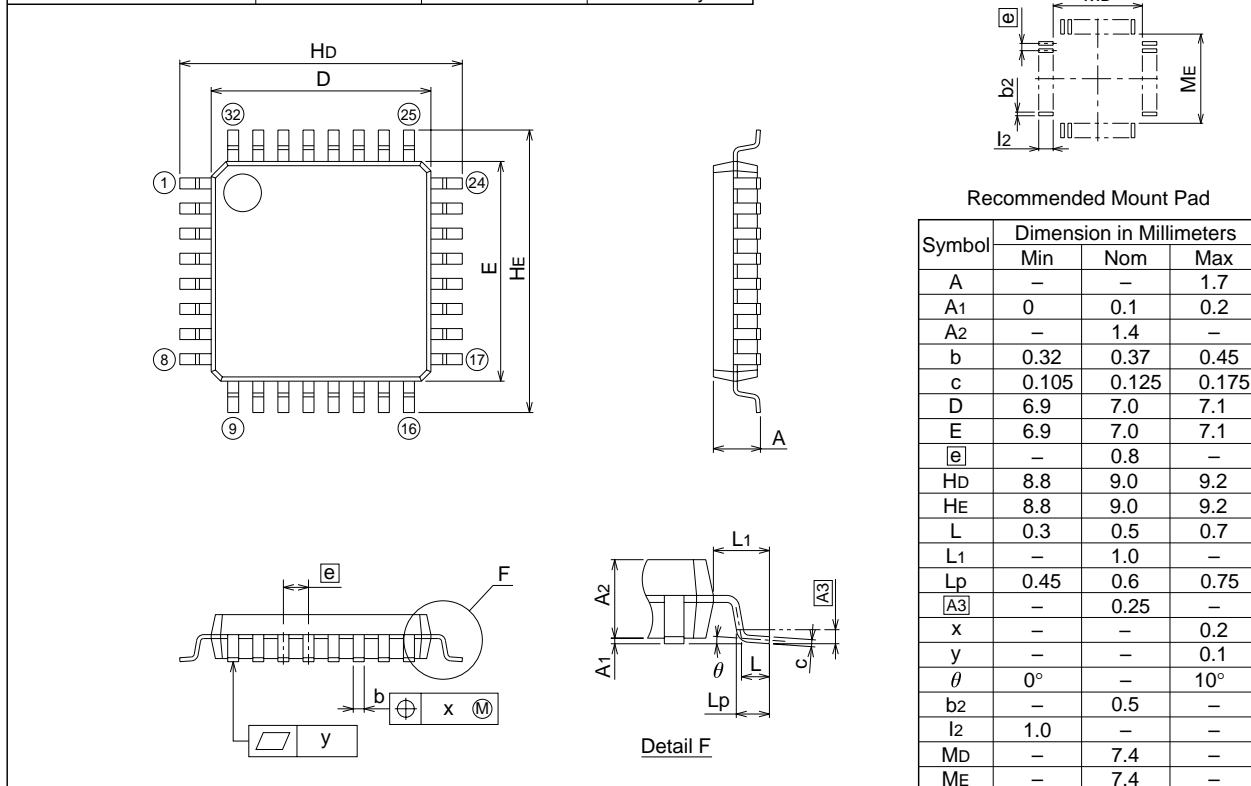
## Package Dimensions

### 32P6U-A

(MMP)

Plastic 32pin 7X7mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP32-P-0707-0.80	-		Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0	0.1	0.2
A2	-	1.4	-
b	0.32	0.37	0.45
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
[e]	-	0.8	-
$H_D$	8.8	9.0	9.2
$H_E$	8.8	9.0	9.2
L	0.3	0.5	0.7
$L_1$	-	1.0	-
$L_p$	0.45	0.6	0.75
[A3]	-	0.25	-
x	-	-	0.2
y	-	-	0.1
$\theta$	0°	-	10°
$b_2$	-	0.5	-
$l_2$	1.0	-	-
$M_d$	-	7.4	-
$M_e$	-	7.4	-

REVISION HISTORY

R8C/11 Group Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 19, 2003		First edition issued
1.10	Sep. 08, 2003	2 5 6 10 12 14	Table 1.1: Shortest instruction execution time and $f(X_{IN})$ changed Figure 1.3: Pin name changed from TXOUT to $\overline{CNTR0}$ Table 1.3: Pin name changed from TXOUT to $\overline{CNTR0}$ The value of HR1 register after reset changed The value of TC register after reset changed Chapter "5. Electrical Characteristics" added
1.20	Oct. 31, 2003	2 6 11 14 15 17 19  20 21 22 23  24 25	Table 1.1: Power consumption values added Table 1.3: Resistor value for CNVss and MODE deleted Register name of address 0050 <sub>16</sub> modified from CMP2IC to CMP1IC, register name of address 005C <sub>16</sub> modified from CMP1IC to CMP0IC Table 5.2: Note 3 and Note 4 deleted tsamp in Table 5.3 deleted Figure 5.1 added Table 5.10: Vcc changed from "4.2 to 5.5V" to "3.3V to 5.5V", low-power ring oscillator changed from "on 100kHz" to "125kHz", X <sub>IN</sub> =5MHz deleted and X <sub>IN</sub> =10MHz added in high-speed mode and medium-speed mode, VC27="0" added in stop mode measuring condition, data added and modified Table 11 to Table 15 added Figure 5.2 added Table 5.16: Note 1, f(BCLK)=5 MHz changed to 10 MHz Table 5.17: low-power ring oscillator changed from "on 100kHz" to "125kHz", X <sub>IN</sub> =5MHz deleted and X <sub>IN</sub> =10MHz added in high-speed mode and medium-speed mode, VC27="0" added in stop mode measuring condition, data added and modified Table 5.18 to Table 5.22 added Figure 5.3 added

**Keep safety first in your circuit designs!**

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