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1. Overview

The M32C/80 group is microcomputer that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/80 group is available in the 100-pin plastic molded QFP/LQFP package. With 16-Mbyte of address space, it is capable of executing instructions at high speed.
With 16-Mbyte of address space, it is capable of executing instructions at high speed.
This ROM-efficient microcomputer achieves considerable decrease of approximate 50% external ROM capacity from existing products.

The M32C/80 group can be used in microprocessor mode for the external ROM version.

1.1 Applications

Audio, cameras, office equipment, communications equipment, portable equipment, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Outline

Tables 1.1 list performance outline of the M32C/80 group.

Table 1.1. Performance outline of M32C/80 group (100-pin version)

	Item	Performance
CPU	Number of basic instructions	108 instructions
	Shortest instruction execution time	31.3 ns (f(BCLK)=32MHz, V_{CC1}=4.2 to 5.0V) 41.7 ns (f(BCLK)=24MHz, V_{CC1}=3.0 to 5.0V)
	Operation mode	Microprocessor mode
	Memory space	16 M bytes
	Memory capacity	See **Table 1.2.**
Peripheral function	Port	Input/Output : 47pins, Input : 1pin
	Multifunction timer	Timer A : 16 bits x 5 channels, Timer B : 16 bits x 6 channels Three phase motor control circuit
	HDLC data process	2 channels
	Serial I/O	5 channels Clock synchronous, UART, IE Bus(option)(1), I^2C Bus(option) (2)
	A-D converter	10-bit A-D converter: 1 circuit, 10 channels
	D-A converter	8 bits x 2 channels
	DMAC	4 channels
	DMAC II	Start by all variable vector interrupt factors Immediate transfer, operation and chain transfer function
	CRC calculation circuit	CCITT-CRC
	X-Y converter	16 bits X 16 bits
	Watchdog timer	15 bits x 1 channel(with prescaler)
	Interrupt	Internal: 33 sources, External: 8 sources, Software: 4 sources, Priority level: 7 levels
	Clock generating circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), Ring oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.
	Oscillation stop detection function	Stop detection of main clock oscillation
	Voltage detection circuit	Present (option)
Electric characteris-tics	Supply voltage	V_{CC1}=4.2 to 5.5V, V_{CC2}=3.0 to V_{CC1} (f(BCLK)=32MHz) V_{CC1}=3.0 to 5.5V, V_{CC2}=3.0 to V_{CC1} (f(BCLK)=24MHz)
	Power consumption	38mA (V_{CC1}=V_{CC2}=5V, f(BCLK)=32MHz) 26mA (V_{CC1}=V_{CC2}=3.3V, f(BCLK)=24MHz) T.B.D (V_{CC1}=V_{CC2}=3.3V, f(Xcin)=32kHz, Wait-mode) T.B.D (V_{CC1}=V_{CC2}=3.3V, Stop mode)
Operating ambient temperature		–20 to 85°C –40 to 85°C(option)
Package		100-pin plastic mold QFP

NOTES:

1. IE Bus is a trademark of NEC corporation.
2. I^2C Bus is a registered trademark of Philips.

If you require this option, please specify so.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/80 group.

The M32C/80 group microcomputer contains RAM as memory to store instructions and data, CPU to execute calculations and peripheral functions as interrupt, timer, serial I/O, D-A converter, DMAC, CRC calculation circuit, A-D converter, HDLC, and I/O ports.

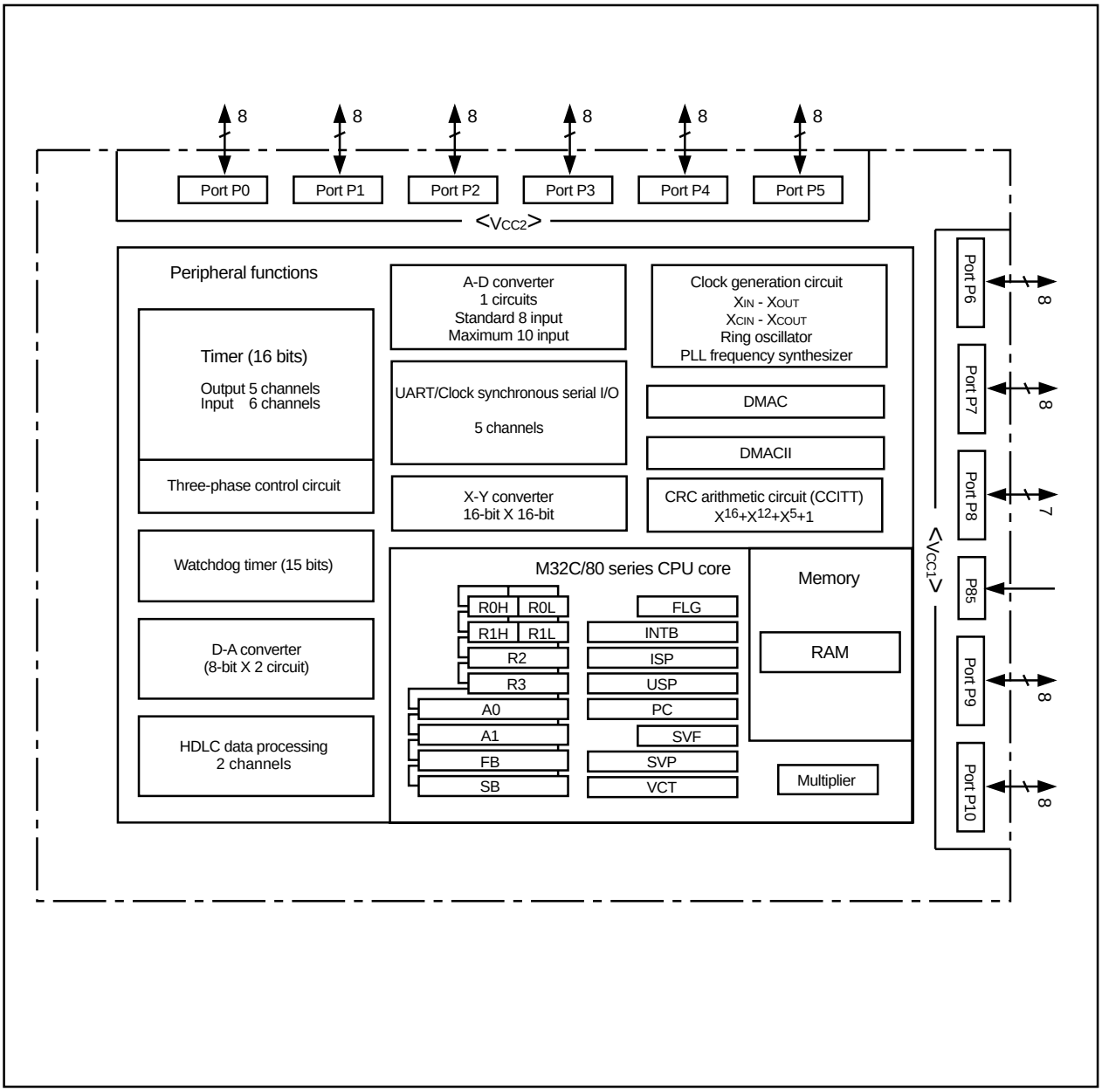


Figure 1.1 M32C/80 Group Block Diagram

1.4 Product Information

The M32C/80 group products are planned to release the following products.

(1) Support for external ROM version and external ROM version with Boot loader

(2) RAM capacity : Figure 1.2

(3) Package

100P6S-A : 0.65mm Pin Pitch Plastic molded QFP

100P6Q-A : 0.5mm Pin Pitch Plastic molded QFP

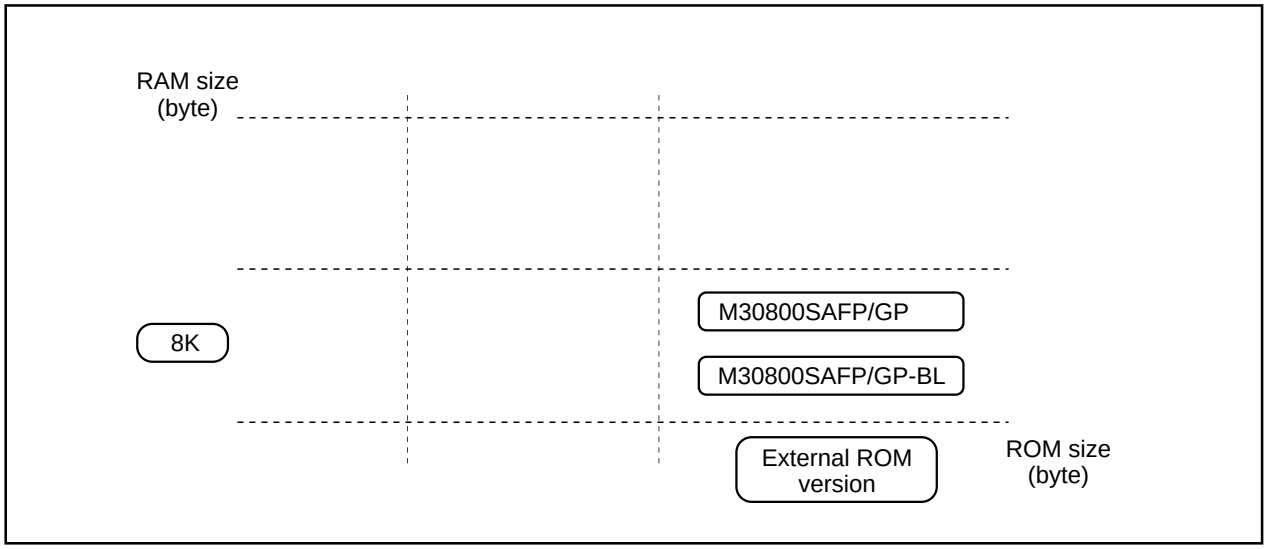


Figure 1.2. RAM expansion

The M32C/80 group products are listed in Table 1.2.

Table 1.2. M32C/80 group **As of May 2003**

Type No	ROM capacity	RAM capacity	Package type	Remarks
M30800SAFP **	-	8K	100P6S-A	External ROM version
M30800SAGP **			100P6Q-A	
M30800SAFP-BL ***			100P6S-A	External ROM version with Boot Loader
M30800SAGP-BL ***			100P6Q-A	

** :Under development

*** :Under planning

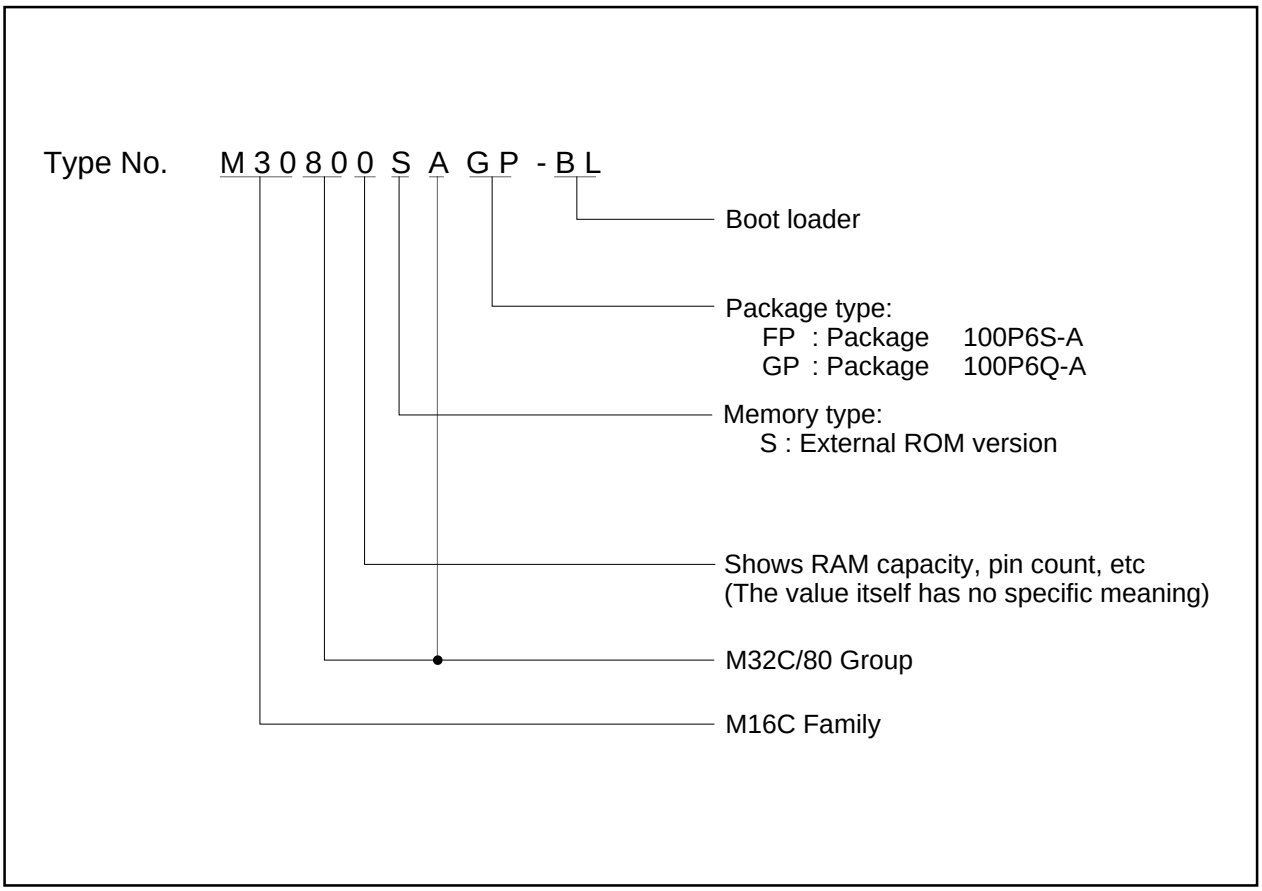


Figure 1.3 Product Numbering System

1.5 Pin Assignments

Figures 1.4 to 1.5 show pin assignments (top view), tables 1.3 to 1.4 list pin names.

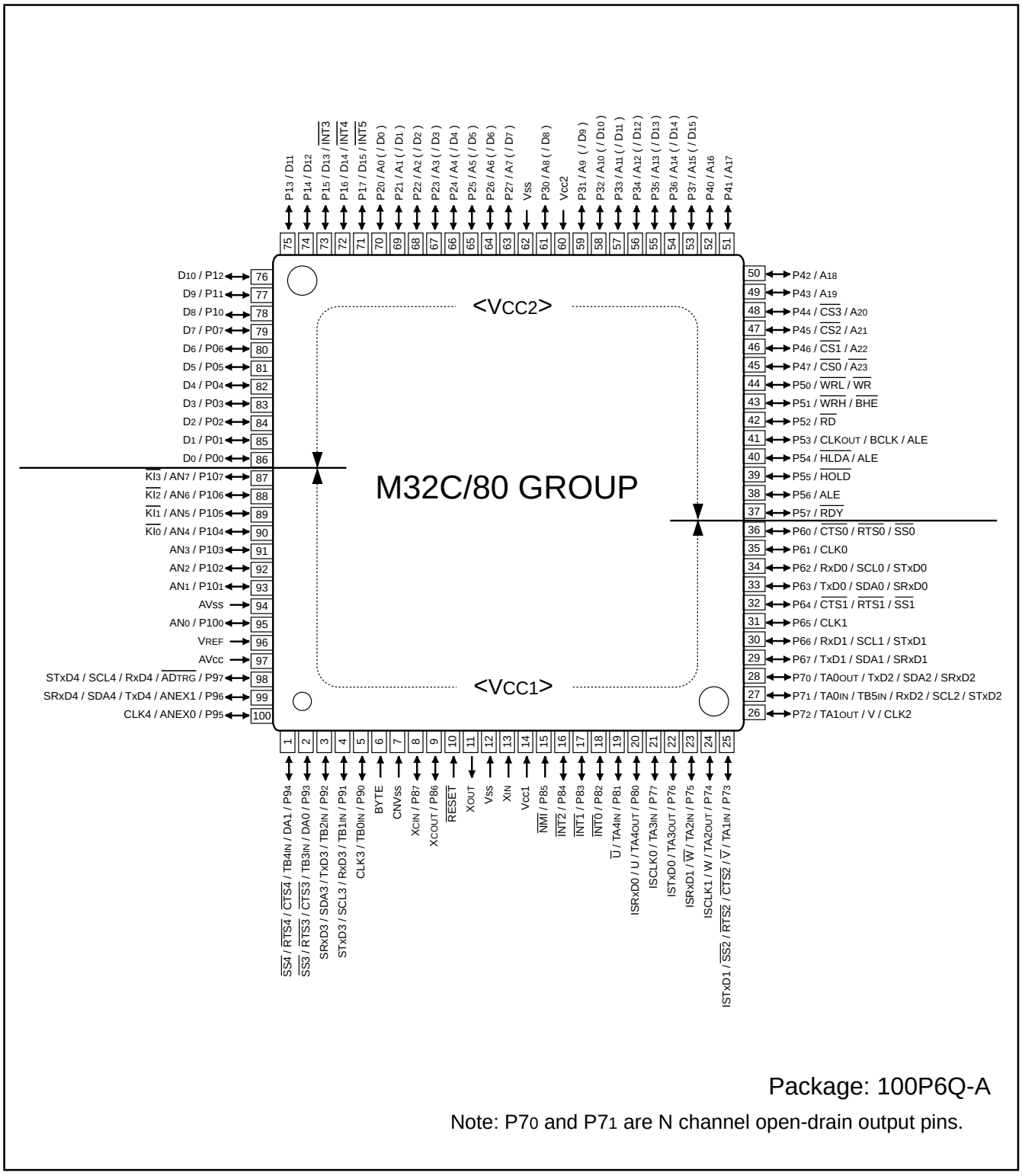
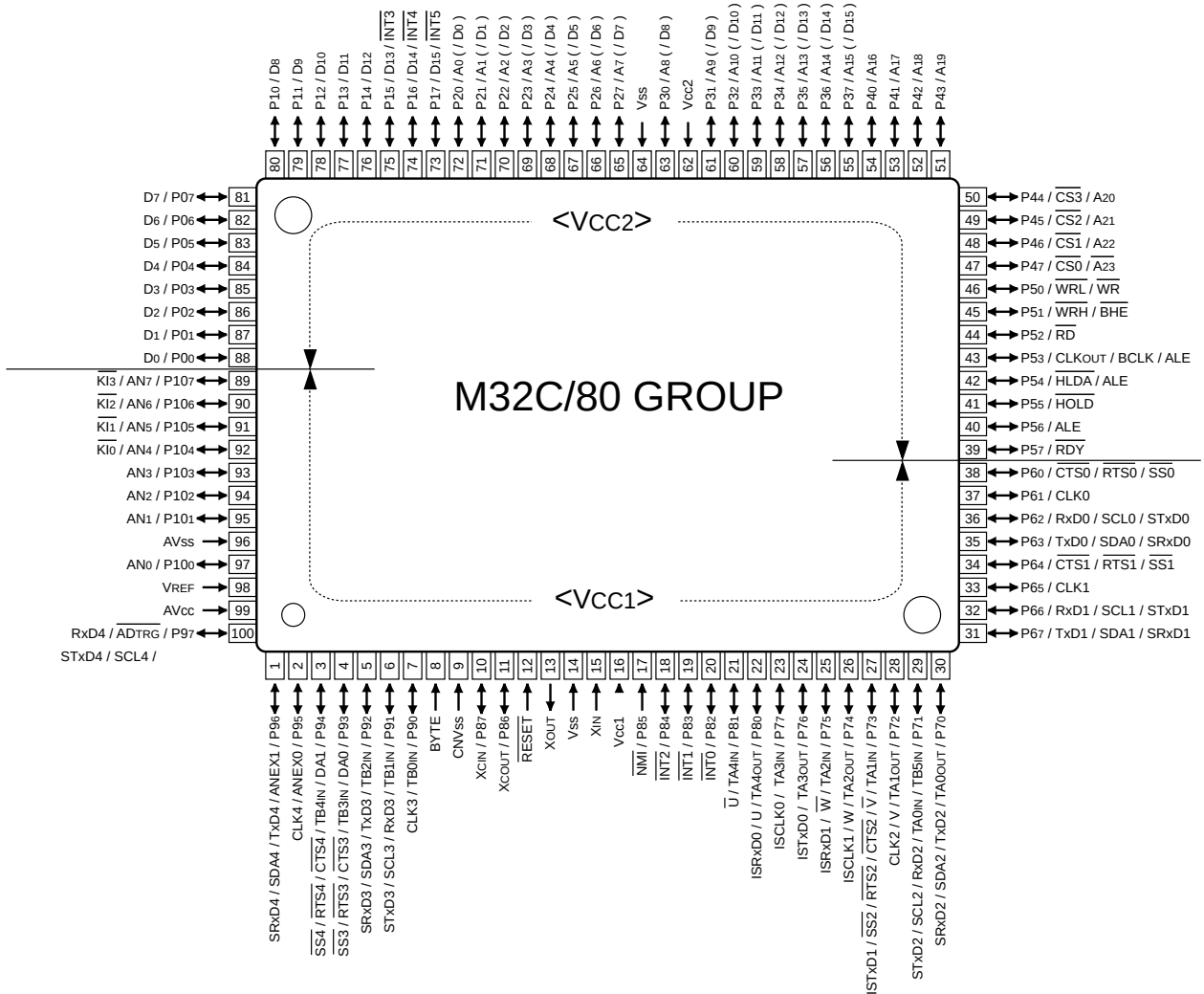


Figure 1.4 Pin assignment for 100-Pin Package



Package: 100P6S-A

Note: P70 and P71 are N channel open-drain output pins.

Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.3 Pin Characteristics for 100-Pin Package (1)

Package Pin No		Control pins	Port	Interrupt pins	Timer pins	UART pins	Analog pins	Bus control pins	HDLC pins
FP	GP								
1	99		P9$_6$			TxD4/SDA4/SRxD4	ANEX1		
2	100		P9$_5$			CLK4	ANEX0		
3	1		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$	DA1		
4	2		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$	DA0		
5	3		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3			
6	4		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3			
7	5		P9$_0$		TB0$_{IN}$	CLK3			
8	6	BYTE							
9	7	CNV$_{SS}$							
10	8	X$_{CIN}$	P8$_7$						
11	9	X$_{COUT}$	P8$_6$						
12	10	$\overline{RESET}$							
13	11	X$_{OUT}$							
14	12	V$_{SS}$							
15	13	X$_{IN}$							
16	14	V$_{CC1}$							
17	15		P8$_5$	$\overline{NMI}$					
18	16		P8$_4$	$\overline{INT2}$					
19	17		P8$_3$	$\overline{INT1}$					
20	18		P8$_2$	$\overline{INT0}$					
21	19		P8$_1$		TA4$_{IN}$/$\overline{U}$				
22	20		P8$_0$		TA4$_{OUT}$/U				ISRxD0
23	21		P7$_7$		TA3$_{IN}$				ISCLK0
24	22		P7$_6$		TA3$_{OUT}$				ISTxD0
25	23		P7$_5$		TA2$_{IN}$/$\overline{W}$				ISRxD1
26	24		P7$_4$		TA2$_{OUT}$/W				ISCLK1
27	25		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$			ISTxD1
28	26		P7$_2$		TA1$_{OUT}$/V	CLK2			
29	27		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2			
30	28		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2			
31	29		P6$_7$			TxD1/SDA1/SRxD1			
32	30		P6$_6$			RxD1/SCL1/STxD1			
33	31		P6$_5$			CLK1			
34	32		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$			
35	33		P6$_3$			TxD0/SDA0/SRxD0			
36	34		P6$_2$			RxD0/SCL0/STxD0			
37	35		P6$_1$			CLK0			
38	36		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
39	37		P5$_7$					$\overline{RDY}$	
40	38		P5$_6$					ALE	
41	39		P5$_5$					$\overline{HOLD}$	
42	40		P5$_4$					$\overline{HLDA}$/ALE	
43	41		P5$_3$					CLK$_{OUT}$/BCLK/ALE	
44	42		P5$_2$					$\overline{RD}$	
45	43		P5$_1$					$\overline{WRH}$/$\overline{BHE}$	
46	44		P5$_0$					$\overline{WRL}$/$\overline{WR}$	
47	45		P4$_7$					$\overline{CS0}$/A$_{23}$	
48	46		P4$_6$					$\overline{CS1}$/A$_{22}$	
49	47		P4$_5$					$\overline{CS2}$/A$_{21}$	
50	48		P4$_4$					$\overline{CS3}$/A$_{20}$	

P7$_0$ and P7$_1$ are N-channel open drain output.

Table 1.4 Pin Characteristics for 100-Pin Package (2)

Package pin No		Control pins	Port	Interrupt pins	Timer pins	UART pins	Analog pins	Bus control pins	HDLC pins
FP	GP								
51	49		P4$_3$					A$_{19}$	
52	50		P4$_2$					A$_{18}$	
53	51		P4$_1$					A$_{17}$	
54	52		P4$_0$					A$_{16}$	
55	53		P3$_7$					A$_{15}$(/D$_{15}$)	
56	54		P3$_6$					A$_{14}$(/D$_{14}$)	
57	55		P3$_5$					A$_{13}$(/D$_{13}$)	
58	56		P3$_4$					A$_{12}$(/D$_{12}$)	
59	57		P3$_3$					A$_{11}$(/D$_{11}$)	
60	58		P3$_2$					A$_{10}$(/D$_{10}$)	
61	59		P3$_1$					A$_9$(/D$_9$)	
62	60	V$_{CC2}$							
63	61		P3$_0$					A$_8$(/D$_8$)	
64	62	V$_{SS}$							
65	63		P2$_7$					A$_7$(/D$_7$)	
66	64		P2$_6$					A$_6$(/D$_6$)	
67	65		P2$_5$					A$_5$(/D$_5$)	
68	66		P2$_4$					A$_4$(/D$_4$)	
69	67		P2$_3$					A$_3$(/D$_3$)	
70	68		P2$_2$					A$_2$(/D$_2$)	
71	69		P2$_1$					A$_1$(/D$_1$)	
72	70		P2$_0$					A$_0$(/D$_0$)	
73	71		P1$_7$	$\overline{\text{INT5}}$				D$_{15}$	
74	72		P1$_6$	$\overline{\text{INT4}}$				D$_{14}$	
75	73		P1$_5$	$\overline{\text{INT3}}$				D$_{13}$	
76	74		P1$_4$					D$_{12}$	
77	75		P1$_3$					D$_{11}$	
78	76		P1$_2$					D$_{10}$	
79	77		P1$_1$					D$_9$	
80	78		P1$_0$					D$_8$	
81	79		P0$_7$					D$_7$	
82	80		P0$_6$					D$_6$	
83	81		P0$_5$					D$_5$	
84	82		P0$_4$					D$_4$	
85	83		P0$_3$					D$_3$	
86	84		P0$_2$					D$_2$	
87	85		P0$_1$					D$_1$	
88	86		P0$_0$					D$_0$	
89	87		P10$_7$	$\overline{\text{KI3}}$			AN$_7$		
90	88		P10$_6$	$\overline{\text{KI2}}$			AN$_6$		
91	89		P10$_5$	$\overline{\text{KI1}}$			AN$_5$		
92	90		P10$_4$	$\overline{\text{KI0}}$			AN$_4$		
93	91		P10$_3$				AN$_3$		
94	92		P10$_2$				AN$_2$		
95	93		P10$_1$				AN$_1$		
96	94	AV$_{SS}$							
97	95		P10$_0$				AN$_0$		
98	96						V$_{REF}$		
99	97	AV$_{CC}$							
100	98		P9$_7$			RxD4/SCL4/STxD4	$\overline{\text{ADTRG}}$		

1.6 Pin Description

Table 1.5 Pin Description (1)

Signal name	Pin name	I/O type	Supply voltage	Description
Power supply input	V_{CC1}, V_{CC2} V_{SS}	I	–	Connect both V_{CC1} and V_{CC2} pins to 3.0 to 5.5V. Connect the V_{SS} pin to 0V. $V_{CC1} \geq V_{CC2}$ (1)
Analog power supply input	AVCC AVSS	I	–	Applies the power supply for the A-D converter. Connect the AVCC pin to V_{CC1}. Connect the AVSS pin to V_{SS}.
Reset input	$\overline{RESET}$	I	V_{CC1}	The microcomputer is in a reset state when applying "L" to the this pin.
CNVSS	CNVSS	I	V_{CC1}	Switches processor mode. Connect this pin to V_{CC1} to start up in microprocessor mode.
External data bus width select input	BYTE	I	V_{CC1}	Switches the data bus in external memory space 3. The data bus is 16 bits long when the this pin is held "L" and 8 bits long when the this pin is held "H". Set it to either one.
Bus control pins	D_0 to D_7	I/O	V_{CC2}	Input and output data (D_0 to D_7) when these pins are set as the data bus.
	D_8 to D_{15}	I/O	V_{CC2}	Input and output data (D_8 to D_{15}) when these pins are set as the data bus.
	A_0 to A_{22}	O	V_{CC2}	Output address bits (A_0 to A_{22}).
	$\overline{A_{23}}$	O	V_{CC2}	The highest-order address bit A_{23} outputs inversely.
	A_0/D_0 to A_7/D_7	I/O	V_{CC2}	Input and output data (D_0 to D_7) and output 8 low-order address bits (A_0 to A_7) by time-sharing when these pins are set as the multiplexed bus.
	A_8/D_8 to A_{15}/D_{15}	I/O	V_{CC2}	Input and output data (D_8 to D_{15}) and output 8 middle-order address bits (A_8 to A_{15}) by time-sharing when external 16-bit data bus are set as the multiplexed bus.
	$\overline{CS0}$ to $\overline{CS3}$	O	V_{CC2}	Output $\overline{CS0}$ to $\overline{CS3}$ signals. $\overline{CS0}$ to $\overline{CS3}$ are chip-select signals to specify an external space.
	$\overline{WRL}/\overline{WR}$ $\overline{WRH}/\overline{BHE}$ $\overline{RD}$	O	V_{CC2}	Output $\overline{WRL}$, $\overline{WRH}$, ($\overline{WR}$, $\overline{BHE}$), $\overline{RD}$ signals. $\overline{WRL}$ and $\overline{WRH}$ or $\overline{BHE}$ and $\overline{WR}$ can be switched by program. ■ $\overline{WRL}$, $\overline{WRH}$ and $\overline{RD}$ are selected The $\overline{WRL}$ signal becomes "L" by writing data to an even address in an external memory space. The $\overline{WRH}$ signal becomes "L" by writing data to an odd address in an external memory space. The $\overline{RD}$ pin signal becomes "L" by reading data in an external memory space. ■ $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ are selected The $\overline{WR}$ signal becomes "L" by writing data in an external memory space. The $\overline{RD}$ signal becomes "L" by reading data in an external memory space. The $\overline{BHE}$ signal becomes "L" by accessing an odd address. Select $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ for an external 8-bit data bus.
	ALE	O	V_{CC2}	ALE is a signal to latch the address.
	$\overline{HOLD}$	I	V_{CC2}	While the $\overline{HOLD}$ pin is held "L", the microcomputer is placed in a hold state.
	$\overline{HLDA}$	O	V_{CC2}	In a hold state, $\overline{HLDA}$ outputs a "L" signal.
	$\overline{RDY}$	I	V_{CC2}	While applying a "L" signal to the $\overline{RDY}$ pin, the microcomputer is placed in a wait state.

I : Input O : Output I/O : Input and output

NOTES:

1. In this manual, hereafter, V_{CC} refers to V_{CC1} unless otherwise noted.

Table 1.6 Pin Description (2)

Signal name	Pin name	I/O type	Supply voltage	Description
Main clock input	XIN	I	VCC1	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To use the external clock, input the clock from XIN and leave XOUT open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To use the external clock, input the clock from XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	VCC1	
BCLK output	BCLK	O	VCC2	Outputs the BCLK signal.
Clock output	CLKOUT	O	VCC2	Outputs the main clock divided by 8 or divided by 32 or the clock having the same frequency as the sub clock from P53.
$\overline{INT}$ interrupt input	$\overline{INT0}$ to $\overline{INT5}$	I	VCC1	Input pins for the $\overline{INT}$ interrupt
$\overline{NMI}$ interrupt input	$\overline{NMI}$	I	VCC1	Input pin for the $\overline{NMI}$ interrupt. Pin states can be read by the P85 bit in the P8 register.
Timer A	TA0OUT to TA4OUT	I/O	VCC1	These are timer A0 to timer A4 I/O pins.
	TA0IN to TA3IN	I	VCC1	These are timer A0 to timer A4 input pins.
Timer B	TB0IN to TB5IN	I	VCC1	These are timer B0 to timer B5 input pins.
Three-phase motor control output	U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$	O	VCC1	These are Three-phase motor control output pins.
Serial I/O	$\overline{CTS0}$ to $\overline{CTS4}$	I	VCC1	These are send control input pins.
	$\overline{RTS0}$ to $\overline{RTS4}$	O	VCC1	These are receive control output pins.
	CLK0 to CLK4	I/O	VCC1	These are transfer clock I/O pins.
	RxD0 to RxD4	I	VCC1	These are serial data input pins.
	TxD0 to TxD4	O	VCC1	These are serial data output pins.(except TxD2 for the N-channel open drain output.)
IIC mode	SDA0 to SDA4	I/O	VCC1	These are serial data I/O pins.(except SDA2 for the N-channel open drain output.)
	SCL0 to SCL4	I/O	VCC1	These are transfer clock I/O pins.(except SCL2 for the N-channel open drain output.)
Serial interface special function	STxD0 to STxD4	I/O	VCC1	These are serial data I/O pins.(except SDA2 for the N-channel open drain output.)
	SRxD0 to SRxD4	I	VCC1	These are serial data input pins.
	RxD0 to RxD4	I	VCC1	These are serial interface special function control pins.
HDLC	ISCLK0,ISCLK1	I/O	VCC1	These are HDLC transfer clock I/O pins.
	ISTxD0,ISTxD1	O	VCC1	These are HDLC data output pins.
	ISRxD0,ISRxD1	I	VCC1	These are HDLC data input pins.

I : Input O : Output I/O : Input and output

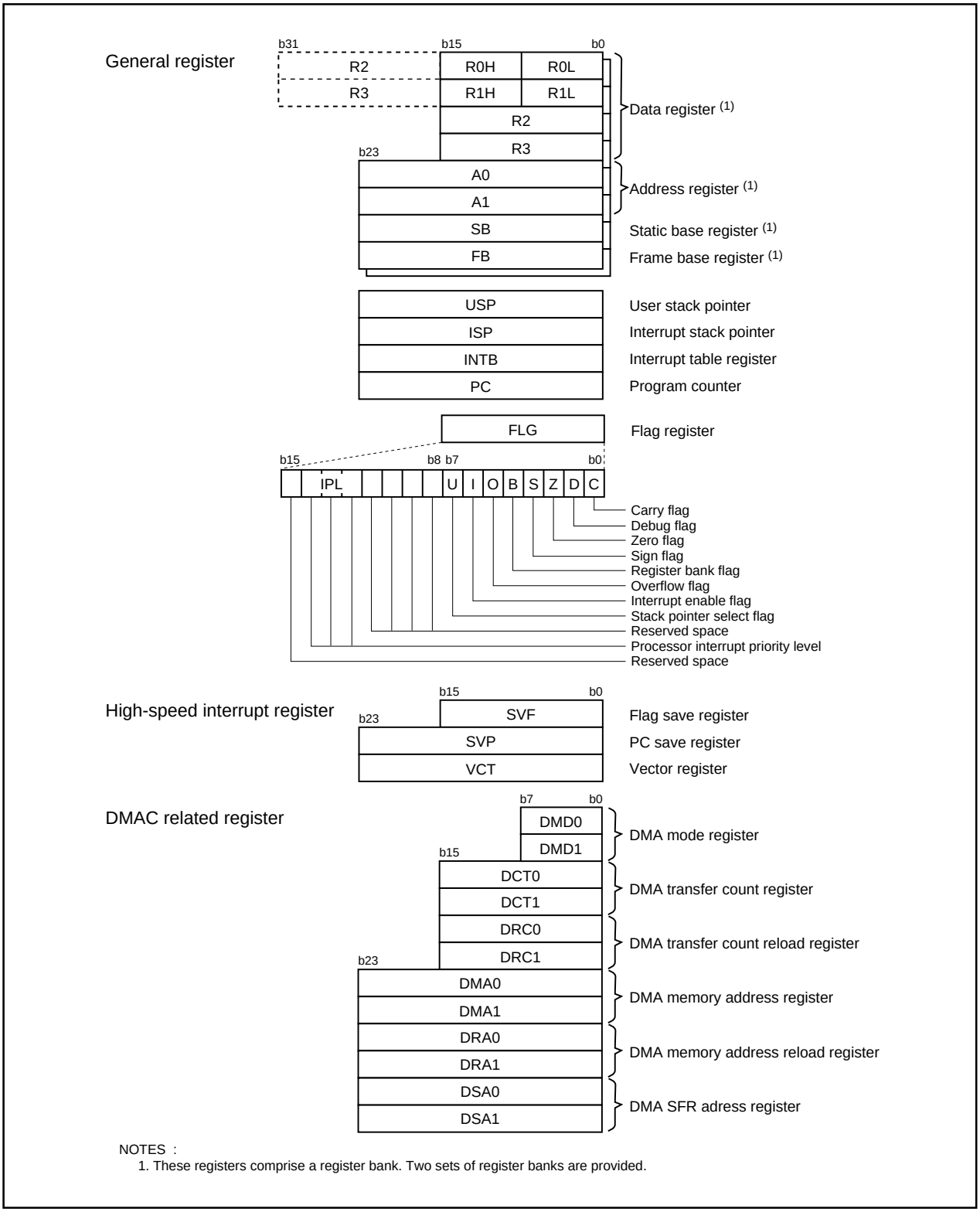
Table 1.7 Pin Description(3)

Signal name	Pin name	I/O type	Supply voltage	Description
Reference voltage input	V_{REF}	I	–	Applies the reference voltage for the A-D converter.
A-D converter	AN_0 to AN_7	I	V_{CC1}	Analog input pins for the A-D converter
	$\overline{ADTRG}$	I	V_{CC1}	This is an A-D trigger input pin.
	ANEX0	I/O	V_{CC1}	This is the extended analog I/O pins for the A-D converter.
	ANEX1	I	V_{CC1}	This is the extended analog input pin for the A-D converter.
D-A converter	DA0, DA1	O	V_{CC1}	This is the Input pin for the D-A converter
I/O port	$P0_0$ to $P0_7$ $P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$ $P4_0$ to $P4_7$ $P5_0$ to $P5_7$	I/O	V_{CC2}	These are 8-bit CMOS I/O ports. Each port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program.
	$P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P9_0$ to $P9_7$ $P10_0$ to $P10_7$	I/O	V_{CC1}	8-bit I/O ports having equivalent functions to P0 (except $P7_0$ and $P7_1$ for the N-channel open drain output.)
	$P8_0$ to $P8_4$, $P8_6$, $P8_7$	I/O	V_{CC1}	I/O ports having equivalent functions to P0
	$P8_5/\overline{NMI}$	I	V_{CC1}	Pin states can be read by the P8_5 bit in the P8 register.
Key input interrupt	$\overline{KI_0}$ to $\overline{KI_3}$	I	V_{CC1}	These are the key input interrupt pins.

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.
A register bank is comprised by 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers.
Two sets of the register banks are provided.



NOTES :
1. These registers comprise a register bank. Two sets of register banks are provided.

Figure 2.1 CPU Register

2.1 General Register

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be divided into high-order bits (R0H) and low-order bits (R0L) to use them as 8-bit data registers.
R0 can be combined with R2 to use the combined one as a 32-bit data register (R2R0) as well as R3R1.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operation.

2.1.3 Static Base Register (SB)

SB is a 24-bit registers for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC is 24 bits wide. It indicates an address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register to indicate a starting address of an interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

USP and ISP as the stack pointer are 24 bits wide. The U flag can switch USP to ISP and vice versa. Refer to the paragraph "Flag Register (FLG)" about the U flag. USP and ISP should be set to an even number to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register to indicate a CPU state.

- **Carry Flag (C)**
  The C flag indicates whether the carry or borrow occurs after an instruction is executed.

- **Debug Flag (D)**
  The D flag is for debug only. It should be set to "0".

- **Zero Flag (Z)**
  The Z flag is set to "1" when a value of zero is obtained from an arithmetic calculation; otherwise "0".

- **Sign Flag (S)**
  The S flag is set to "1" when a negative value is obtained from an arithmetic calculation; otherwise "0".

- **Register Bank Select Flag (B)**
  The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

- **Overflow Flag (O)**
  The O flag is set to "1" when a result of an arithmetic operation overflows; otherwise "0".

- **Interrupt Enable Flag (I)**
  The I flag enables a maskable interrupt.
  An interrupt is disabled when the I flag is set to "0" and is enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

- **Stack Pointer Select Flag (U)**
  ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".
  The U flag is set to "0" when the hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

- **Processor Interrupt Priority Level (IPL)**
  IPL is 3 bits wide. It assigns an interrupt priority levels from level 0 to level 7.
  If a requested interrupt has a greater priority than IPL, the interrupt is enabled.

- **Reserved Space**
  When write, the reserved space should be set to "0". When read, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated to the high-speed interrupt are as follows. Refer to the paragraph "High-speed Interrupt" for details.

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-associated Registers

Registers associated to DMAC are as follows. Refer to the section "DMAC" for details.

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/80 group.

Total address space is 16 Mbytes wide from addresses 000000$_{16}$ to FFFFFF$_{16}$.

The internal ROM is allocated in lower addresses beginning with address FFFFFF$_{16}$. For example, a 64-Kbyte internal ROM is allocated in addresses from FF0000$_{16}$ to FFFFFF$_{16}$.

The fixed interrupt vectors are allocated in addresses from FFFFDC$_{16}$ to FFFFFF$_{16}$. It stores the starting address of each interrupt routine. Refer to "**10. Interrupt**" for details.

The internal RAM is allocated in higher addresses beginning with address 000400$_{16}$. For example, a 8-Kbyte internal RAM are allocated in addresses from 000400$_{16}$ to 0023FF$_{16}$. It stores data, calls the subroutine and becomes stacks when an interrupt is acknowledged.

The SFR is allocated in addresses from 000000$_{16}$ to 0003FF$_{16}$. The control registers for the peripheral function such as I/O port, A-D conversion, serial I/O, timer are allocated here. All addresses, which have nothing allocated within the SFR, are reserved space and cannot be accessed by users.

The special page vectors are allocated in addresses FFFE00$_{16}$ to FFFFDB$_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to Renesas publication "**Software Manual**" for details.

In memory expansion and microprocessor modes, some spaces are reserved for future use and cannot be used by users.

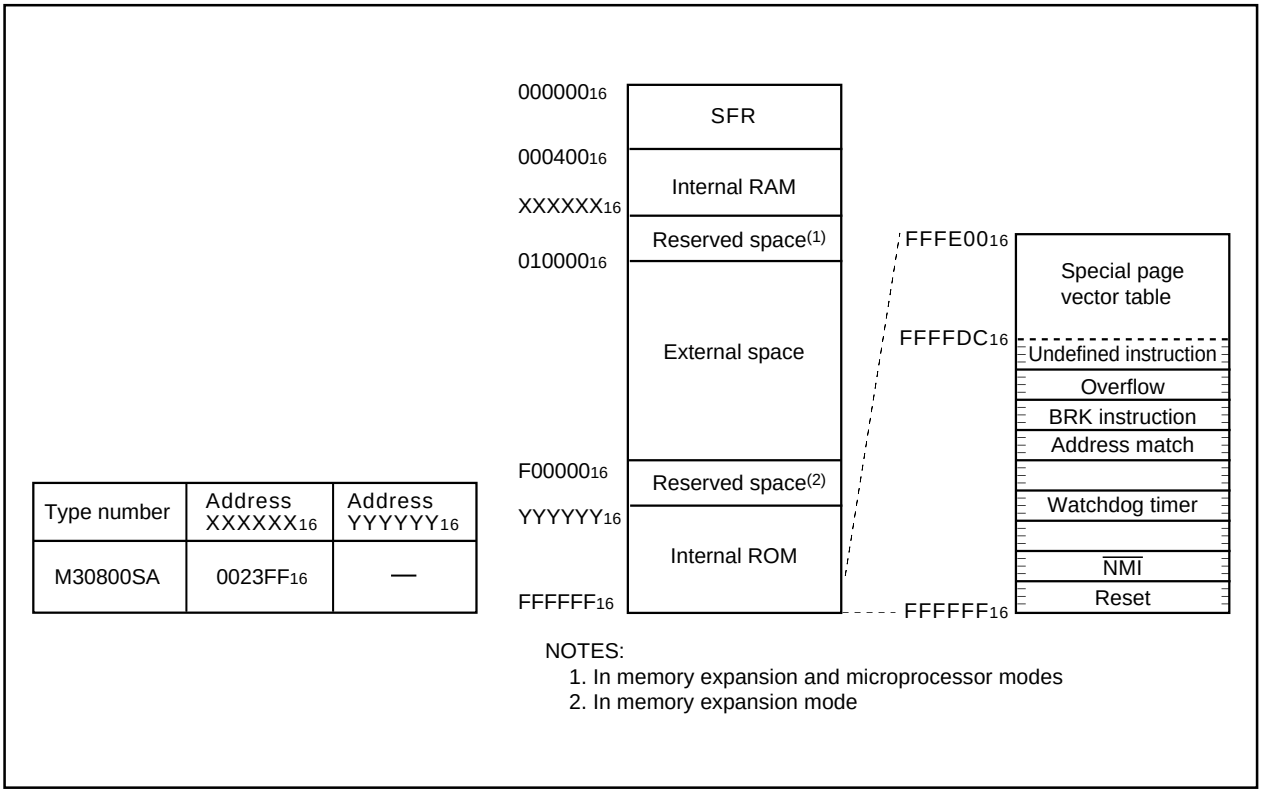


Figure 3.1 Memory Map

4. Special Function Registers (SFR)

Table 4.1. SFR table(1)

Address	Register	Symbol	Value after RESET	
000016				
000116				
000216				
000316				
000416	Processor mode register 0 (Note 2)	PM0	1000 00002(CNVss pin ="L") 0000 00112(CNVss pin ="H")	
000516	Processor mode register 1	PM1	0X00 00002	
000616	System clock control register 0	CM0	0000 X0002	
000716	System clock control register 1	CM1	0010 00002	
000816				
000916	Address match interrupt enable register	AIER	0000 00002	
000A16	Protect register	PRCR	XXXX 00002	
000B16	External data bus width control register	DS	XXXX 10002(BYTE pin ="L") XXXX 00002(BYTE pin ="H")	
000C16	Main clock division register	MCD	XXX0 10002	
000D16	Oscillation stop detect register	CM2	0000 00002	
000E16	Watchdog timer start register	WDTS	XX16	
000F16	Watchdog timer control register (Note 3)	WDC	000X XXXX2	
001016 001116 001216	Address match interrupt register 0	RMAD0	0000 00002 0000 00002 0000 00002	
001316	Processor mode register 2	PM2	XXXX X0002	
001416 001516 001616	Address match interrupt register 1	RMAD1	0000 00002 0000 00002 0000 00002	
001716	Voltage detection register 2 (Note 4)	VCR2	0000 00002	
001816 001916 001A16	Address match interrupt register 2	RMAD2	0000 00002 0000 00002 0000 00002	
001B16	Voltage detection register 1 (Note 4)	VCR1	0000 10002	
001C16 001D16 001E16	Address match interrupt register 3	RMAD3	0000 00002 0000 00002 0000 00002	
001F16	Voltage detection register 0	VCR0	0000 00002	*
002016				
002116				
002216				
002316				
002416				
002516				
002616	PLL control register 0	PLC0	0001 X0102	
002716	PLL control register 1	PLC1	000X 00002	
002816 002916 002A16	Address match interrupt register 4	RMAD4	0000 00002 0000 00002 0000 00002	
002B16	RAM test register 0	RAMT0	0000 00002	*
002C16 002D16 002E16	Address match interrupt register 5	RMAD5	0000 00002 0000 00002 0000 00002	
002F16	Voltage down detection interrupt register	D4INT	0000 00002	

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. The PM00 and PM01 bits do not change at software reset, watchdog timer reset.
3. The WDC5 bit is “0” (cold start) immediately after power-on. It can only be set to “1” in a program. It is set to “0” when the input voltage at the VCC1 pin drops to Vdet2 or less while the VC25 bit in the VCR2 register is set to “1” (RAM retention limit detection circuit enable).
4. This register does not change at software reset, watchdog timer reset.

X : Nothing is mapped to this bit. Users cannot use any symbols with *. No access is allowed.

Table 4.2. SFR table(2)

Address	Register	Symbol	Value after RESET
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆	Address match interrupt register 6	RMAD6	0000 0000₂
0039₁₆			0000 0000₂
003A₁₆			0000 0000₂
003B₁₆			
003C₁₆	Address match interrupt register 7	RMAD7	0000 0000₂
003D₁₆			0000 0000₂
003E₁₆			0000 0000₂
003F₁₆			
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆	External area wait control register 0	EWCR0	X0X0 0011₂
0049₁₆	External area wait control register 1	EWCR1	X0X0 0011₂
004A₁₆	External area wait control register 2	EWCR2	X0X0 0011₂
004B₁₆	External area wait control register 3	EWCR3	X0X0 0011₂
004C₁₆	Page mode wait control register 0	PWCR0	0001 0001₂
004D₁₆	Page mode wait control register 1	PWCR1	0001 0001₂
004E₁₆			
004F₁₆			
0050₁₆			
0051₁₆			
0052₁₆			
0053₁₆			
0054₁₆			
0055₁₆			
0056₁₆			
0057₁₆			
0058₁₆			
0059₁₆			
005A₁₆			
005B₁₆			
005C₁₆			
005D₁₆			
005E₁₆			
005F₁₆			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.3. SFR table(3)

Address	Register	Symbol	Value after RESET
006016			
006116			
006216			
006316			
006416			
006516			
006616			
006716			
006816	DMA0 interrupt control register	DM0IC	XXXX X0002
006916	Timer B5 interrupt control register	TB5IC	XXXX X0002
006A16	DMA2 interrupt control register	DM2IC	XXXX X0002
006B16	UART2 receive /ACK interrupt control register	S2RIC	XXXX X0002
006C16	Timer A0 interrupt control register	TA0IC	XXXX X0002
006D16	UART3 receive /ACK interrupt control register	S3RIC	XXXX X0002
006E16	Timer A2 interrupt control register	TA2IC	XXXX X0002
006F16	UART4 receive /ACK interrupt control register	S4RIC	XXXX X0002
007016	Timer A4 interrupt control register	TA4IC	XXXX X0002
007116	UART0/UART3 bus conflict detect interrupt control register	BCN0IC/BCN3IC	XXXX X0002
007216	UART0 receive/ACK interrupt control register	S0RIC	XXXX X0002
007316	A-D0 interrupt control register	AD0IC	XXXX X0002
007416	UART1 receive/ACK interrupt control register	S1RIC	XXXX X0002
007516	Intelligent I/O interrupt control register 0	IIO0IC	XXXX X0002
007616	Timer B1 interrupt control register	TB1IC	XXXX X0002
007716	Intelligent I/O interrupt control register 2	IIO2IC	XXXX X0002
007816	Timer B3 interrupt control register	TB3IC	XXXX X0002
007916			
007A16	INT5 interrupt control register	INT5IC	XX00 X0002
007B16			
007C16	INT3 interrupt control register	INT3IC	XX00 X0002
007D16			
007E16	INT1 interrupt control register	INT1IC	XX00 X0002
007F16			
008016			
008116			
008216			
008316			
008416			
008516			
008616			
008716			
008816	DMA1 interrupt control register	DM1IC	XXXX X0002
008916	UART2 transmit /NACK interrupt control register	S2TIC	XXXX X0002
008A16	DMA3 interrupt control register	DM3IC	XXXX X0002
008B16	UART3 transmit /NACK interrupt control register	S3TIC	XXXX X0002
008C16	Timer A1 interrupt control register	TA1IC	XXXX X0002
008D16	UART4 transmit /NACK interrupt control register	S4TIC	XXXX X0002
008E16	Timer A3 interrupt control register	TA3IC	XXXX X0002
008F16	UART2 bus conflict detect interrupt control register	BCN2IC	XXXX X0002

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.4. SFR table(4)

Address	Register	Symbol	Value after RESET
009016	UART0 transmit /NACK interrupt control register	S0TIC	XXXX X0002
009116	UART1/UART4 bus conflict detect interrupt control register	BCN1IC/BCN4IC	XXXX X0002
009216	UART1 transmit/NACK interrupt control register	S1TIC	XXXX X0002
009316	Key input interrupt control register	KUPIC	XXXX X0002
009416	Timer B0 interrupt control register	TB0IC	XXXX X0002
009516	Intelligent I/O interrupt control register 1	IIO1IC	XXXX X0002
009616	Timer B2 interrupt control register	TB2IC	XXXX X0002
009716	Intelligent I/O interrupt control register 3	IIO3IC	XXXX X0002
009816	Timer B4 interrupt control register	TB4IC	XXXX X0002
009916			
009A16	INT4 interrupt control register	INT4IC	XX00 X0002
009B16			
009C16	INT2 interrupt control register	INT2IC	XX00 X0002
009D16			
009E16	INT0 interrupt control register	INT0IC	XX00 X0002
009F16	Exit priority register	RLVL	XX0X 00002
00A016	Interrupt request register 0	IIO0IR	0000 000X2
00A116	Interrupt request register 1	IIO1IR	0000 000X2
00A216	Interrupt request register 2	IIO2IR	0000 000X2
00A316	Interrupt request register 3	IIO3IR	0000 000X2
00A416			
00A516			
00A616			
00A716			
00A816			
00A916			
00AA16			
00AB16			
00AC16			
00AD16			
00AE16			
00AF16			
00B016	Interrupt enable register 0	IIO0IE	0000 00002
00B116	Interrupt enable register 1	IIO1IE	0000 00002
00B216	Interrupt enable register 2	IIO2IE	0000 00002
00B316	Interrupt enable register 3	IIO3IE	0000 00002
00B416			
00B516			
00B616			
00B716			
00B816			
00B916			
00BA16			
00BB16			
00BC16			
00BD16			
00BE16			
00BF16			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.5. SFR table(5)

Address	Register	Symbol	Value after RESET
00C0$_{16}$			
00C1$_{16}$			
00C2$_{16}$			
00C3$_{16}$			
00C4$_{16}$			
00C5$_{16}$			
00C6$_{16}$			
00C7$_{16}$			
00C8$_{16}$			
00C9$_{16}$			
00CA$_{16}$			
00CB$_{16}$			
00CC$_{16}$			
00CD$_{16}$			
00CE$_{16}$			
00CF$_{16}$			
00D0$_{16}$			
00D1$_{16}$			
00D2$_{16}$			
00D3$_{16}$			
00D4$_{16}$			
00D5$_{16}$			
00D6$_{16}$			
00D7$_{16}$			
00D8$_{16}$			
00D9$_{16}$			
00DA$_{16}$			
00DB$_{16}$			
00DC$_{16}$			
00DD$_{16}$			
00DE$_{16}$			
00DF$_{16}$			
00E0$_{16}$			
00E1$_{16}$			
00E2$_{16}$			
00E3$_{16}$			
00E4$_{16}$			
00E5$_{16}$			
00E6$_{16}$			
00E7$_{16}$			
00E8$_{16}$ 00E9$_{16}$	SI/O receive buffer register 0	G0RB	XXXX XXXX$_2$ XX00 XXXX$_2$
00EA$_{16}$	Transmit buffer/ receive data register 0	G0TB	XX$_{16}$
00EB$_{16}$			
00EC$_{16}$	Receive input register 0	G0RI	XX$_{16}$
00ED$_{16}$	SI/O communication mode register 0	G0MR	0000 0000$_2$
00EE$_{16}$	Transmit output register 0	G0TO	XX$_{16}$
00EF$_{16}$	SI/O communication control register 0	G0CR	0000 X011$_2$

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.6. SFR table(6)

Address	Register	Symbol	Value after RESET
00F0$_{16}$	Data compare register 00	G0CMP0	XX$_{16}$
00F1$_{16}$	Data compare register 01	G0CMP1	XX$_{16}$
00F2$_{16}$	Data compare register 02	G0CMP2	XX$_{16}$
00F3$_{16}$	Data compare register 03	G0CMP3	XX$_{16}$
00F4$_{16}$	Data mask register 00	G0MSK0	XX$_{16}$
00F5$_{16}$	Data mask register 01	G0MSK1	XX$_{16}$
00F6$_{16}$	Communication clock select register	CCS	XXXX 0000$_2$
00F7$_{16}$			
00F8$_{16}$ 00F9$_{16}$	Receive CRC code register 0	G0RCRC	XX$_{16}$ XX$_{16}$
00FA$_{16}$ 00FB$_{16}$	Transmit CRC code register 0	G0TCRC	00$_{16}$ 00$_{16}$
00FC$_{16}$	SI/O expansion mode register 0	G0EMR	0000 0000$_2$
00FD$_{16}$	SI/O expansion receive control register 0	G0ERC	0000 0000$_2$
00FE$_{16}$	SI/O special communication interrupt detect register 0	G0IRF	0000 00XX$_2$
00FF$_{16}$	SI/O expansion transmit control register 0	G0ETC	0000 0XXX$_2$
0100$_{16}$			
0101$_{16}$			
0102$_{16}$			
0103$_{16}$			
0104$_{16}$			
0105$_{16}$			
0106$_{16}$			
0107$_{16}$			
0108$_{16}$			
0109$_{16}$			
010A$_{16}$			
010B$_{16}$			
010C$_{16}$			
010D$_{16}$			
010E$_{16}$			
010F$_{16}$			
0110$_{16}$			
0111$_{16}$			
0112$_{16}$			
0113$_{16}$			
0114$_{16}$			
0115$_{16}$			
0116$_{16}$			
0117$_{16}$			
0118$_{16}$			
0119$_{16}$			
011A$_{16}$			
011B$_{16}$			
011C$_{16}$			
011D$_{16}$			
011E$_{16}$			
011F$_{16}$			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.7. SFR table(7)

Address	Register	Symbol	Value after RESET
0120₁₆			
0121₁₆			
0122₁₆			
0123₁₆			
0124₁₆			
0125₁₆			
0126₁₆			
0127₁₆			
0128₁₆ 0129₁₆	SI/O receive buffer register 1	G1RB	XXXX XXXX₂ XX00 XXXX₂
012A₁₆	SI/O transmit buffer/ receive data register 1	G1TB	XX₁₆
012B₁₆			
012C₁₆	Receive input register 1	G1RI	XX₁₆
012D₁₆	SI/O communication mode register 1	G1MR	0000 0000₂
012E₁₆	Transmit output register 1	G1TO	XX₁₆
012F₁₆	SI/O communication control register 1	G1CR	0000 X011₂
0130₁₆	Data compare register 10	G1CMP0	XX₁₆
0131₁₆	Data compare register 11	G1CMP1	XX₁₆
0132₁₆	Data compare register 12	G1CMP2	XX₁₆
0133₁₆	Data compare register 13	G1CMP3	XX₁₆
0134₁₆	Data mask register 10	G1MSK0	XX₁₆
0135₁₆	Data mask register 11	G1MSK1	XX₁₆
0136₁₆			
0137₁₆			
0138₁₆ 0139₁₆	Receive CRC code register 1	G1RCRC	XX₁₆ XX₁₆
013A₁₆ 013B₁₆	Transmit CRC code register 1	G1TCRC	00₁₆ 00₁₆
013C₁₆	SI/O expansion mode register 1	G1EMR	0000 0000₂
013D₁₆	SI/O expansion receive control register 1	G1ERC	0000 0000₂
013E₁₆	SI/O special communication interrupt detect register 1	G1IRF	0000 00XX₂
013F₁₆	SI/O expansion transmit control register 1	G1ETC	0000 0XXX₂
0140₁₆			
0141₁₆			
0142₁₆			
0143₁₆			
0144₁₆			
0145₁₆			
0146₁₆			
0147₁₆			
0148₁₆			
0149₁₆			
014A₁₆			
014B₁₆			
014C₁₆			
014D₁₆			
014E₁₆			
014F₁₆			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.8. SFR table(8)

Address	Register	Symbol	Value after RESET
0150₁₆			
0151₁₆			
0152₁₆			
0153₁₆			
0154₁₆			
0155₁₆			
0156₁₆			
0157₁₆			
0158₁₆			
0159₁₆			
015A₁₆			
015B₁₆			
015C₁₆			
015D₁₆			
015E₁₆			
015F₁₆			
0160₁₆			
0161₁₆			
0162₁₆			
0163₁₆			
0164₁₆			
0165₁₆			
0166₁₆			
0167₁₆			
0168₁₆			
0169₁₆			
016A₁₆			
016B₁₆			
016C₁₆			
016D₁₆			
016E₁₆			
016F₁₆			
0170₁₆			
0171₁₆			
0172₁₆			
0173₁₆			
0174₁₆			
0175₁₆			
0176₁₆			
0177₁₆			
0178₁₆			
0179₁₆			
017A₁₆			
017B₁₆			
≈			≈

NOTES:
1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.-9. SFR table(9)

Address	Register	Symbol	Value after RESET
01E0$_{16}$			
01E1$_{16}$			
01E2$_{16}$			
01E3$_{16}$			
01E4$_{16}$			
01E5$_{16}$			
01E6$_{16}$			
01E7$_{16}$			
01E8$_{16}$			
01E9$_{16}$			
01EA$_{16}$			
01EB$_{16}$			
01EC$_{16}$			
01ED$_{16}$			
01EE$_{16}$			
01EF$_{16}$			
01F0$_{16}$			
01F1$_{16}$			
01F2$_{16}$			
01F3$_{16}$			
01F4$_{16}$			
01F5$_{16}$			
01F6$_{16}$			
01F7$_{16}$			
01F8$_{16}$			
01F9$_{16}$			
01FA$_{16}$			
01FB$_{16}$			
01FC$_{16}$			
01FD$_{16}$			
01FE$_{16}$			
01FF$_{16}$			
0200$_{16}$			
0201$_{16}$			
0202$_{16}$			
0203$_{16}$			
0204$_{16}$			
0205$_{16}$			
0206$_{16}$			
0207$_{16}$			
0208$_{16}$			
0209$_{16}$			
020A$_{16}$			
020B$_{16}$			
020C$_{16}$			
020D$_{16}$			
020E$_{16}$			
020F$_{16}$			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.10. SFR table(10)

Address	Register	Symbol	Value after RESET
0210$_{16}$			
0211$_{16}$			
0212$_{16}$			
0213$_{16}$			
0214$_{16}$			
0215$_{16}$			
0216$_{16}$			
0217$_{16}$			
0218$_{16}$			
0219$_{16}$			
021A$_{16}$			
021B$_{16}$			
021C$_{16}$			
021D$_{16}$			
021E$_{16}$			
021F$_{16}$			
0220$_{16}$			
0221$_{16}$			
0222$_{16}$			
0223$_{16}$			
0224$_{16}$			
0225$_{16}$			
0226$_{16}$			
0227$_{16}$			
0228$_{16}$			
0229$_{16}$			
022A$_{16}$			
022B$_{16}$			
022C$_{16}$			
022D$_{16}$			
022E$_{16}$			
022F$_{16}$			
0230$_{16}$			
0231$_{16}$			
0232$_{16}$			
0233$_{16}$			
0234$_{16}$			
0235$_{16}$			
0236$_{16}$			
0237$_{16}$			
0238$_{16}$			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.11. SFR table(11)

Address	Register	Symbol	Value after RESET
0239₁₆			
023A₁₆			
023B₁₆			
023C₁₆			
023D₁₆			
023E₁₆			
023F₁₆			
0240₁₆			
0241₁₆			
0242₁₆			
0243₁₆			
0244₁₆			
0245₁₆			
0246₁₆			
0247₁₆			
0248₁₆			
0249₁₆			
024A₁₆			
024B₁₆			
024C₁₆			
024D₁₆			
024E₁₆			
024F₁₆			
0250₁₆			
0251₁₆			
0252₁₆			
0253₁₆			
0254₁₆			
0255₁₆			
0256₁₆			
0257₁₆			
0258₁₆			
0259₁₆			
025A₁₆			
025B₁₆			
025C₁₆			
025D₁₆			
025E₁₆			
025F₁₆			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.12. SFR table(12)

Address	Register	Symbol	Value after RESET
026016			
026116			
026216			
026316			
026416			
026516			
026616			
026716			
026816			
026916			
026A16			
026B16			
026C16			
026D16			
026E16			
026F16			
027016			
027116			
027216			
027316			
027416			
027516			
027616			
027716			
027816			
027916			
027A16			
027B16			
027C16			
027D16			
027E16			
027F16			
028016			
028116			
028216			
028316			
028416			
028516			
028616			
028716			
028816			
028916			
028A16			
028B16			
028C16			
028D16			
028E16			
028F16			

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
X : Nothing is mapped to this bit.

Table 4.13. SFR table(13)

Address	Register	Symbol	Value after RESET
0290₁₆			
0291₁₆			
0292₁₆			
0293₁₆			
0294₁₆			
0295₁₆			
0296₁₆			
0297₁₆			
0298₁₆			
0299₁₆			
029A₁₆			
029B₁₆			
029C₁₆			
029D₁₆			
029E₁₆			
029F₁₆			
02A0₁₆			
02A1₁₆			
02A2₁₆			
02A3₁₆			
02A4₁₆			
02A5₁₆			
02A6₁₆			
02A7₁₆			
02A8₁₆			
02A9₁₆			
02AA₁₆			
02AB₁₆			
02AC₁₆			
02AD₁₆			
02AE₁₆			
02AF₁₆			
02B0₁₆			
02B1₁₆			
02B2₁₆			
02B3₁₆			
02B4₁₆			
02B5₁₆			
02B6₁₆			
02B7₁₆			
02B8₁₆			

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
X : Nothing is mapped to this bit.

Table 4.14. SFR table(14)

Address	Register	Symbol	Value after RESET
02B9$_{16}$			
02BA$_{16}$			
02BB$_{16}$			
02BC$_{16}$			
02BD$_{16}$			
02BE$_{16}$			
02BF$_{16}$			
02C0$_{16}$	X0 register/Y0 register	X0R,Y0R	XX$_{16}$
02C1$_{16}$			XX$_{16}$
02C2$_{16}$	X1 register/Y1 register	X1R,Y1R	XX$_{16}$
02C3$_{16}$			XX$_{16}$
02C4$_{16}$	X2 register/Y2 register	X2R,Y2R	XX$_{16}$
02C5$_{16}$			XX$_{16}$
02C6$_{16}$	X3 register/Y3 register	X3R,Y3R	XX$_{16}$
02C7$_{16}$			XX$_{16}$
02C8$_{16}$	X4 register/Y4 register	X4R,Y4R	XX$_{16}$
02C9$_{16}$			XX$_{16}$
02CA$_{16}$	X5 register/Y5 register	X5R,Y5R	XX$_{16}$
02CB$_{16}$			XX$_{16}$
02CC$_{16}$	X6 register/Y6 register	X6R,Y6R	XX$_{16}$
02CD$_{16}$			XX$_{16}$
02CE$_{16}$	X7 register/Y7 register	X7R,Y7R	XX$_{16}$
02CF$_{16}$			XX$_{16}$
02D0$_{16}$	X8 register/Y8 register	X8R,Y8R	XX$_{16}$
02D1$_{16}$			XX$_{16}$
02D2$_{16}$	X9 register/Y9 register	X9R,Y9R	XX$_{16}$
02D3$_{16}$			XX$_{16}$
02D4$_{16}$	X10 register/Y10 register	X10R,Y10R	XX$_{16}$
02D5$_{16}$			XX$_{16}$
02D6$_{16}$	X11 register/Y11 register	X11R,Y11R	XX$_{16}$
02D7$_{16}$			XX$_{16}$
02D8$_{16}$	X12 register/Y12 register	X12R,Y12R	XX$_{16}$
02D9$_{16}$			XX$_{16}$
02DA$_{16}$	X13 register/Y13 register	X13R,Y13R	XX$_{16}$
02DB$_{16}$			XX$_{16}$
02DC$_{16}$	X14 register/Y14 register	X14R,Y14R	XX$_{16}$
02DD$_{16}$			XX$_{16}$
02DE$_{16}$	X15 register/Y15 register	X15R,Y15R	XX$_{16}$
02DF$_{16}$			XX$_{16}$

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.15. SFR table(15)

Address	Register	Symbol	Value after RESET
02E0$_{16}$	XY control register	XYC	XXXX XX00$_2$
02E1$_{16}$			
02E2$_{16}$			
02E3$_{16}$			
02E4$_{16}$	UART1 special mode register 4	U1SMR4	0000 0000$_2$
02E5$_{16}$	UART1 special mode register 3	U1SMR3	0000 0000$_2$
02E6$_{16}$	UART1 special mode register 2	U1SMR2	0000 0000$_2$
02E7$_{16}$	UART1 special mode register	U1SMR	0000 0000$_2$
02E8$_{16}$	UART1 transmit/receive mode register	U1MR	0000 0000$_2$
02E9$_{16}$	UART1 baud rate generator	U1BRG	XX$_{16}$
02EA$_{16}$ 02EB$_{16}$	UART1 transmit buffer register	U1TB	XX$_{16}$ XX$_{16}$
02EC$_{16}$	UART1 transmit/receive control register 0	U1C0	0000 1000$_2$
02ED$_{16}$	UART1 transmit/receive control register 1	U1C1	0000 0010$_2$
02EE$_{16}$ 02EF$_{16}$	UART1 receive buffer register	U1RB	XX$_{16}$ XX$_{16}$
02F0$_{16}$			
02F1$_{16}$			
02F2$_{16}$			
02F3$_{16}$			
02F4$_{16}$	UART4 special mode register 4	U4SMR4	0000 0000$_2$
02F5$_{16}$	UART4 special mode register 3	U4SMR3	0000 0000$_2$
02F6$_{16}$	UART4 special mode register 2	U4SMR2	0000 0000$_2$
02F7$_{16}$	UART4 special mode register	U4SMR	0000 0000$_2$
02F8$_{16}$	UART4 transmit/receive mode register	U4MR	0000 0000$_2$
02F9$_{16}$	UART4 baud rate generator	U4BRG	XX$_{16}$
02FA$_{16}$ 02FB$_{16}$	UART4 transmit buffer register	U4TB	XX$_{16}$ XX$_{16}$
02FC$_{16}$	UART4 transmit/receive control register 0	U4C0	0000 1000$_2$
02FD$_{16}$	UART4 transmit/receive control register 1	U4C1	0000 0010$_2$
02FE$_{16}$ 02FF$_{16}$	UART4 receive buffer register	U4RB	XX$_{16}$ XX$_{16}$
0300$_{16}$	Timer B3,B4,B5 count start flag	TBSR	000X XXXX$_2$
0301$_{16}$			
0302$_{16}$ 0303$_{16}$	Timer A1-1 register	TA11	XX$_{16}$ XX$_{16}$
0304$_{16}$ 0305$_{16}$	Timer A2-1 register	TA21	XX$_{16}$ XX$_{16}$
0306$_{16}$ 0307$_{16}$	Timer A4-1 register	TA41	XX$_{16}$ XX$_{16}$
0308$_{16}$	Three-phase PWM control register 0	INVC0	0000 0000$_2$
0309$_{16}$	Three-phase PWM control register 1	INVC1	0000 0000$_2$
030A$_{16}$	Three-phase output buffer register 0	IDB0	XX00 0000$_2$
030B$_{16}$	Three-phase output buffer register 1	IDB1	XX00 0000$_2$
030C$_{16}$	Dead time timer	DTT	XX$_{16}$
030D$_{16}$	Timer B2 interrupt generation frequency set counter	ICTB2	XX$_{16}$
030E$_{16}$			
030F$_{16}$			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.16. SFR table(16)

Address	Register	Symbol	Value after RESET
031016	Timer B3 register	TB3	XX16
031116			XX16
031216	Timer B4 register	TB4	XX16
031316			XX16
031416	Timer B5 register	TB5	XX16
031516			XX16
031616			
031716			
031816			
031916			
031A16			
031B16	Timer B3 mode register	TB3MR	00XX 00002
031C16	Timer B4 mode register	TB4MR	00XX 00002
031D16	Timer B5 mode register	TB5MR	00XX 00002
031E16			
031F16	External interrupt cause select register	IFSR	0000 00002
032016			
032116			
032216			
032316			
032416	UART3 special mode register 4	U3SMR4	0000 00002
032516	UART3 special mode register 3	U3SMR3	0000 00002
032616	UART3 special mode register 2	U3SMR2	0000 00002
032716	UART3 special mode register	U3SMR	0000 00002
032816	UART3 transmit/receive mode register	U3MR	0000 00002
032916	UART3 baud rate generator	U3BRG	XX16
032A16	UART3 transmit buffer register	U3TB	XX16
032B16			XX16
032C16	UART3 transmit/receive control register 0	U3C0	0000 10002
032D16	UART3 transmit/receive control register 1	U3C1	0000 00102
032E16	UART3 receive buffer register	U3RB	XX16
032F16			XX16
033016			
033116			
033216			
033316			
033416	UART2 special mode register 4	U2SMR4	0000 00002
033516	UART2 special mode register 3	U2SMR3	0000 00002
033616	UART2 special mode register 2	U2SMR2	0000 00002
033716	UART2 special mode register	U2SMR	0000 00002
033816	UART2 transmit/receive mode register	U2MR	0000 00002
033916	UART2 baud rate generator	U2BRG	XX16
033A16	UART2 transmit buffer register	U2TB	XX16
033B16			XX16
033C16	UART2 transmit/receive control register 0	U2C0	0000 10002
033D16	UART2 transmit/receive control register 1	U2C1	0000 00102
033E16	UART2 receive buffer register	U2RB	XX16
033F16			XX16

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.17. SFR table(17)

Address	Register	Symbol	Value after RESET
0340₁₆	Count start flag	TABSR	0000 0000₂
0341₁₆	Clock prescaler reset flag	CPSRF	0XXX XXXX₂
0342₁₆	One-shot start flag	ONSF	0000 0000₂
0343₁₆	Trigger select register	TRGSR	0000 0000₂
0344₁₆	Up-down flag	UDF	0000 0000₂
0345₁₆			
0346₁₆ 0347₁₆	Timer A0 register	TA0	XX₁₆ XX₁₆
0348₁₆ 0349₁₆	Timer A1 register	TA1	XX₁₆ XX₁₆
034A₁₆ 034B₁₆	Timer A2 register	TA2	XX₁₆ XX₁₆
034C₁₆ 034D₁₆	Timer A3 register	TA3	XX₁₆ XX₁₆
034E₁₆ 034F₁₆	Timer A4 register	TA4	XX₁₆ XX₁₆
0350₁₆ 0351₁₆	Timer B0 register	TB0	XX₁₆ XX₁₆
0352₁₆ 0353₁₆	Timer B1 register	TB1	XX₁₆ XX₁₆
0354₁₆ 0355₁₆	Timer B2 register	TB2	XX₁₆ XX₁₆
0356₁₆	Timer A0 mode register	TA0MR	0000 0X00₂
0357₁₆	Timer A1 mode register	TA1MR	0000 0X00₂
0358₁₆	Timer A2 mode register	TA2MR	0000 0X00₂
0359₁₆	Timer A3 mode register	TA3MR	0000 0X00₂
035A₁₆	Timer A4 mode register	TA4MR	0000 0X00₂
035B₁₆	Timer B0 mode register	TB0MR	00XX 0000₂
035C₁₆	Timer B1 mode register	TB1MR	00XX 0000₂
035D₁₆	Timer B2 mode register	TB2MR	00XX 0000₂
035E₁₆	Timer B2 special mode register	TB2SC	XXXX XXX0₂
035F₁₆	Count source prescaler register	TCSPR	0XXX 0000₂
0360₁₆			
0361₁₆			
0362₁₆			
0363₁₆			
0364₁₆	UART0 special mode register 4	U0SMR4	0000 0000₂
0365₁₆	UART0 special mode register 3	U0SMR3	0000 0000₂
0366₁₆	UART0 special mode register 2	U0SMR2	0000 0000₂
0367₁₆	UART0 special mode register	U0SMR	0000 0000₂
0368₁₆	UART0 transmit/receive mode register	U0MR	0000 0000₂
0369₁₆	UART0 baud rate generator	U0BRG	XX₁₆
036A₁₆ 036B₁₆	UART0 transmit buffer register	U0TB	XX₁₆ XX₁₆
036C₁₆	UART0 transmit/receive control register 0	U0C0	0000 1000₂
036D₁₆	UART0 transmit/receive control register 1	U0C1	0000 0010₂
036E₁₆ 036F₁₆	UART0 receive buffer register	U0RB	XX₁₆ XX₁₆

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
X : Nothing is mapped to this bit.

Table 4.18. SFR table(18)

Address	Register	Symbol	Value after RESET
037016			
037116			
037216			
037316			
037416			
037516			
037616			
037716			
037816	DMA0 cause select register	DM0SL	0X00 00002
037916	DMA1 cause select register	DM1SL	0X00 00002
037A16	DMA2 cause select register	DM2SL	0X00 00002
037B16	DMA3 cause select register	DM3SL	0X00 00002
037C16 037D16	CRC data register	CRCD	XX16 XX16
037E16	CRC input register	CRCIN	XX16
037F16			
038016 038116	A-D0 register 0	AD00	XX16 XX16
038216 038316	A-D0 register 1	AD01	XX16 XX16
038416 038516	A-D0 register 2	AD02	XX16 XX16
038616 038716	A-D0 register 3	AD03	XX16 XX16
038816 038916	A-D0 register 4	AD04	XX16 XX16
038A16 038B16	A-D0 register 5	AD05	XX16 XX16
038C16 038D16	A-D0 register 6	AD06	XX16 XX16
038E16 038F16	A-D0 register 7	AD07	XX16 XX16
039016			
039116			
039216	A-D0 control register 4	AD0CON4	XXXX 00XX2
039316			
039416	A-D0 control register 2	AD0CON2	XX0X XXX02
039516	A-D0 control register 3	AD0CON3	XXXX X0002
039616	A-D0 control register 0	AD0CON0	0000 00002
039716	A-D0 control register 1	AD0CON1	0000 00002
039816	D-A register 0	DA0	XX16
039916			
039A16	D-A register 1	DA1	XX16
039B16			
039C16	D-A control register	DACON	XXXX XX002
039D16			
039E16			
039F16			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.19. SFR table(19)

Address	Register	Symbol	Value after RESET
03A0$_{16}$			
03A1$_{16}$			
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function select register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$	Function select register C2	PSC2	XXXX X00X$_2$
03AD$_{16}$	Function select register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function select register C	PSC	00X0 0000$_2$
03B0$_{16}$	Function select register A0	PS0	0000 0000$_2$
03B1$_{16}$	Function select register A1	PS1	0000 0000$_2$
03B2$_{16}$	Function select register B0	PSL0	0000 0000$_2$
03B3$_{16}$	Function select register B1	PSL1	0000 0000$_2$
03B4$_{16}$	Function select register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function select register A3	PS3	0000 0000$_2$
03B6$_{16}$	Function select register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function select register B3	PSL3	0000 0000$_2$
03B8$_{16}$			
03B9$_{16}$			
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 register	P6	XX$_{16}$
03C1$_{16}$	Port P7 register	P7	XX$_{16}$
03C2$_{16}$	Port P6 direction register	PD6	0000 0000$_2$
03C3$_{16}$	Port P7 direction register	PD7	0000 0000$_2$
03C4$_{16}$	Port P8 register	P8	XX$_{16}$
03C5$_{16}$	Port P9 register	P9	XX$_{16}$
03C6$_{16}$	Port P8 direction register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 direction register	PD9	0000 0000$_2$
03C8$_{16}$	Port P10 register	P10	XX$_{16}$
03C9$_{16}$			
03CA$_{16}$	Port P10 direction register	PD10	0000 0000$_2$
03CB$_{16}$			
03CC$_{16}$			
03CD$_{16}$			
03CE$_{16}$			
03CF$_{16}$			

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit.

Table 4.20. SFR table(20)

Address	Register	Symbol	Value after RESET
03D0₁₆			
03D1₁₆			
03D2₁₆			
03D3₁₆			
03D4₁₆			
03D5₁₆			
03D6₁₆			
03D7₁₆			
03D8₁₆			
03D9₁₆			
03DA₁₆	Pull-up control register 2	PUR2	0000 0000₂
03DB₁₆	Pull-up control register 3	PUR3	XXXX XX00₂
03DC₁₆			
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 register	P0	XX₁₆
03E1₁₆	Port P1 register	P1	XX₁₆
03E2₁₆	Port P0 direction register	PD0	0000 0000₂
03E3₁₆	Port P1 direction register	PD1	0000 0000₂
03E4₁₆	Port P2 register	P2	XX₁₆
03E5₁₆	Port P3 register	P3	XX₁₆
03E6₁₆	Port P2 direction register	PD2	0000 0000₂
03E7₁₆	Port P3 direction register	PD3	0000 0000₂
03E8₁₆	Port P4 register	P4	XX₁₆
03E9₁₆	Port P5 register	P5	XX₁₆
03EA₁₆	Port P4 direction register	PD4	0000 0000₂
03EB₁₆	Port P5 direction register	PD5	0000 0000₂
03EC₁₆			
03ED₁₆			
03EE₁₆			
03EF₁₆			
03F0₁₆	Pull-up control register 0	PUR0	0000 0000₂
03F1₁₆	Pull-up control register 1	PUR1	XXXX 0000₂
03F2₁₆			
03F3₁₆			
03F4₁₆			
03F5₁₆			
03F6₁₆			
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆			
03FD₁₆			
03FE₁₆			
03FF₁₆	Port control register	PCR	XXXX XXX0₂

NOTES:

1. The blank areas are reserved and cannot be accessed by users.

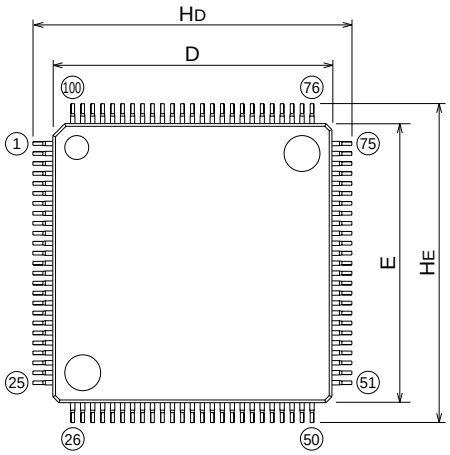
X : Nothing is mapped to this bit.

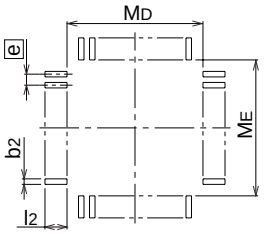
Package Dimensions

100P6Q-A (MMP)

Plastic 100pin 14X14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	–	0.63	Cu Alloy





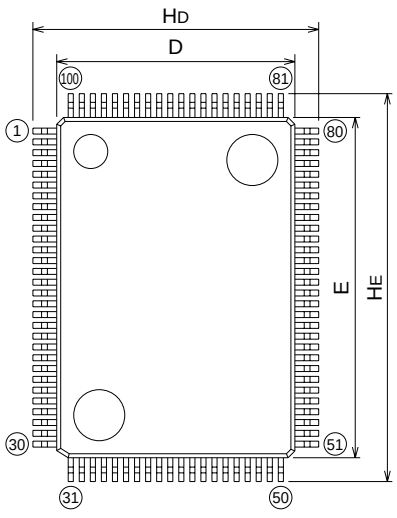
Recommended Mount Pad

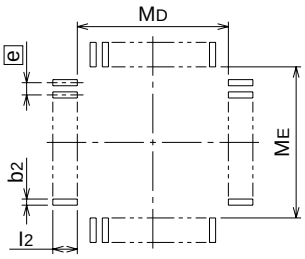
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.5	–
HD	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	14.4	–
ME	–	14.4	–

100P6S-A (MMP)

Plastic 100pin 14X20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	–	1.58	Alloy 42





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	–	1.4	–
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b2	–	0.35	–
l2	1.3	–	–
MD	–	14.6	–
ME	–	20.6	–

REVISION HISTORY	M32C/80 Group Short Sheet / Data Sheet

Rev.	Date	Description	
		Page	Summary
0.10	Sep. 13, 2002	–	First edition issued
0.11	Sep. 19, 2002	3	Table 1.1.1 “CAN” deleted.
0.12	Nov. 20, 2002	3	Table 1.1.1 “4.2 to 5.5V” --> “3.0 to 5.5V” "3.0 to 3.6V (f(XIN)=20MHz without software wait)." deleted. "26mA (f(XIN)=20MHz without software wait,Vcc=3.3V)" deleted.
0.30	Aug. 07, 2002	–	1. Overview changed. 1.2 Performance Outline changed. 1.3 Block Diagram added. 1.5 Pin Assignments changed. Table 1.3 Pin Characteristics for 100-Pin Package changed. 1.6 Pin Description added. 2. Central Processing Unit (CPU) added. 3. Memory added. 4. Special Function Registers (SFR) added.

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