REJ03B0046-0040Z
Rev.0.40
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1. Overview

The M32C/85 is a single-chip microcomputer that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/85 group is available in 144-pin and 100-pin plastic molded QFP/LQFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It incorporates a multiplier and DMAC adequate for office automation, communication devices and industrial equipments and other high-speed processing applications.

1.1 Applications

Audio, cameras, office equipment, communications equipment, portable equipment, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error.
Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Outline

Tables 1.1 and 1.2 list performance outlines of the M32C/85 group.

Table 1.1 M32C/85 Group Performance (144-Pin Package)

Item		Performance
CPU	Basic instructions	108 instructions
	Shortest instruction execution time	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V) 50 ns (f(BCLK)=20 MHz, VCC1=3.0 V to 5.5 V)
	Operation mode	Single-chip, memory expansion and microprocessor modes
	Memory space	16 Mbytes
	Memory capacity	See Table 1.3
Peripheral function	Port	123 I/O pins and 1 input pin
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function or waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)
	Serial I/O	5 channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I^2C bus(2)
	CAN module	2 channels Supporting CAN 2.0B specification
	A-D converter	10-bit A-D converter: 1 circuit, 34 channels
	D-A converter	8-bit x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt factors Immediate transfer, calculation transfer and chain transfer functions
	CRC calculation circuit	CRC-CCITT
	X-Y converter	16 bits X 16 bits
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	39 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock generating circuit	4 circuits Main clock oscillation circuit(*), sub clock oscillation circuit(*), ring oscillator, PLL frequency synthesizer (*)Oscillation circuits include an internal feedback resistor and external ceramic resonator/crystal oscillator.
	Oscillator stop detect function	Main clock oscillator stop detect function
	Supply voltage detect circuit	Available (option)
Electric charact-eristics	Supply voltage	V_{CC1}=4.2 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=32 MHz) V_{CC1}=3.0 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=20 MHz)
	Power consumption	38 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 26 mA (V_{CC1}=V_{CC2}=3.3 V, f(BCLK)=20 MHz) TBD (V_{CC1}=V_{CC2}=3.3 V, f(X_{CIN})=32 kHz, wait mode)
Flash memory	Program/erase supply voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V
	Program and erase endurance	100 times
Operating ambient temperature		–20 to 85°C, –40 to 85°C (option)
Package		144-pin plastic mold QFP

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.

All options are on a request basis.

Table 1.2 M32C/85 Group Performance (100-Pin Package)

Item		Performance
CPU	Basic instructions	108 instructions
	Shortest instruction execution time	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V) 50 ns (f(BCLK)=20 MHz, V_{CC1}=3.0 V to 5.5 V)
	Operation mode	Single-chip, memory expansion and microprocessor modes
	Memory space	16 Mbytes
	Memory capacity	See Table 1.3
Peripheral function	Port	87 I/O pins and 1 input pin
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function or waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)
	Serial I/O	5 channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I^2C bus(2)
	CAN module	2 channels Supporting CAN 2.0B specification
	A-D converter	10-bit A-D converter: 1 circuit, 26 channels
	D-A converter	8-bit x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt factors Immediate transfer, calculation transfer and chain transfer functions
	CRC calculation circuit	CRC-CCITT
	X-Y converter	16 bits X 16 bits
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	39 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock generating circuit	4 circuits Main clock oscillation circuit(*), sub clock oscillation circuit(*), ring oscillator, PLL frequency synthesizer (*)Oscillation circuits include an internal feedback resistor and external ceramic resonator/crystal oscillator.
	Oscillator stop detect function	Main clock oscillator stop detect function
	Supply voltage detect circuit	Available (option)
Electric charact-teristics	Supply voltage	V_{CC1}=4.2 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=32 MHz) V_{CC1}=3.0 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=20 MHz)
	Power consumption	38 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 26 mA (V_{CC1}=V_{CC2}=3.3 V, f(BCLK)=20 MHz) TBD (V_{CC1}=V_{CC2}=3.3 V, f(X_{CIN})=32 kHz, wait mode)
Flash memory	Program/erase supply voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V
	Program and erase endurance	100 times
Operating ambient temperature		–20 to 85°C, –40 to 85°C (option)
Package		100-pin plastic mold QFP

NOTES:
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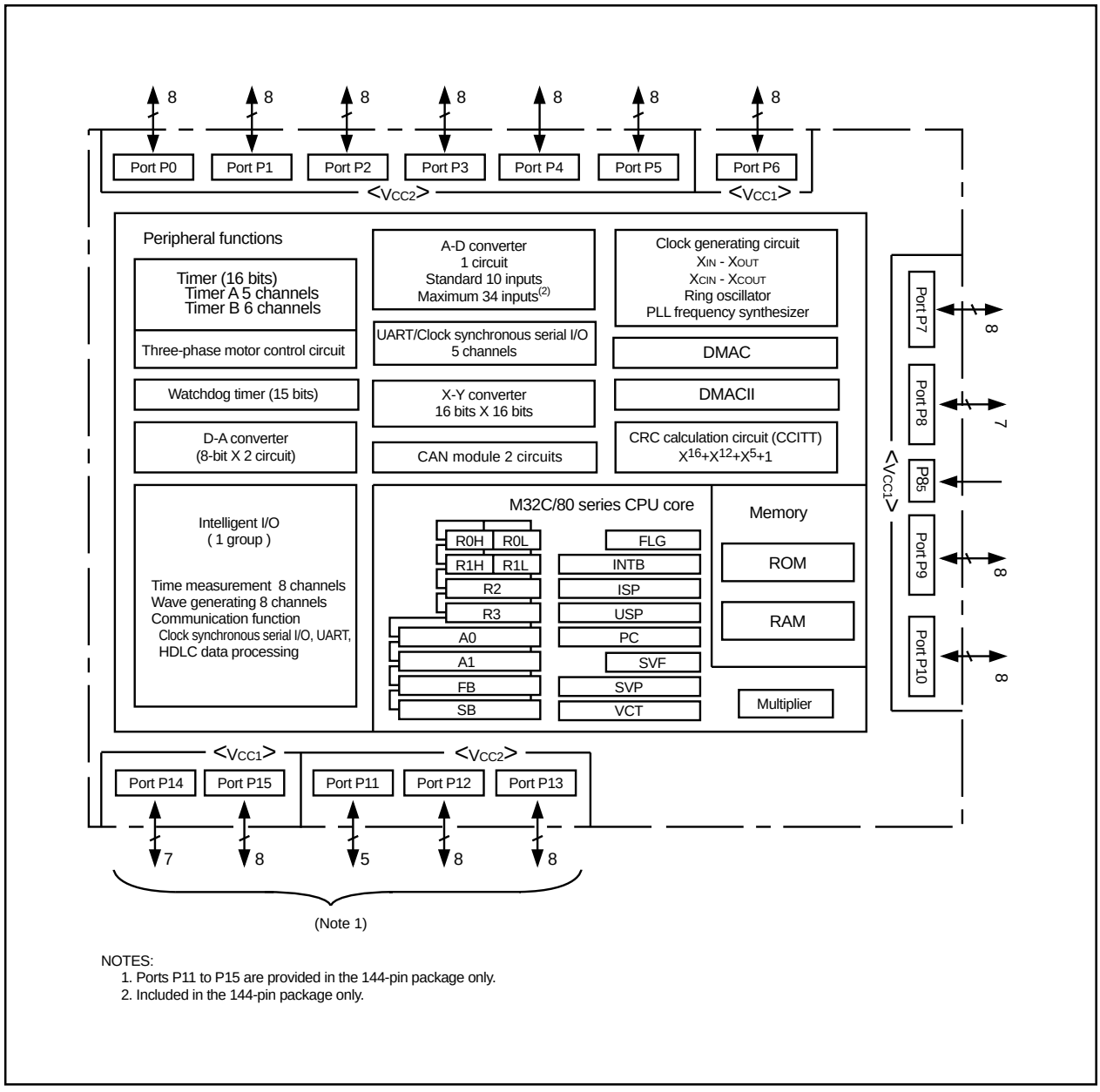
2. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/85 group microcomputer.

The M32C/85 group microcomputer contains ROM and RAM as memory to store instructions and data, CPU to execute calculations and peripheral functions such as interrupt, timer, serial I/O, DMAC, CRC calculation circuit, A-D converter, D-A converter, intelligent I/O and ports.



NOTES:
1. Ports P11 to P15 are provided in the 144-pin package only.
2. Included in the 144-pin package only.

Figure 1.1 M32C/85 Group Block Diagram

1.4 Product Information

Renesas plans to release the following products in the M32C/85 group:

(1) Support for the flash memory version and masked ROM version

(2) ROM/RAM capacity

(3) Package

100P6S-A : Plastic molded QFP

100P6Q-A : Plastic molded QFP

144P6Q-A : Plastic molded QFP

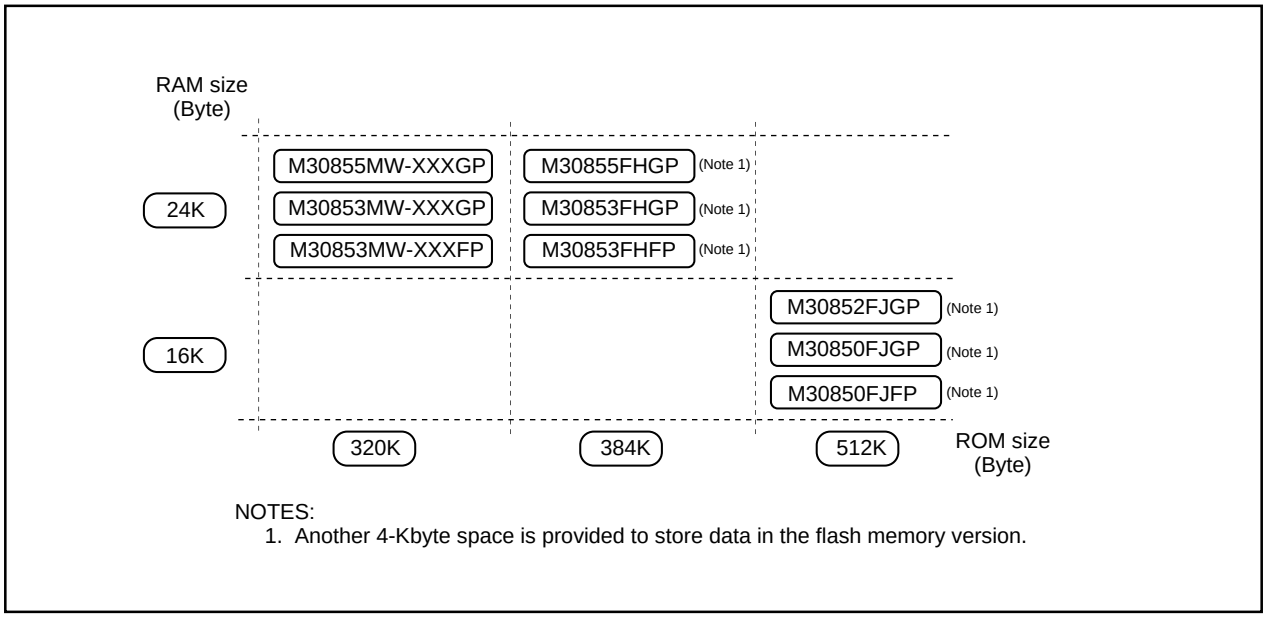


Figure 1.2 ROM/RAM Capacity

Table 1.3 M32C/85 Group **As of September, 2003**

Type number		ROM capacity	RAM capacity	Package type	Remarks
M30852FJGP	(D)	512K(1)	16K	144P6Q-A	Flash memory
M30850FJGP	(D)			100P6Q-A	
M30850FJFP	(D)			100P6S-A	
M30855FHGP	(D)	384K(1)	24K	144P6Q-A	
M30853FHGP	(D)			100P6Q-A	
M30853FHFP	(D)			100P6S-A	
M30855MW-XXXGP	(D)	320K	24K	144P6Q-A	Masked ROM
M30853MW-XXXGP	(D)			100P6Q-A	
M30853MW-XXXFP	(D)			100P6S-A	

(D): Under development

NOTES:

1. Another 4-Kbyte space is provided to store data in the flash memory version.

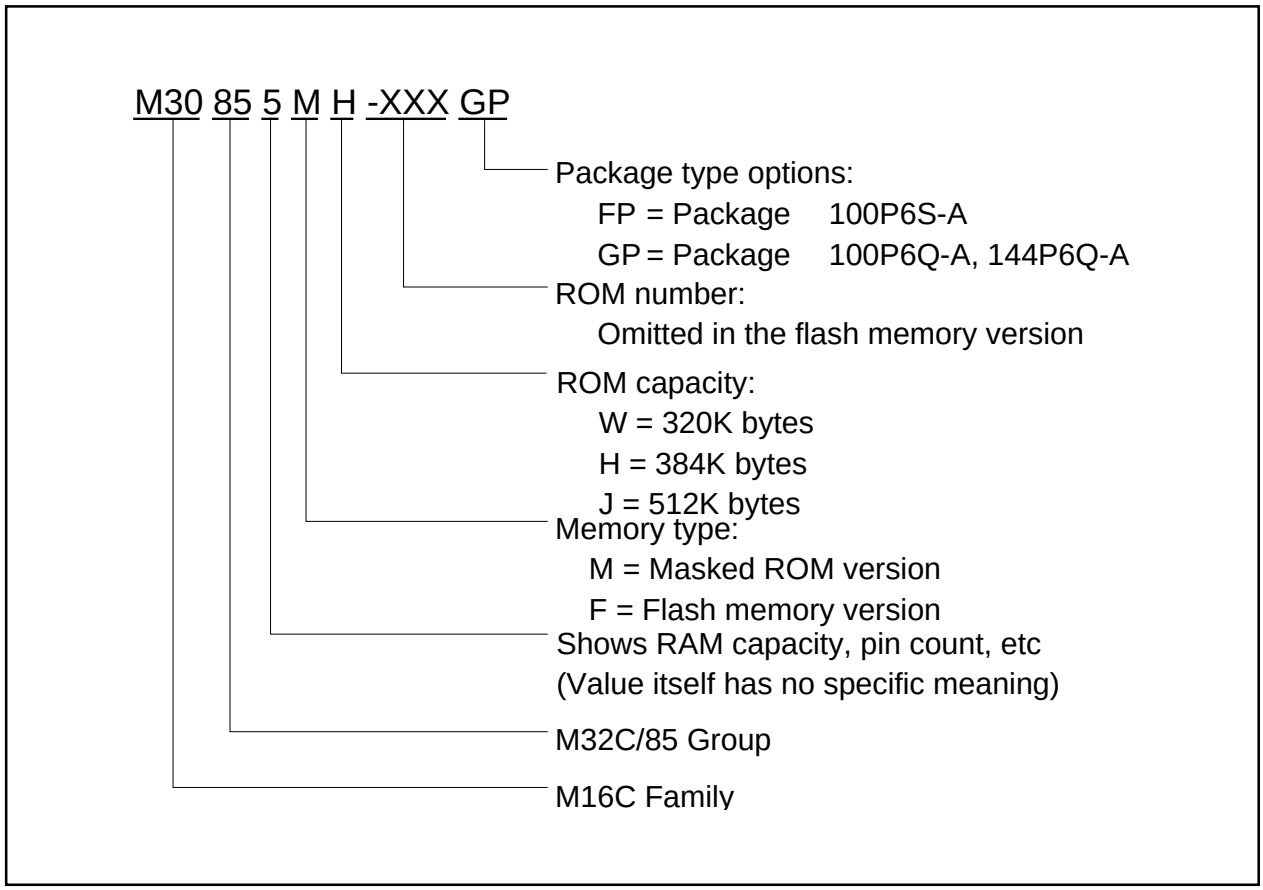


Figure 1.3 Product Numbering System

1.5 Pin Assignments and Descriptions

Figures 1.4 to 1.6 show pin assignments (top view).

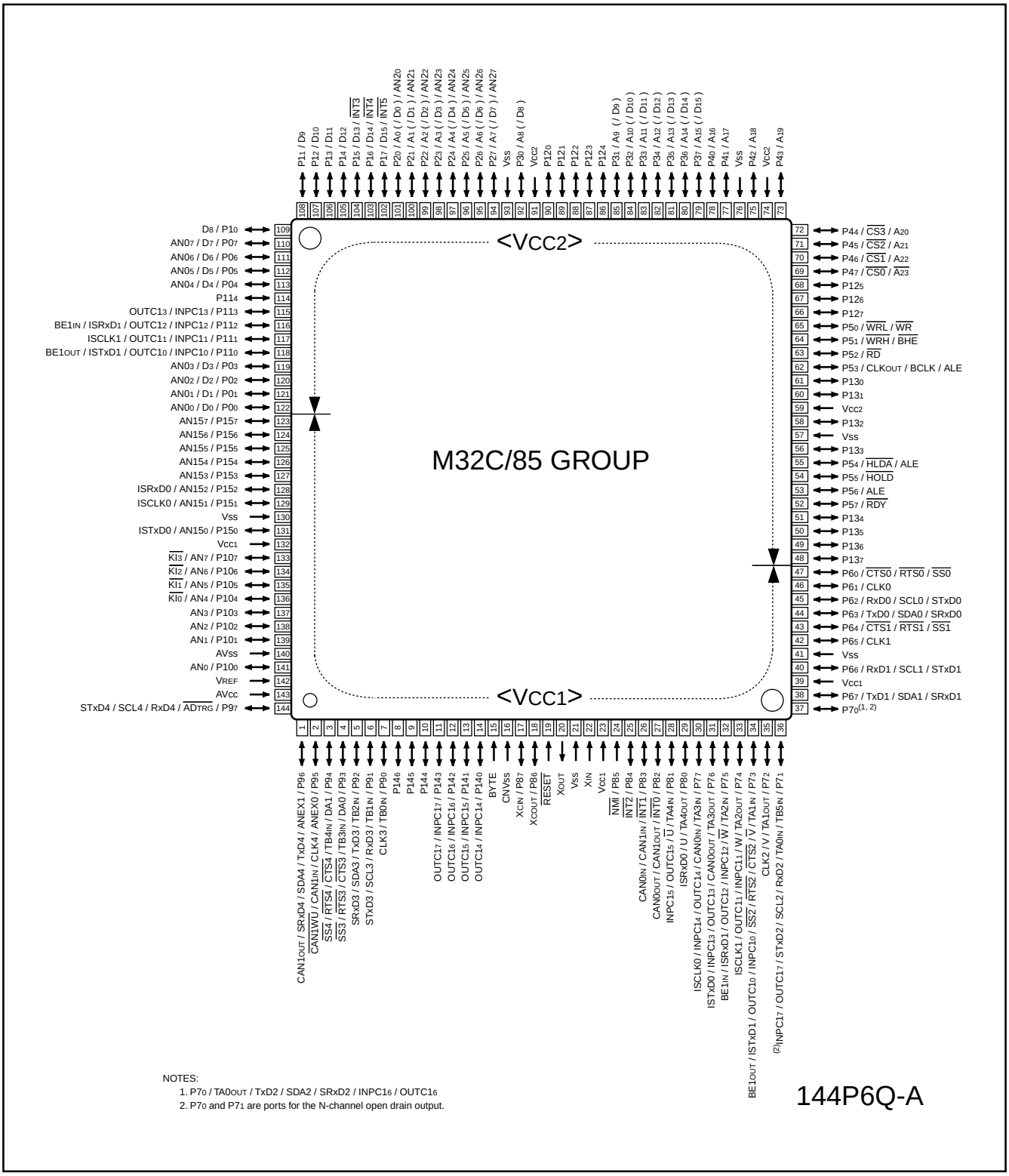


Figure 1.4 Pin Assignment for 144-Pin Package

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
1		P9$_6$			TxD4/SDA4/SRxD4/CAN1$_{OUT}$		ANEX1	
2		P9$_5$			CLK4/CAN1$_{IN}$/$\overline{CAN1WU}$		ANEX0	
3		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1	
4		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0	
5		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3			
6		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3			
7		P9$_0$		TB0$_{IN}$	CLK3			
8		P14$_6$						
9		P14$_5$						
10		P14$_4$						
11		P14$_3$				INPC1$_7$/OUTC1$_7$		
12		P14$_2$				INPC1$_6$/OUTC1$_6$		
13		P14$_1$				INPC1$_5$/OUTC1$_5$		
14		P14$_0$				INPC1$_4$/OUTC1$_4$		
15	BYTE							
16	CNV$_{SS}$							
17	X$_{CIN}$	P8$_7$						
18	X$_{COUT}$	P8$_6$						
19	$\overline{RESET}$							
20	X$_{OUT}$							
21	V$_{SS}$							
22	X$_{IN}$							
23	V$_{CC1}$							
24		P8$_5$	$\overline{NMI}$					
25		P8$_4$	$\overline{INT2}$					
26		P8$_3$	$\overline{INT1}$		CAN0$_{IN}$/CAN1$_{IN}$			
27		P8$_2$	$\overline{INT0}$		CAN0$_{OUT}$/CAN1$_{OUT}$			
28		P8$_1$		TA4$_{IN}$/$\overline{U}$		INPC1$_5$/OUTC1$_5$		
29		P8$_0$		TA4$_{OUT}$/U		ISRxD0		
30		P7$_7$		TA3$_{IN}$	CAN0$_{IN}$	INPC1$_4$/OUTC1$_4$/ISCLK0		
31		P7$_6$		TA3$_{OUT}$	CAN0$_{OUT}$	INPC1$_3$/OUTC1$_3$/ISTxD0		
32		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$		
33		P7$_4$		TA2$_{OUT}$/W		INPC1$_1$/OUTC1$_1$/ISCLK1		
34		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	INPC1$_0$/OUTC1$_0$/ISTxD1/BE1$_{OUT}$		
35		P7$_2$		TA1$_{OUT}$/V	CLK2			
36		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	INPC1$_7$/OUTC1$_7$		
37		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	INPC1$_6$/OUTC1$_6$		
38		P6$_7$			TxD1/SDA1/SRxD1			
39	V$_{CC1}$							
40		P6$_6$			RxD1/SCL1/STxD1			
41	V$_{SS}$							
42		P6$_5$			CLK1			
43		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$			
44		P6$_3$			TxD0/SDA0/SRxD0			
45		P6$_2$			RxD0/SCL0/STxD0			
46		P6$_1$			CLK0			
47		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
48		P13$_7$						

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
49		$P13_6$						
50		$P13_5$						
51		$P13_4$						
52		$P5_7$						$\overline{RDY}$
53		$P5_6$						ALE
54		$P5_5$						$\overline{HOLD}$
55		$P5_4$						$\overline{HLDA}$/ALE
56		$P13_3$						
57	V_{SS}							
58		$P13_2$						
59	V_{CC2}							
60		$P13_1$						
61		$P13_0$						
62		$P5_3$						CLK_{OUT}/BCLK/ALE
63		$P5_2$						$\overline{RD}$
64		$P5_1$						$\overline{WRH}$/$\overline{BHE}$
65		$P5_0$						$\overline{WRL}$/$\overline{WR}$
66		$P12_7$						
67		$P12_6$						
68		$P12_5$						
69		$P4_7$						$\overline{CS0}$/A_{23}
70		$P4_6$						$\overline{CS1}$/A_{22}
71		$P4_5$						$\overline{CS2}$/A_{21}
72		$P4_4$						$\overline{CS3}$/A_{20}
73		$P4_3$						A_{19}
74	V_{CC2}							
75		$P4_2$						A_{18}
76	V_{SS}							
77		$P4_1$						A_{17}
78		$P4_0$						A_{16}
79		$P3_7$						A_{15}(/D_{15})
80		$P3_6$						A_{14}(/D_{14})
81		$P3_5$						A_{13}(/D_{13})
82		$P3_4$						A_{12}(/D_{12})
83		$P3_3$						A_{11}(/D_{11})
84		$P3_2$						A_{10}(/D_{10})
85		$P3_1$						A_9(/D_9)
86		$P12_4$						
87		$P12_3$						
88		$P12_2$						
89		$P12_1$						
90		$P12_0$						
91	V_{CC2}							
92		$P3_0$						A_8(/D_8)
93	V_{SS}							
94		$P2_7$					$AN2_7$	A_7(/D_7)
95		$P2_6$					$AN2_6$	A_6(/D_6)
96		$P2_5$					$AN2_5$	A_5(/D_5)

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
97		$P2_4$					$AN2_4$	A_4(/D_4)
98		$P2_3$					$AN2_3$	A_3(/D_3)
99		$P2_2$					$AN2_2$	A_2(/D_2)
100		$P2_1$					$AN2_1$	A_1(/D_1)
101		$P2_0$					$AN2_0$	A_0(/D_0)
102		$P1_7$	$\overline{INT5}$					D_{15}
103		$P1_6$	$\overline{INT4}$					D_{14}
104		$P1_5$	$\overline{INT3}$					D_{13}
105		$P1_4$						D_{12}
106		$P1_3$						D_{11}
107		$P1_2$						D_{10}
108		$P1_1$						D_9
109		$P1_0$						D_8
110		$P0_7$					$AN0_7$	D_7
111		$P0_6$					$AN0_6$	D_6
112		$P0_5$					$AN0_5$	D_5
113		$P0_4$					$AN0_4$	D_4
114		$P11_4$						
115		$P11_3$				INPC1_3/OUTC1_3		
116		$P11_2$				INPC1_2/OUTC1_2/ISRxD1/BE1$_{IN}$		
117		$P11_1$				INPC1_1/OUTC1_1/ISCLK1		
118		$P11_0$				INPC1_0/OUTC1_0/ISTxD1/BE1$_{OUT}$		
119		$P0_3$					$AN0_3$	D_3
120		$P0_2$					$AN0_2$	D_2
121		$P0_1$					$AN0_1$	D_1
122		$P0_0$					$AN0_0$	D_0
123		$P15_7$					$AN15_7$	
124		$P15_6$					$AN15_6$	
125		$P15_5$					$AN15_5$	
126		$P15_4$					$AN15_4$	
127		$P15_3$					$AN15_3$	
128		$P15_2$				ISRxD0	$AN15_2$	
129		$P15_1$				ISCLK0	$AN15_1$	
130	V_{SS}							
131		$P15_0$				ISTxD0	$AN15_0$	
132	V_{CC1}							
133		$P10_7$	$\overline{KI_3}$				AN_7	
134		$P10_6$	$\overline{KI_2}$				AN_6	
135		$P10_5$	$\overline{KI_1}$				AN_5	
136		$P10_4$	$\overline{KI_0}$				AN_4	
137		$P10_3$					AN_3	
138		$P10_2$					AN_2	
139		$P10_1$					AN_1	
140	AV_{SS}							
141		$P10_0$					AN_0	
142	V_{REF}							
143	AV_{CC}							
144		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

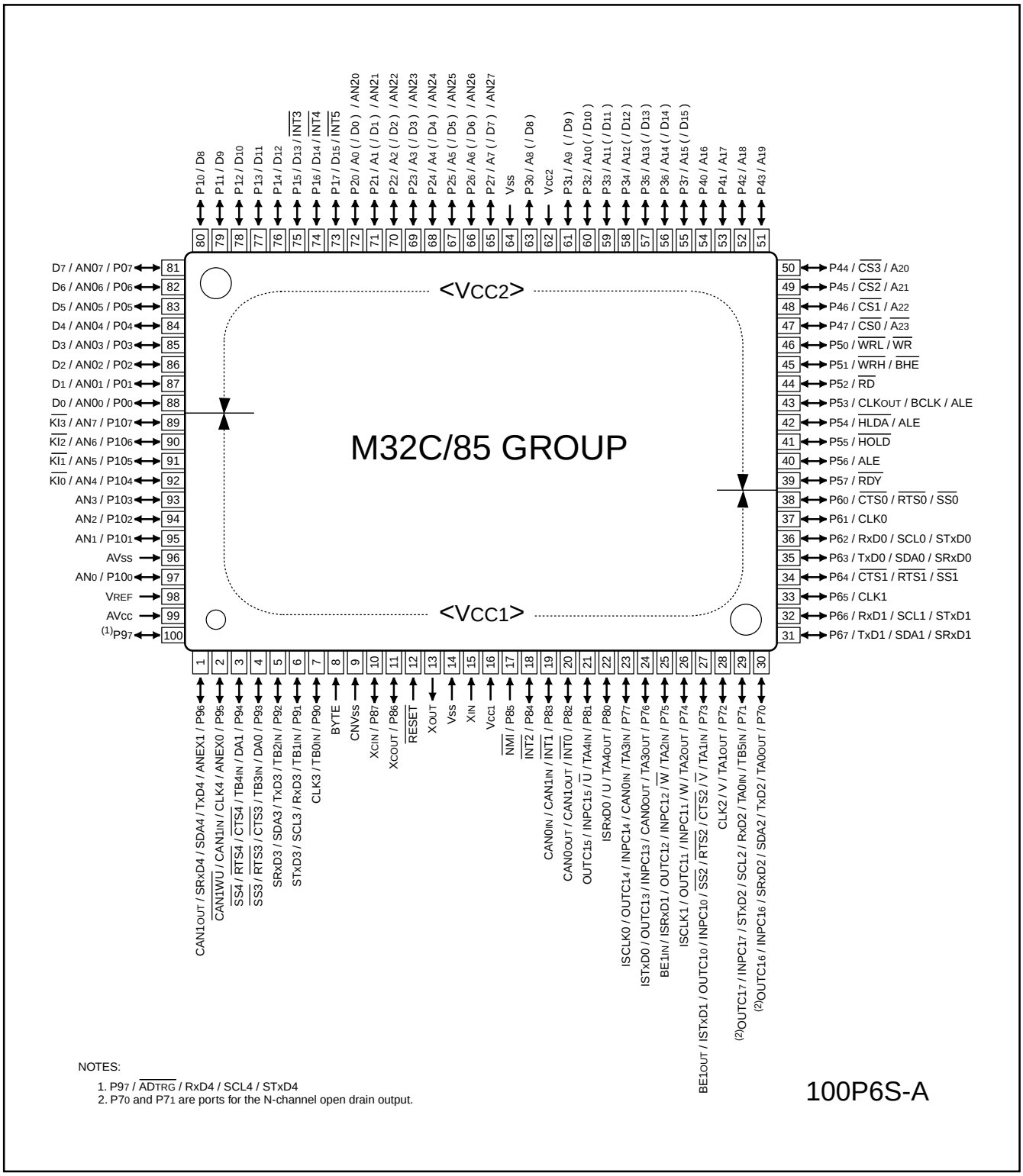
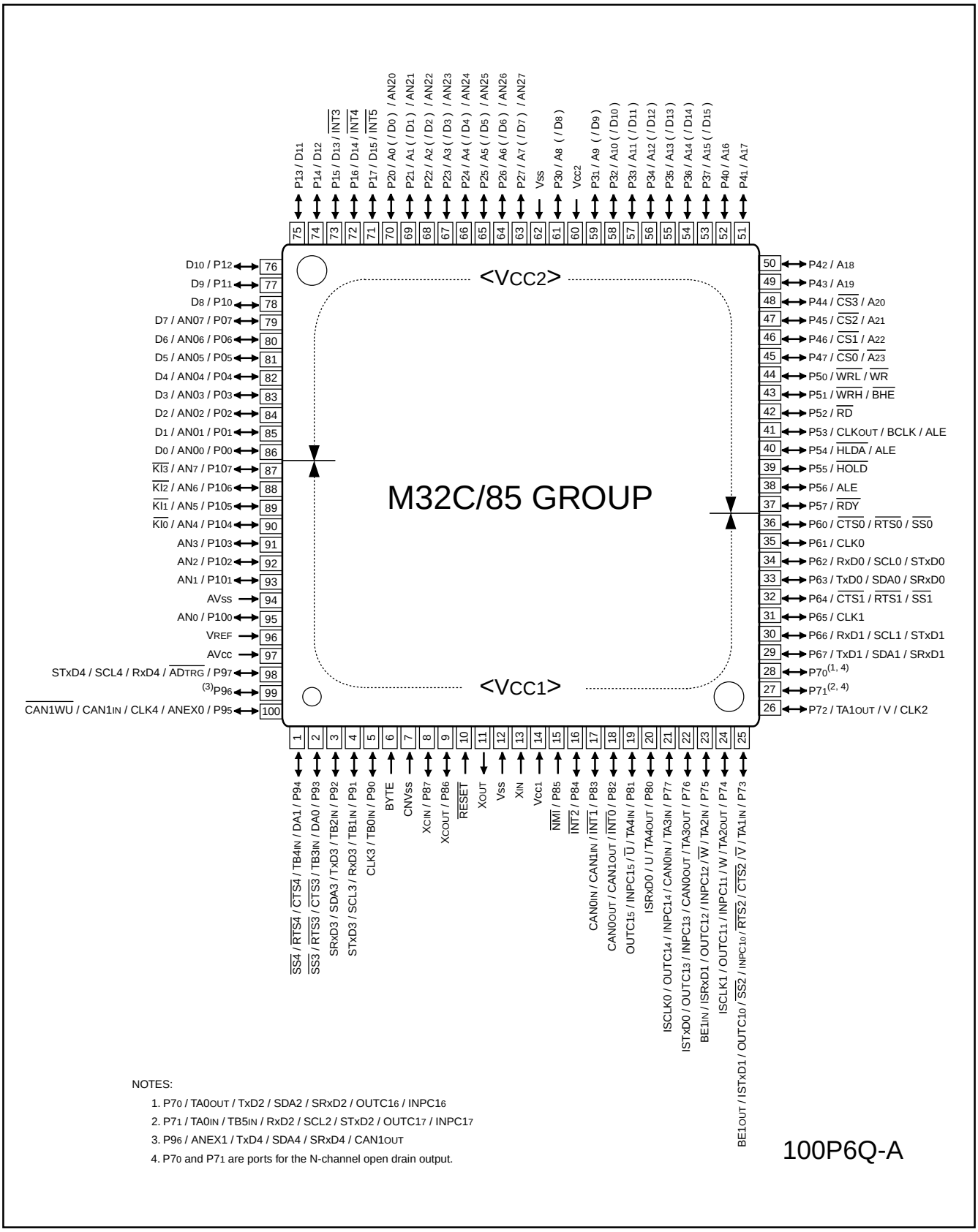


Figure 1.5 Pin assignment for 100-Pin Package



NOTES:
1. P70 / TA0OUT / TxD2 / SDA2 / SRxD2 / OUTC16 / INPC16
2. P71 / TA0IN / TB5IN / RxD2 / SCL2 / STxD2 / OUTC17 / INPC17
3. P96 / ANEX1 / TxD4 / SDA4 / SRxD4 / CAN1OUT
4. P70 and P71 are ports for the N-channel open drain output.

Figure 1.6 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No		Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
FP	GP								
1	99		P9$_6$			TxD4/SDA4/SRxD4/CAN1$_{OUT}$		ANEX1	
2	100		P9$_5$			CLK4/CAN1IN/$\overline{CAN1WU}$		ANEX0	
3	1		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1	
4	2		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0	
5	3		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3			
6	4		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3			
7	5		P9$_0$		TB0$_{IN}$	CLK3			
8	6	BYTE							
9	7	CNV$_{SS}$							
10	8	X$_{CIN}$	P8$_7$						
11	9	X$_{COUT}$	P8$_6$						
12	10	$\overline{RESET}$							
13	11	X$_{OUT}$							
14	12	V$_{SS}$							
15	13	X$_{IN}$							
16	14	V$_{CC1}$							
17	15		P8$_5$	$\overline{NMI}$					
18	16		P8$_4$	$\overline{INT2}$					
19	17		P8$_3$	$\overline{INT1}$		CAN0$_{IN}$/CAN1$_{IN}$			
20	18		P8$_2$	$\overline{INT0}$		CAN0$_{OUT}$/CAN1$_{OUT}$			
21	19		P8$_1$		TA4$_{IN}$/$\overline{U}$		INPC1$_5$/OUTC1$_5$		
22	20		P8$_0$		TA4$_{OUT}$/U		ISRxD0		
23	21		P7$_7$		TA3$_{IN}$	CAN0$_{IN}$	INPC1$_4$/OUTC1$_4$/ISCLK0		
24	22		P7$_6$		TA3$_{OUT}$	CAN0$_{OUT}$	INPC1$_3$/OUTC1$_3$/ISTxD0		
25	23		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$		
26	24		P7$_4$		TA2$_{OUT}$/W		INPC1$_1$/OUTC1$_1$/ISCLK1		
27	25		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	INPC1$_0$/OUTC1$_0$/ISTxD1/BE1$_{OUT}$		
28	26		P7$_2$		TA1$_{OUT}$/V	CLK2			
29	27		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	INPC1$_7$/OUTC1$_7$		
30	28		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	INPC1$_6$/OUTC1$_6$		
31	29		P6$_7$			TxD1/SDA1/SRxD1			
32	30		P6$_6$			RxD1/SCL1/STxD1			
33	31		P6$_5$			CLK1			
34	32		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$			
35	33		P6$_3$			TxD0/SDA0/SRxD0			
36	34		P6$_2$			RxD0/SCL0/STxD0			
37	35		P6$_1$			CLK0			
38	36		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
39	37		P5$_7$						$\overline{RDY}$
40	38		P5$_6$						ALE
41	39		P5$_5$						$\overline{HOLD}$
42	40		P5$_4$						$\overline{HLDA}$/ALE
43	41		P5$_3$						CLK$_{OUT}$/BCLK/ALE
44	42		P5$_2$						$\overline{RD}$
45	43		P5$_1$						$\overline{WRH}$/$\overline{BHE}$
46	44		P5$_0$						$\overline{WRL}$/$\overline{WR}$
47	45		P4$_7$						$\overline{CS0}$/A$_{23}$
48	46		P4$_6$						$\overline{CS1}$/A$_{22}$
49	47		P4$_5$						$\overline{CS2}$/A$_{21}$
50	48		P4$_4$						$\overline{CS3}$/A$_{20}$

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package pin No		Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
FP	GP								
51	49		$P4_3$						A_{19}
52	50		$P4_2$						A_{18}
53	51		$P4_1$						A_{17}
54	52		$P4_0$						A_{16}
55	53		$P3_7$						A_{15}(/D_{15})
56	54		$P3_6$						A_{14}(/D_{14})
57	55		$P3_5$						A_{13}(/D_{13})
58	56		$P3_4$						A_{12}(/D_{12})
59	57		$P3_3$						A_{11}(/D_{11})
60	58		$P3_2$						A_{10}(/D_{10})
61	59		$P3_1$						A_9(/D_9)
62	60	V_{CC2}							
63	61		$P3_0$						A_8(/D_8)
64	62	V_{SS}							
65	63		$P2_7$					$AN2_7$	A_7(/D_7)
66	64		$P2_6$					$AN2_6$	A_6(/D_6)
67	65		$P2_5$					$AN2_5$	A_5(/D_5)
68	66		$P2_4$					$AN2_4$	A_4(/D_4)
69	67		$P2_3$					$AN2_3$	A_3(/D_3)
70	68		$P2_2$					$AN2_2$	A_2(/D_2)
71	69		$P2_1$					$AN2_1$	A_1(/D_1)
72	70		$P2_0$					$AN2_0$	A_0(/D_0)
73	71		$P1_7$	$\overline{INT5}$					D_{15}
74	72		$P1_6$	$\overline{INT4}$					D_{14}
75	73		$P1_5$	$\overline{INT3}$					D_{13}
76	74		$P1_4$						D_{12}
77	75		$P1_3$						D_{11}
78	76		$P1_2$						D_{10}
79	77		$P1_1$						D_9
80	78		$P1_0$						D_8
81	79		$P0_7$					$AN0_7$	D_7
82	80		$P0_6$					$AN0_6$	D_6
83	81		$P0_5$					$AN0_5$	D_5
84	82		$P0_4$					$AN0_4$	D_4
85	83		$P0_3$					$AN0_3$	D_3
86	84		$P0_2$					$AN0_2$	D_2
87	85		$P0_1$					$AN0_1$	D_1
88	86		$P0_0$					$AN0_0$	D_0
89	87		$P10_7$	$\overline{KI_3}$				AN_7	
90	88		$P10_6$	$\overline{KI_2}$				AN_6	
91	89		$P10_5$	$\overline{KI_1}$				AN_5	
92	90		$P10_4$	$\overline{KI_0}$				AN_4	
93	91		$P10_3$					AN_3	
94	92		$P10_2$					AN_2	
95	93		$P10_1$					AN_1	
96	94	AV_{SS}							
97	95		$P10_0$					AN_0	
98	96	V_{REF}							
99	97	AV_{CC}							
100	98		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

1.6 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Symbol	Function	I/O type	Supply voltage	Description
V_{CC1}, V_{CC2} V_{SS}	Power supply input	I I	–	Apply 3.0 to 5.5V to both V_{CC1} and V_{CC2} pins. Apply 0V to the V_{SS} pin. $V_{CC1} \geq V_{CC2}$(1)
CNVSS	CNVSS	I	V_{CC1}	Switches processor mode. Connect this pin to V_{SS} to start up in single-chip mode (memory expansion mode). Connect this pin to V_{CC} to start up in microprocessor mode.
$\overline{RESET}$	Reset input	I	V_{CC1}	The microcomputer is in a reset state when applying "L" to the $\overline{RESET}$ pin.
X_{IN} X_{OUT}	Clock input Clock output	I O	V_{CC1}	I/O pins for the main clock generating circuit. Connect a ceramic resonator or crystal oscillator between X_{IN} and X_{OUT}. To use an external clock, input the clock to X_{IN} and leave X_{OUT} open.
BYTE	Input to switch external data bus width	I	V_{CC1}	Switches the data bus in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when the BYTE pin is held "H". Set to either. Connect this pin to V_{SS} when an external bus is not used.
AVCC	Analog power supply input	I	–	Applies power supply for the A-D converter and D-A converter. Connect this pin to V_{CC1}.
AVSS	Analog power supply input	I	–	Applies power supply for the A-D converter and D-A converter. Connect this pin to V_{SS}.
V_{REF}	Reference voltage input	I	–	Applies reference voltage for the A-D converter.
P00 to P07	I/O port P0	I/O	V_{CC2}	8-bit I/O ports in CMOS having a direction register to select input or output. Each pin is set as an input port or output port. An input port in single-chip mode can be set for a pull-up or for no pull-up in 4-bit unit by program. When these pins are used as bus control pins in memory expansion mode and microprocessor mode, internal pull-up resistor cannot be selected. Ports used as input ports can be set for a pull-up or for no pull-up in the modes above.
D0 to D7	Data bus	I/O		Inputs and outputs data (D0 to D7) when these pins are set as the separate bus.
AN00 to AN07	Analog input pin	I		Analog input pins for the A-D converter
P10 to P17	I/O port P1	I/O	V_{CC2}	8-bit I/O ports having equivalent functions to P0
$\overline{INT3}$ to $\overline{INT5}$	$\overline{INT}$ interrupt input pin	I		Input pins for the $\overline{INT}$ interrupt
D8 to D15	Data bus	I/O		Inputs and outputs data (D8 to D15) when these pins are set as the separate bus.
P20 to P27	I/O port P2	I/O	V_{CC2}	8-bit I/O ports having equivalent functions to P0
A0 to A7	Address bus	O		Outputs 8 low-order address bits (A0 to A7).
A0/D0 to A7/D7	Address bus/data bus	I/O		Inputs and outputs data (D0 to D7) and outputs 8 low-order address bits (A0 to A7) by time-sharing when these pins are set as the multiplexed bus.
AN20 to AN27	Analog input pin	I		Analog input pins for A-D converter
P30 to P37	I/O port P3	I/O	V_{CC2}	8-bit I/O ports having equivalent functions to P0
A8 to A15	Address bus	O		Outputs 8 middle-order address bits (A8 to A15).
A8/D8 to A15/D15	Address bus/data bus	I/O		Inputs and outputs data (D8 to D15) and outputs 8 middle-order address bits (A8 to A15) by time-sharing when external 16-bit data bus is set as the multiplexed bus.
P40 to P47	I/O port P4	I/O	V_{CC2}	8-bit I/O ports having equivalent functions to P0
A16 to A22, $\overline{A23}$	Address bus	O		Outputs 8 high-order address bits (A16 to A22, $\overline{A23}$). The highest-order bit ($\overline{A23}$) inversed is also output.
$\overline{CS0}$ to $\overline{CS3}$	Chip-select	O		Output $\overline{CS0}$ to $\overline{CS3}$ signals. $\overline{CS0}$ to $\overline{CS3}$ are chip-select signals specifying an external space.

I : Input O : Output I/O : Input and output

NOTES:

1. In this manual, hereafter, V_{CC} refers to V_{CC1} unless otherwise noted.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Supply voltage	Description
P5$_0$ to P5$_7$	I/O port P5	I/O	V_{CC2}	8-bit I/O ports having equivalent functions to P0
CLK$_{OUT}$	Clock output	O		Outputs the main clock divided by 8 or divided by 32 or the clock having the same frequency as the sub clock from P5$_3$.
$\overline{WRL}$	Bus control pin	O		Output $\overline{WRL}$, $\overline{WRH}$, ($\overline{WR}$, $\overline{BHE}$), $\overline{RD}$, BCLK, $\overline{HLDA}$ and ALE signals. $\overline{WRL}$ and $\overline{WRH}$ or $\overline{BHE}$ and $\overline{WR}$ can be switched by program. ■ $\overline{WRL}$, $\overline{WRH}$ and $\overline{RD}$ are selected The $\overline{WRL}$ signal becomes "L" by writing data to an even address in an external memory space. The $\overline{WRH}$ signal becomes "L" by writing data to an odd address in an external memory space. The $\overline{RD}$ pin signal becomes "L" by reading data in an external memory space. ■ $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ are selected The $\overline{WR}$ signal becomes "L" by writing data to an external memory space. The $\overline{RD}$ signal becomes "L" by reading data in an external memory space. The $\overline{BHE}$ signal becomes "L" by accessing an odd address. Select $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ for an external 8-bit data bus. While the $\overline{HOLD}$ pin is held "L", the microcomputer is placed in a hold state. In a hold state, $\overline{HLDA}$ outputs a "L" signal. ALE is a signal latching the address. While the $\overline{RDY}$ pin is held "L", the microcomputer is placed in a wait state.
$\overline{WR}$		O		
$\overline{WRH}$		O		
$\overline{BHE}$		O		
$\overline{RD}$		O		
BCLK		O		
$\overline{HLDA}$		O		
$\overline{HOLD}$		I		
ALE		O		
$\overline{RDY}$		I		
P6$_0$ to P6$_7$	I/O port P6	I/O	V_{CC1}	8-bit I/O ports having equivalent functions to P0
$\overline{CTS0}$, $\overline{CTS1}$	UART pin	I		I/O pins for UART0 (P6$_0$ to P6$_3$) and UART1 (P6$_4$ to P6$_7$)
$\overline{RTS0}$, $\overline{RTS1}$		O		
$\overline{SS0}$, $\overline{SS1}$		I		
CLK0, CLK1		I/O		
RxD0, RxD1		I		
SCL0, SCL1		I/O		
STxD0, STxD1		O		
TxD0, TxD1		O		
SDA0, SDA1		i/O		
SRxD0, SRxD1		I		

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Supply voltage	Description
$P7_0$ to $P7_7$	I/O port P7	I/O	V_{CC1}	8-bit I/O ports having equivalent functions to P0 ($P7_0$ and $P7_1$ are ports for the N-channel open drain output.)
$TA0_{OUT}$ to $TA3_{OUT}$	Timer A pin	I/O		I/O pins for timers A0 to A3
$TA0_{IN}$ to $TA3_{IN}$		I		
$TB5_{IN}$	Timer B pin	I		Input pin for timer B5
V, $\overline{V}$	Three-phase motor	O		V-phase output pin
W, $\overline{W}$	control output pin	O		W-phase output pin
$\overline{CTS2}$	UART pin	I		I/O pins for UART2
$\overline{RTS2}$		O		
$\overline{SS2}$		I		
CLK2		I/O		
RxD2		I		
SCL2		I/O		
STxD2		O		
TxD2		O		
SDA2		I/O		
SRxD2		I		
$INPC1_0$ to $INPC1_4$	Intelligent I/O pin	I		$INPC1_0$ to $INPC1_4$, $INPC1_6$ and $INPC1_7$ are input pins for the time measurement function.
$INPC1_6$, $INPC1_7$		I		
$OUTC1_0$ to $OUTC1_4$		O		$OUTC1_0$ to $OUTC1_4$, $OUTC1_6$ and $OUTC1_7$ are output pins for the waveform generating function.
$OUTC1_6$, $OUTC1_7$		O		
ISCLK0, ISCLK1		I/O		ISCLK0 and ISCLK1 input and output the clock for the intelligent I/O communication function.
ISTxD0, ISTxD1		O		
ISRxD1		I		ISRxD1 and $BE1_{IN}$ input received data for the intelligent I/O communication function.
$BE1_{OUT}$		O		ISTxD0, ISTxD1 and $BE1_{OUT}$ output transmit data for the intelligent I/O communication function.
$BE1_{IN}$		I		
$CAN0_{OUT}$	CAN pin	O		I/O pins for the CAN communication function
$\overline{CAN0_{IN}}$		I		
$P8_0$ to $P8_4$, $P8_6$, $P8_7$	I/O port P8	I/O	V_{CC1}	I/O ports having equivalent functions to P0
X_{CIN}	Sub clock	I		I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between X_{CIN} and X_{COUT}.
X_{COUT}		O		
$TA4_{OUT}$	Timer A pin	I/O		I/O pins for timer A4
$TA4_{IN}$		I		
U, $\overline{U}$	Three-phase motor control output pin	O		U-phase output pins
$\overline{INT0}$ to $\overline{INT2}$	$\overline{INT}$ interrupt input pin	I		Input pins for the $\overline{INT}$ interrupt
$INPC1_5$	Intelligent I/O pin	I		$INPC1_5$ is an input pin for the time measurement function.
$OUTC1_5$		O		$OUTC1_5$ is an output pin for the waveform generating function.
ISRxD0		I		ISRxD0 inputs received data for the intelligent I/O communication function.
$CAN0_{OUT}$, $CAN1_{OUT}$	CAN pin	O		I/O pins for the CAN communication function
$CAN0_{IN}$, $CAN1_{IN}$		I		
$P8_5$/$\overline{NMI}$	$\overline{NMI}$ interrupt input pin	I		Input pin for the $\overline{NMI}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Supply voltage	Description
$P9_0$ to $P9_7$	I/O port P9	I/O	V_{CC1}	8-bit I/O ports having equivalent functions P0. The PRCR register prevents PD9 and PS3 registers from rewriting.
$TB0_{IN}$ to $TB4_{IN}$	Timer B pin	I		Input pins for timers B0 to B4
$\overline{CTS3}$, $\overline{CTS4}$	UART pin	I		I/O pins for UART3 ($P9_0$ to $P9_3$) and UART4 ($P9_4$ to $P9_7$)
$\overline{RTS3}$, $\overline{RTS4}$		O		
$\overline{SS3}$, $\overline{SS4}$		I		
CLK3, CLK4		I/O		
RxD3, RxD4		I		
SCL3, SCL4		I/O		
STxD3, STxD4		O		
TxD3, TxD4		O		
SDA3, SDA4		I/O		
SRxD3, SRxD4		I		
DA0, DA1	D-A output pin	O		Output pins for the D-A converter
ANEX0,	A-D related pin	I/O		ANEX0 is an extended analog I/O pin for the A-D converter.
ANEX1,		I		ANEX1 is an extended analog input pin for the A-D converter.
$\overline{ADTRG}$		I		$\overline{ADTRG}$ is an A-D trigger input pin.
$\overline{CAN1WU}$	CAN1 interrupt input pin	I		Input pin for the CAN1 wake-up interrupt.
$CAN1_{OUT}$,	CAN pin	O		Input pins for the CAN communication function
$CAN1_{IN}$		I		
$P10_0$ to $P10_7$	I/O port P10	I/O	V_{CC1}	8-bit I/O ports having equivalent functions to P0
$\overline{KI0}$ to $\overline{KI3}$	Key input interrupt pin	I		Input pins for the key input interrupt
AN_0 to AN_7	Analog input pin	I		Analog input pins for the A-D converter

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (144-Pin Package only) (Continued)

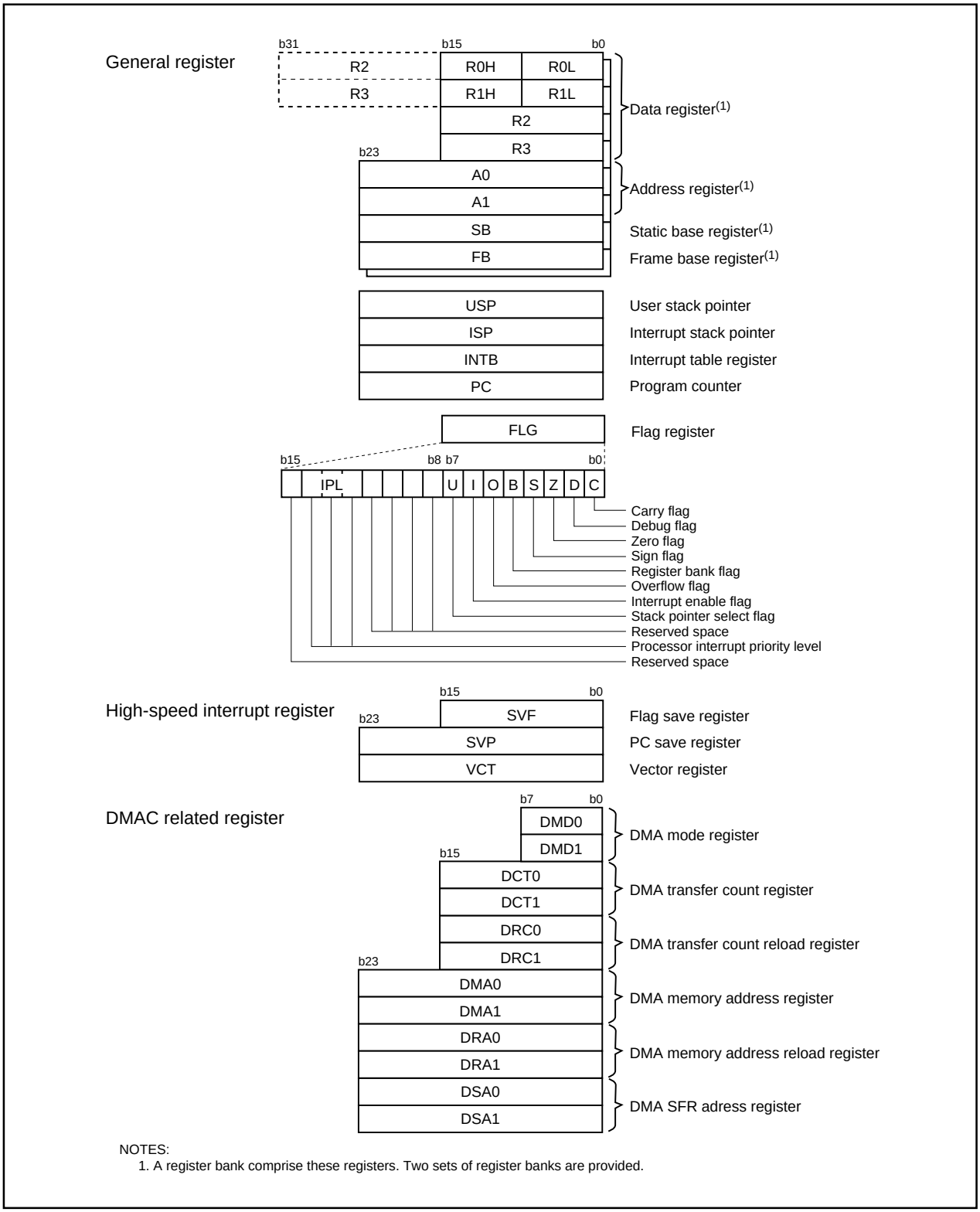
Symbol	Function	I/O type	Supply voltage	Description
$P11_0$ to $P11_4$	I/O port P11	I/O	V_{CC2}	5-bit I/O ports having equivalent functions to P0.
$INPC1_0$ to $INPC1_3$	Intelligent I/O pin	I		$INPC1_0$ to $INPC1_3$ are input pins for the time measurement function.
$OUTC1_0$ to $OUTC1_3$		O		$OUTC1_0$ to $OUTC1_3$ are output pins for the waveform generating function.
ISCLK1		I/O		ISCLK1 inputs and outputs the clock and is an I/O pin for the intelligent I/O communication function.
ISTxD1		O		
ISRxD1		I		ISRxD1 and $BE1_{IN}$ input received data for the intelligent I/O communication function.
$BE1_{OUT}$		O		
$BE1_{IN}$		I		ISTxD1 and $BE1_{OUT}$ output transmit data for the intelligent I/O communication function.
$P12_0$ to $P12_7$	I/O port P12	I/O	V_{CC2}	8-bit I/O ports having equivalent functions to P0
$P13_0$ to $P13_7$	I/O port P13	I/O	V_{CC2}	8-bit I/O ports having equivalent functions to P0
$P14_0$ to $P14_7$	I/O port P14	I/O	V_{CC1}	8-bit I/O ports having equivalent functions to P0
$INPC1_4$ to $INPC1_7$	Intelligent I/O pin	I		$INPC1_4$ to $INPC1_7$ are input pins for the time measurement function.
$OUTC1_4$ to $OUTC1_7$		O		$OUTC1_4$ to $OUTC1_7$ are output pins for the waveform generating function.
$P15_0$ to $P15_7$	I/O port P15	I/O	V_{CC1}	8-bit I/O ports having equivalent functions to P0
$AN15_0$ to $AN15_7$	Analog input port	I		Analog input pins for the A-D converter
ISCLK0	Intelligent I/O pin	I/O		ISCLK0 inputs and outputs the clock for the intelligent I/O communication function.
ISRxD0		I		ISRxD0 inputs received data for the intelligent I/O communication function.
ISTxD0		O		ISTxD0 outputs transmit data for the intelligent I/O communication function.

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

A register bank comprises 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.



NOTES:
1. A register bank comprise these registers. Two sets of register banks are provided.

Figure 2.1 CPU Register

2.1 General Register

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R3R1.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC is 24 bits wide. It indicates an address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating a starting address of an interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

USP and ISP as the stack pointer are 24 bits wide. The U flag can switch USP to ISP and vice versa. Refer to "2.1.8 Flag Register (FLG)" about the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow occurs after an instruction is executed.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic calculation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic calculation; otherwise "0".

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when a result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
An interrupt is disabled when the I flag is set to "0" and is enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".
The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide. It assigns an interrupt priority levels from level 0 to level 7.
If a requested interrupt has a greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to the reserved space, set to "0". When read, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows.

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-associated Registers

Registers associated with DMAC are as follows.

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/85 group.

The M32C/85 provides 16-Mbyte address space from addresses 000000$_{16}$ to FFFFFF$_{16}$.

The internal ROM is allocated in lower addresses beginning with address FFFFFF$_{16}$. For example, a 64-Kbyte internal ROM is allocated in addresses FF0000$_{16}$ to FFFFFF$_{16}$.

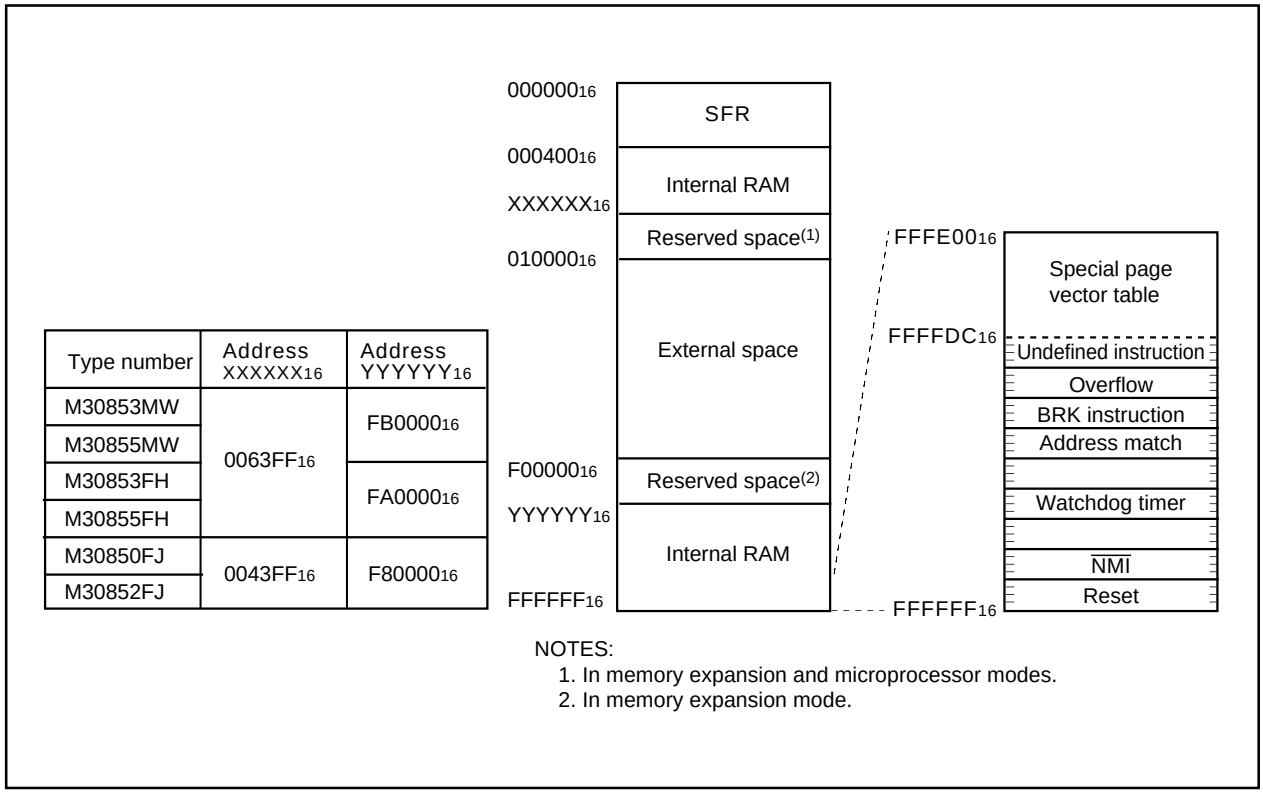
The fixed interrupt vectors are allocated in addresses FFFFDC$_{16}$ to FFFFFF$_{16}$. It stores the starting address of each interrupt routine.

The internal RAM is allocated in higher addresses beginning with address 000400$_{16}$. For example, a 10-Kbyte internal RAM is allocated in addresses 000400$_{16}$ to 002BFF$_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowleged.

The SFR is allocated in addresses 000000$_{16}$ to 0003FF$_{16}$. The control registers for peripheral functions such as I/O port, A-D conversion, serial I/O, timer are allocated here. All addresses, which have nothing allocated within the SFR, are reserved space and cannot be accessed by users.

The special page vectors are allocated in addresses FFFE00$_{16}$ to FFFFDB$_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **Software Manual** for details.

In memory expansion mode and microprocessor mode, some space are reserved and cannot be accessed by users.



Type number	Address XXXXXX$_{16}$	Address YYYYYY$_{16}$
M30853MW	0063FF$_{16}$	FB0000$_{16}$
M30855MW		
M30853FH		FA0000$_{16}$
M30855FH		
M30850FJ	0043FF$_{16}$	F80000$_{16}$
M30852FJ		

Figure 3.1 Memory Map

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
0000$_{16}$			
0001$_{16}$			
0002$_{16}$			
0003$_{16}$			
0004$_{16}$	Processor mode register 0	PM0	1000 0000$_2$(CNVss pin ="L") 0000 0011$_2$(CNVss pin ="H")
0005$_{16}$	Processor mode register 1	PM1	0X00 0000$_2$
0006$_{16}$	System clock control register 0	CM0	0000 1000$_2$
0007$_{16}$	System clock control register 1	CM1	0010 0000$_2$
0008$_{16}$			
0009$_{16}$	Address match interrupt enable register	AIER	00$_{16}$
000A$_{16}$	Protect register	PRCR	XXXX 0000$_2$
000B$_{16}$	External data bus width control register	DS	XXXX 1000$_2$(BYTE pin ="L") XXXX 0000$_2$(BYTE pin ="H")
000C$_{16}$	Main clock division register	MCD	XXX0 1000$_2$
000D$_{16}$	Oscillation stop detect register	CM2	00$_{16}$
000E$_{16}$	Watchdog timer start register	WDTS	XX$_{16}$
000F$_{16}$	Watchdog timer control register	WDC	000X XXXX$_2$
0010$_{16}$ 0011$_{16}$ 0012$_{16}$	Address match interrupt register 0	RMAD0	000000$_{16}$
0013$_{16}$	Processor mode register 2	PM2	XXX0 0000$_2$
0014$_{16}$ 0015$_{16}$ 0016$_{16}$	Address match interrupt register 1	RMAD1	000000$_{16}$
0017$_{16}$	Voltage detection register 2	VCR2	00$_{16}$
0018$_{16}$ 0019$_{16}$ 001A$_{16}$	Address match interrupt register 2	RMAD2	000000$_{16}$
001B$_{16}$	Voltage detection register 1	VCR1	0000 1000$_2$
001C$_{16}$ 001D$_{16}$ 001E$_{16}$	Address match interrupt register 3	RMAD3	000000$_{16}$
001F$_{16}$			
0020$_{16}$			
0021$_{16}$			
0022$_{16}$			
0023$_{16}$			
0024$_{16}$			
0025$_{16}$			
0026$_{16}$	PLL control register 0	PLC0	0001 X010$_2$
0027$_{16}$	PLL control register 1	PLC1	000X 0000$_2$
0028$_{16}$ 0029$_{16}$ 002A$_{16}$	Address match interrupt register 4	RMAD4	000000$_{16}$
002B$_{16}$			
002C$_{16}$ 002D$_{16}$ 002E$_{16}$	Address match interrupt register 5	RMAD5	000000$_{16}$
002F$_{16}$	Voltage down detect interrupt register	D4INT	XX00 0000$_2$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆ 0039₁₆ 003A₁₆	Address match interrupt register 6	RMAD6	000000₁₆
003B₁₆			
003C₁₆ 003D₁₆ 003E₁₆	Address match interrupt register 7	RMAD7	000000₁₆
003F₁₆			
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆	External space wait control register 0	EWCR0	X0X0 0011₂
0049₁₆	External space wait control register 1	EWCR1	X0X0 0011₂
004A₁₆	External space wait control register 2	EWCR1	X0X0 0011₂
004B₁₆	External space wait control register 3	EWCR3	X0X0 0011₂
004C₁₆	Page mode wait control register 0	PWCR0	0001 0001₂
004D₁₆	Page mode wait control register 1	PWCR1	0001 0001₂
004E₁₆			
004F₁₆			
0050₁₆			
0051₁₆			
0052₁₆			
0053₁₆			
0054₁₆			
0055₁₆	Flash memory control register 1	FMR1	0000 0101₂
0056₁₆			
0057₁₆	Flash memory control register 0	FMR0	0000 0001₂
0058₁₆			
0059₁₆			
005A₁₆			
005B₁₆			
005C₁₆			
005D₁₆			
005E₁₆			
005F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
006016			
006116			
006216			
006316			
006416			
006516			
006616			
006716			
006816	DMA0 interrupt control register	DM0IC	XXXX X0002
006916	Timer B5 interrupt control register	TB5IC	XXXX X0002
006A16	DMA2 interrupt control register	DM2IC	XXXX X0002
006B16	UART2 receive /ACK interrupt control register	S2RIC	XXXX X0002
006C16	Timer A0 interrupt control register	TA0IC	XXXX X0002
006D16	UART3 receive /ACK interrupt control register	S3RIC	XXXX X0002
006E16	Timer A2 interrupt control register	TA2IC	XXXX X0002
006F16	UART4 receive /ACK interrupt control register	S4RIC	XXXX X0002
007016	Timer A4 interrupt control register	TA4IC	XXXX X0002
007116	UART0/UART3 bus conflict detect interrupt control register	BCN0IC/BCN3IC	XXXX X0002
007216	UART0 receive/ACK interrupt control register	S0RIC	XXXX X0002
007316	A-D0 conversion interrupt control register	AD0IC	XXXX X0002
007416	UART1 receive/ACK interrupt control register	S1RIC	XXXX X0002
007516	Intelligent I/O interrupt control register 0 CAN interrupt 3 control register	IIO0IC CAN3IC	XXXX X0002
007616	Timer B1 interrupt control register	TB1IC	XXXX X0002
007716	Intelligent I/O interrupt control register 2	IIO2IC	XXXX X0002
007816	Timer B3 interrupt control register	TB3IC	XXXX X0002
007916	Intelligent I/O interrupt control register 4	IIO4IC	XXXX X0002
007A16	INT5 interrupt control register	INT5IC	XX00 X0002
007B16			
007C16	INT3 interrupt control register	INT3IC	XX00 X0002
007D16	Intelligent I/O interrupt control register 8	IIO8IC	XXXX X0002
007E16	INT1 interrupt control register	INT1IC	XX00 X0002
007F16	Intelligent I/O interrupt control register 10/ CAN interrupt 1 control register	IIO10IC CAN1IC	XXXX X0002
008016			
008116	CAN interrupt 2 control register	CAN2IC	XXXX X0002
008216			
008316			
008416			
008516			
008616			
008716			
008816	DMA1 interrupt control register	DM1IC	XXXX X0002
008916	UART2 transmit /NACK interrupt control register	S2TIC	XXXX X0002
008A16	DMA3 interrupt control register	DM3IC	XXXX X0002
008B16	UART3 transmit /NACK interrupt control register	S3TIC	XXXX X0002
008C16	Timer A1 interrupt control register	TA1IC	XXXX X0002
008D16	UART4 transmit /NACK interrupt control register	S4TIC	XXXX X0002
008E16	Timer A3 interrupt control register	TA3IC	XXXX X0002
008F16	UART2 bus conflict detect interrupt control register	BCN2IC	XXXX X0002

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
009016	UART0 transmit /NACK interrupt control register	S0TIC	XXXX X0002
009116	UART1/UART4 bus conflict detect interrupt control register	BCN1IC/BCN4IC	XXXX X0002
009216	UART1 transmit/NACK interrupt control register	S1TIC	XXXX X0002
009316	Key input interrupt control register	KUPIC	XXXX X0002
009416	Timer B0 interrupt control register	TB0IC	XXXX X0002
009516	Intelligent I/O interrupt control register 1 CAN interrupt 4 control register	IIO1IC CAN4IC	XXXX X0002
009616	Timer B2 interrupt control register	TB2IC	XXXX X0002
009716	Intelligent I/O interrupt control register 3	IIO3IC	XXXX X0002
009816	Timer B4 interrupt control register	TB4IC	XXXX X0002
009916	CAN interrupt 5 control register	CAN5IC	XXXX X0002
009A16	INT4 interrupt control register	INT4IC	XX00 X0002
009B16			
009C16	INT2 interrupt control register	INT2IC	XX00 X0002
009D16	Intelligent I/O interrupt control register 9/ CAN interrupt 0 control register	IIO9IC CAN0IC	XXXX X0002
009E16	INT0 interrupt control register	INT0IC	XX00 X0002
009F16	Exit priority control register	RLVL	XXXX 00002
00A016	Interrupt request register 0	IIO0IR	0000 X00X2
00A116	Interrupt request register 1	IIO1IR	0000 X00X2
00A216	Interrupt request register 2	IIO2IR	0000 X00X2
00A316	Interrupt request register 3	IIO3IR	0000 X00X2
00A416	Interrupt request register 4	IIO4IR	0000 X00X2
00A516	Interrupt request register 5	IIO5IR	0000 X00X2
00A616			
00A716			
00A816	Interrupt request register 8	IIO8IR	0000 X00X2
00A916	Interrupt request register 9	IIO9IR	0000 X00X2
00AA16	Interrupt request register 10	IIO10IR	0000 X00X2
00AB16	Interrupt request register 11	IIO11IR	0000 X00X2
00AC16			
00AD16			
00AE16			
00AF16			
00B016	Interrupt enable register 0	IIO0IE	0000 X0002
00B116	Interrupt enable register 1	IIO1IE	0000 X0002
00B216	Interrupt enable register 2	IIO2IE	0000 X0002
00B316	Interrupt enable register 3	IIO3IE	0000 X0002
00B416	Interrupt enable register 4	IIO4IE	0000 X0002
00B516	Interrupt enable register 5	IIO5IE	0000 X0002
00B616			
00B716			
00B816	Interrupt enable register 8	IIO8IE	0000 X0002
00B916	Interrupt enable register 9	IIO9IE	0000 X0002
00BA16	Interrupt enable register 10	IIO10IE	0000 X0002
00BB16	Interrupt enable register 11	IIO11IE	0000 X0002
00BC16			
00BD16			
00BE16			
00BF16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0$_{16}$			
00C1$_{16}$			
00C2$_{16}$			
00C3$_{16}$			
00C4$_{16}$			
00C5$_{16}$			
00C6$_{16}$			
00C7$_{16}$			
00C8$_{16}$			
00C9$_{16}$			
00CA$_{16}$			
00CB$_{16}$			
00CC$_{16}$			
00CD$_{16}$			
00CE$_{16}$			
00CF$_{16}$			
00D0$_{16}$			
00D1$_{16}$			
00D2$_{16}$			
00D3$_{16}$			
00D4$_{16}$			
00D5$_{16}$			
00D6$_{16}$			
00D7$_{16}$			
00D8$_{16}$			
00D9$_{16}$			
00DA$_{16}$			
00DB$_{16}$			
00DC$_{16}$			
00DD$_{16}$			
00DE$_{16}$			
00DF$_{16}$			
00E0$_{16}$			
00E1$_{16}$			
00E2$_{16}$			
00E3$_{16}$			
00E4$_{16}$			
00E5$_{16}$			
00E6$_{16}$			
00E7$_{16}$			
00E8$_{16}$ 00E9$_{16}$	SI/O receive buffer register 0	G0RB	XXXX XXXX$_2$ XX00 XXXX$_2$
00EA$_{16}$	Transmit buffer/receive data register 0	G0TB	XX$_{16}$
00EB$_{16}$			
00EC$_{16}$	Receive input register 0	G0RI	XX$_{16}$
00ED$_{16}$	SI/O communication mode register 0	G0MR	00$_{16}$
00EE$_{16}$	Transmit output register 0	G0TO	XX$_{16}$
00EF$_{16}$	SI/O communication control register 0	G0CR	0000 X011$_2$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00F0$_{16}$	Data compare register 00	G0CMP0	XX$_{16}$
00F1$_{16}$	Data compare register 01	G0CMP1	XX$_{16}$
00F2$_{16}$	Data compare register 02	G0CMP2	XX$_{16}$
00F3$_{16}$	Data compare register 03	G0CMP3	XX$_{16}$
00F4$_{16}$	Data mask register 00	G0MSK0	XX$_{16}$
00F5$_{16}$	Data mask register 01	G0MSK1	XX$_{16}$
00F6$_{16}$	Communication clock select register	CCS	XXXX 0000$_2$
00F7$_{16}$			
00F8$_{16}$ 00F9$_{16}$	Receive CRC code register 0	G0RCRC	XX$_{16}$ XX$_{16}$
00FA$_{16}$ 00FB$_{16}$	Transmit CRC code register 0	G0TCRC	00$_{16}$ 00$_{16}$
00FC$_{16}$	SI/O extended mode register 0	G0EMR	00$_{16}$
00FD$_{16}$	SI/O extended receive control register 0	G0ERC	00$_{16}$
00FE$_{16}$	SI/O special communication interrupt detect register 0	G0IRF	0000 00XX$_2$
00FF$_{16}$	SI/O extended transmit control register 0	G0ETC	0000 0XXX$_2$
0100$_{16}$ 0101$_{16}$	Time measurement/waveform generating register 10	G1TM0/G1PO0	XX$_{16}$ XX$_{16}$
0102$_{16}$ 0103$_{16}$	Time measurement/waveform generating register 11	G1TM1/G1PO1	XX$_{16}$ XX$_{16}$
0104$_{16}$ 0105$_{16}$	Time measurement/waveform generating register 12	G1TM2/G1PO2	XX$_{16}$ XX$_{16}$
0106$_{16}$ 0107$_{16}$	Time measurement/waveform generating register 13	G1TM3/G1PO3	XX$_{16}$ XX$_{16}$
0108$_{16}$ 0109$_{16}$	Time measurement/waveform generating register 14	G1TM4/G1PO4	XX$_{16}$ XX$_{16}$
010A$_{16}$ 010B$_{16}$	Time measurement/waveform generating register 15	G1TM5/G1PO5	XX$_{16}$ XX$_{16}$
010C$_{16}$ 010D$_{16}$	Time measurement/waveform generating register 16	G1TM6/G1PO6	XX$_{16}$ XX$_{16}$
010E$_{16}$ 010F$_{16}$	Time measurement/waveform generating register 17	G1TM7/G1PO7	XX$_{16}$ XX$_{16}$
0110$_{16}$	Waveform generating control register 10	G1POCR0	0000 X000$_2$
0111$_{16}$	Waveform generating control register 11	G1POCR1	0X00 X000$_2$
0112$_{16}$	Waveform generating control register 12	G1POCR2	0X00 X000$_2$
0113$_{16}$	Waveform generating control register 13	G1POCR3	0X00 X000$_2$
0114$_{16}$	Waveform generating control register 14	G1POCR4	0X00 X000$_2$
0115$_{16}$	Waveform generating control register 15	G1POCR5	0X00 X000$_2$
0116$_{16}$	Waveform generating control register 16	G1POCR6	0X00 X000$_2$
0117$_{16}$	Waveform generating control register 17	G1POCR7	0X00 X000$_2$
0118$_{16}$	Time measurement control register 10	G1TMCR0	00$_{16}$
0119$_{16}$	Time measurement control register 11	G1TMCR1	00$_{16}$
011A$_{16}$	Time measurement control register 12	G1TMCR2	00$_{16}$
011B$_{16}$	Time measurement control register 13	G1TMCR3	00$_{16}$
011C$_{16}$	Time measurement control register 14	G1TMCR4	00$_{16}$
011D$_{16}$	Time measurement control register 15	G1TMCR5	00$_{16}$
011E$_{16}$	Time measurement control register 16	G1TMCR6	00$_{16}$
011F$_{16}$	Time measurement control register 17	G1TMCR7	00$_{16}$

X: Indeterminate

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Address	Register	Symbol	Value after RESET
012016	Base timer register 1	G1BT	XX16
012116			XX16
012216	Base timer control register 10	G1BCR0	0016
012316	Base timer control register 11	G1BCR1	0016
012416	Time measurement prescaler register 16	G1TPR6	0016
012516	Time measurement prescaler register 17	G1TPR7	0016
012616	Function enable register 1	G1FE	0016
012716	Function select register 1	G1FS	0016
012816	SI/O receive buffer register 1	G1RB	XXXX XXXX2
012916			XX00 XXXX2
012A16	Transmit buffer/receive data register 1	G1TB	XX16
012B16			
012C16	Receive input register 1	G1RI	XX16
012D16	SI/O communication mode register 1	G1MR	0016
012E16	Transmit output register 1	G1TO	XX16
012F16	SI/O communication control register 1	G1CR	0000 X0112
013016	Data compare register 10	G1CMP0	XX16
013116	Data compare register 11	G1CMP1	XX16
013216	Data compare register 12	G1CMP2	XX16
013316	Data compare register 13	G1CMP3	XX16
013416	Data mask register 10	G1MSK0	XX16
013516	Data mask register 11	G1MSK1	XX16
013616			
013716			
013816	Receive CRC code register 1	G1RCRC	XX16
013916			XX16
013A16	Transmit CRC code register 1	G1TCRC	0016
013B16			0016
013C16	SI/O extended mode register 1	G1EMR	0016
013D16	SI/O extended receive control register 1	G1ERC	0016
013E16	SI/O special communication interrupt detect register 1	G1IRF	0000 00XX2
013F16	SI/O extended transmit control register 1	G1ETC	0000 0XXX2
014016			
014116			
014216			
014316			
014416			
014516			
014616			
014716			
014816			
014916			
014A16			
014B16			
014C16			
014D16			
014E16			
014F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0150₁₆			
0151₁₆			
0152₁₆			
0153₁₆			
0154₁₆			
0155₁₆			
0156₁₆			
0157₁₆			
0158₁₆			
0159₁₆			
015A₁₆			
015B₁₆			
015C₁₆			
015D₁₆			
015E₁₆			
015F₁₆			
0160₁₆			
0161₁₆			
0162₁₆			
0163₁₆			
0164₁₆			
0165₁₆			
0166₁₆			
0167₁₆			
0168₁₆			
0169₁₆			
016A₁₆			
016B₁₆			
016C₁₆			
016D₁₆			
016E₁₆			
016F₁₆			
0170₁₆			
0171₁₆			
0172₁₆			
0173₁₆			
0174₁₆			
0175₁₆			
0176₁₆			
0177₁₆			
0178₁₆	Input function select register	IPS	00₁₆
0179₁₆	Input function select register A	IPSA	00₁₆
017A₁₆			
017B₁₆			
017C₁₆			
017D₁₆ to 01DF₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
01E0$_{16}$	CAN0 message slot buffer 0 standard ID0	C0SLOT0_0	XX$_{16}$
01E1$_{16}$	CAN0 message slot buffer 0 standard ID1	C0SLOT0_1	XX$_{16}$
01E2$_{16}$	CAN0 message slot buffer 0 extended ID0	C0SLOT0_2	XX$_{16}$
01E3$_{16}$	CAN0 message slot buffer 0 extended ID1	C0SLOT0_3	XX$_{16}$
01E4$_{16}$	CAN0 message slot buffer 0 extended ID2	C0SLOT0_4	XX$_{16}$
01E5$_{16}$	CAN0 message slot buffer 0 data length code	C0SLOT0_5	XX$_{16}$
01E6$_{16}$	CAN0 message slot buffer 0 data 0	C0SLOT0_6	XX$_{16}$
01E7$_{16}$	CAN0 message slot buffer 0 data 1	C0SLOT0_7	XX$_{16}$
01E8$_{16}$	CAN0 message slot buffer 0 data 2	C0SLOT0_8	XX$_{16}$
01E9$_{16}$	CAN0 message slot buffer 0 data 3	C0SLOT0_9	XX$_{16}$
01EA$_{16}$	CAN0 message slot buffer 0 data 4	C0SLOT0_10	XX$_{16}$
01EB$_{16}$	CAN0 message slot buffer 0 data 5	C0SLOT0_11	XX$_{16}$
01EC$_{16}$	CAN0 message slot buffer 0 data 6	C0SLOT0_12	XX$_{16}$
01ED$_{16}$	CAN0 message slot buffer 0 data 7	C0SLOT0_13	XX$_{16}$
01EE$_{16}$	CAN0 message slot buffer 0 time stamp high-order	C0SLOT0_14	XX$_{16}$
01EF$_{16}$	CAN0 message slot buffer 0 time stamp low-order	C0SLOT0_15	XX$_{16}$
01F0$_{16}$	CAN0 message slot buffer 1 standard ID0	C0SLOT1_0	XX$_{16}$
01F1$_{16}$	CAN0 message slot buffer 1 standard ID1	C0SLOT1_1	XX$_{16}$
01F2$_{16}$	CAN0 message slot buffer 1 extended ID0	C0SLOT1_2	XX$_{16}$
01F3$_{16}$	CAN0 message slot buffer 1 extended ID1	C0SLOT1_3	XX$_{16}$
01F4$_{16}$	CAN0 message slot buffer 1 extended ID2	C0SLOT1_4	XX$_{16}$
01F5$_{16}$	CAN0 message slot buffer 1 data length code	C0SLOT1_5	XX$_{16}$
01F6$_{16}$	CAN0 message slot buffer 1 data 0	C0SLOT1_6	XX$_{16}$
01F7$_{16}$	CAN0 message slot buffer 1 data 1	C0SLOT1_7	XX$_{16}$
01F8$_{16}$	CAN0 message slot buffer 1 data 2	C0SLOT1_8	XX$_{16}$
01F9$_{16}$	CAN0 message slot buffer 1 data 3	C0SLOT1_9	XX$_{16}$
01FA$_{16}$	CAN0 message slot buffer 1 data 4	C0SLOT1_10	XX$_{16}$
01FB$_{16}$	CAN0 message slot buffer 1 data 5	C0SLOT1_11	XX$_{16}$
01FC$_{16}$	CAN0 message slot buffer 1 data 6	C0SLOT1_12	XX$_{16}$
01FD$_{16}$	CAN0 message slot buffer 1 data 7	C0SLOT1_13	XX$_{16}$
01FE$_{16}$	CAN0 message slot buffer 1 time stamp high-order	C0SLOT1_14	XX$_{16}$
01FF$_{16}$	CAN0 message slot buffer 1 time stamp low-order	C0SLOT1_15	XX$_{16}$
0200$_{16}$ 0201$_{16}$	CAN0 control register 0	C0CTLR0	XX01 0X01$_2$(1) XXXX 0000$_2$(1)
0202$_{16}$ 0203$_{16}$	CAN0 status register	C0STR	00$_{16}$(1) X000 0X01$_2$(1)
0204$_{16}$ 0205$_{16}$	CAN0 extended ID register	C0IDR	00$_{16}$(1) 00$_{16}$(1)
0206$_{16}$ 0207$_{16}$	CAN0 configuration register	C0CONR	0000 XXXX$_2$(1) 0000 0000$_2$(1)
0208$_{16}$ 0209$_{16}$	CAN0 time stamp register	C0TSR	00$_{16}$(1) 00$_{16}$(1)
020A$_{16}$	CAN0 transmit error count register	C0TEC	00$_{16}$(1)
020B$_{16}$	CAN0 receive error count register	C0REC	00$_{16}$(1)
020C$_{16}$ 020D$_{16}$	CAN0 slot interrupt status register	C0SISTR	00$_{16}$(1) 00$_{16}$(1)
020E$_{16}$			
020F$_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
021016 021116	CAN0 slot interrupt mask register	C0SIMKR	0016(2) 0016(2)
021216			
021316			
021416	CAN0 error interrupt mask register	C0EIMKR	XXXX X0002(2)
021516	CAN0 error interrupt status register	C0EISTR	XXXX X0002(2)
021616	CAN0 error cause register	C0EFR	0016(2)
021716	CAN0 baud rate prescaler	C0BRP	0000 00012(2)
021816			
021916	CAN0 mode register	C0MDR	XXXX XX002(2)
021A16			
021B16			
021C16			
021D16			
021E16			
021F16			
022016 022116	CAN0 single shot control register	C0SSCTLR	0016(2) 0016(2)
022216			
022316			
022416 022516	CAN0 single shot status register	C0SSSTR	0016(2) 0016(2)
022616			
022716			
022816	CAN0 global mask register standard ID0	C0GMR0	XXX0 00002(2)
022916	CAN0 global mask register standard ID1	C0GMR1	XX00 00002(2)
022A16	CAN0 global mask register extended ID0	C0GMR2	XXXX 00002(2)
022B16	CAN0 global mask register extended ID1	C0GMR3	0016(2)
022C16	CAN0 global mask register extended ID2	C0GMR4	XX00 00002(2)
022D16			
022E16			
022F16			
023016	CAN0 message slot 0 control register / CAN0 local mask register A standard ID0	C0MCTL0/ C0LMAR0	0000 00002(2) XXX0 00002(2)
023116	CAN0 message slot 1 control register / CAN0 local mask register A standard ID1	C0MCTL1/ C0LMAR1	0000 00002(2) XX00 00002(2)
023216	CAN0 message slot 2 control register / CAN0 local mask register A extended ID0	C0MCTL2/ C0LMAR2	0000 00002(2) XXXX 00002(2)
023316	CAN0 message slot 3 control register / CAN0 local mask register A extended ID1	C0MCTL3/ C0LMAR3	0016(2) 0016(2)
023416	CAN0 message slot 4 control register / CAN0 local mask register A extended ID2	C0MCTL4/ C0LMAR4	0000 00002(2) XX00 00002(2)
023516	CAN0 message slot 5 control register	C0MCTL5	0016(2)
023616	CAN0 message slot 6 control register	C0MCTL6	0016(2)
023716	CAN0 message slot 7 control register	C0MCTL7	0016(2)
023816	CAN0 message slot 8 control register / CAN0 local mask register B standard ID0	C0MCTL8/ C0LMBR0	0000 00002(2) XXX0 00002(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
023916	CAN0 message slot 9 control register / CAN0 local mask register B standard ID1	C0MCTL9/ C0LMBR1	0000 00002(2) XX00 00002(2)
023A16	CAN0 message slot 10 control register / CAN0 local mask register B extended ID0	C0MCTL10/ C0LMBR2	0000 00002(2) XXXX 00002(2)
023B16	CAN0 message slot 11 control register / CAN0 local mask register B extended ID1	C0MCTL11/ C0LMBR3	0016(2) 0016(2)
023C16	CAN0 message slot 12 control register / CAN0 local mask register B extended ID2	C0MCTL12/ C0LMBR4	0000 00002(2) XX00 00002(2)
023D16	CAN0 message slot 13 control register	C0MCTL13	0016(2)
023E16	CAN0 message slot 14 control register	C0MCTL14	0016(2)
023F16	CAN0 message slot 15 control register	C0MCTL15	0016(2)
024016	CAN0 slot buffer select register	C0SBS	0016(2)
024116	CAN0 control register 1	C0CTLR1	X000 00XX2(2)
024216	CAN0 sleep control register	C0SLPR	XXXX XXX02
024316			
024416 024516	CAN0 acceptance filter support register	C0AFS	0016(2) 0116(2)
024616			
024716			
024816			
024916			
024A16			
024B16			
024C16			
024D16			
024E16			
024F16			
025016	CAN1 slot buffer select register	C1SBS	0016(3)
025116	CAN1 control register 1	C1CTLR1	X000 00XX2(3)
025216	CAN1 sleep control register	C1SLPR	XXXX XXX02(3)
025316			
025416 025516	CAN1 acceptance filter support register	C1AFS	0016(3) 0116(3)
025616			
025716			
025816			
025916			
025A16			
025B16			
025C16			
025D16			
025E16			
025F16			

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.
3. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
026016	CAN1 message slot buffer 0 standard ID0	C1SLOT0_0	XX16
026116	CAN1 message slot buffer 0 standard ID1	C1SLOT0_1	XX16
026216	CAN1 message slot buffer 0 extended ID0	C1SLOT0_2	XX16
026316	CAN1 message slot buffer 0 extended ID1	C1SLOT0_3	XX16
026416	CAN1 message slot buffer 0 extended ID2	C1SLOT0_4	XX16
026516	CAN1 message slot buffer 0 data length code	C1SLOT0_5	XX16
026616	CAN1 message slot buffer 0 data 0	C1SLOT0_6	XX16
026716	CAN1 message slot buffer 0 data 1	C1SLOT0_7	XX16
026816	CAN1 message slot buffer 0 data 2	C1SLOT0_8	XX16
026916	CAN1 message slot buffer 0 data 3	C1SLOT0_9	XX16
026A16	CAN1 message slot buffer 0 data 4	C1SLOT0_10	XX16
026B16	CAN1 message slot buffer 0 data 5	C1SLOT0_11	XX16
026C16	CAN1 message slot buffer 0 data 6	C1SLOT0_12	XX16
026D16	CAN1 message slot buffer 0 data 7	C1SLOT0_13	XX16
026E16	CAN1 message slot buffer 0 time stamp high-order	C1SLOT0_14	XX16
026F16	CAN1 message slot buffer 0 time stamp low-order	C1SLOT0_15	XX16
027016	CAN1 message slot buffer 1 standard ID0	C1SLOT1_0	XX16
027116	CAN1 message slot buffer 1 standard ID1	C1SLOT1_1	XX16
027216	CAN1 message slot buffer 1 extended ID0	C1SLOT1_2	XX16
027316	CAN1 message slot buffer 1 extended ID1	C1SLOT1_3	XX16
027416	CAN1 message slot buffer 1 extended ID2	C1SLOT1_4	XX16
027516	CAN1 message slot buffer 1 data length code	C1SLOT1_5	XX16
027616	CAN1 message slot buffer 1 data 0	C1SLOT1_6	XX16
027716	CAN1 message slot buffer 1 data 1	C1SLOT1_7	XX16
027816	CAN1 message slot buffer 1 data 2	C1SLOT1_8	XX16
027916	CAN1 message slot buffer 1 data 3	C1SLOT1_9	XX16
027A16	CAN1 message slot buffer 1 data 4	C1SLOT1_10	XX16
027B16	CAN1 message slot buffer 1 data 5	C1SLOT1_11	XX16
027C16	CAN1 message slot buffer 1 data 6	C1SLOT1_12	XX16
027D16	CAN1 message slot buffer 1 data 7	C1SLOT1_13	XX16
027E16	CAN1 message slot buffer 1 time stamp high-order	C1SLOT1_14	XX16
027F16	CAN1 message slot buffer 1 time stamp low-order	C1SLOT1_15	XX16
028016 028116	CAN1 control register 0	C1CTLR0	XX01 0X012(1) XXXX 00002(1)
028216 028316	CAN1 status register	C1STR	0000 00002(1) X000 0X012(1)
028416 028516	CAN1 extended ID register	C1IDR	0016(1) 0016(1)
028616 028716	CAN1 configuration register	C1CONR	0000 XXXX2(1) 0000 00002(1)
028816 028916	CAN1 time stamp register	C1TSR	0016(1) 0016(1)
028A16	CAN1 transmit error count register	C1TEC	0016(1)
028B16	CAN1 receive error count register	C1REC	0016(1)
028C16 028D16	CAN1 slot interrupt status register	C1SISTR	0016(1) 0016(1)
028E16			
028F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
029016 029116	CAN1 slot interrupt mask register	C1SIMKR	0016(2) 0016(2)
029216			
029316			
029416	CAN1 error interrupt mask register	C1EIMKR	XXXX X0002(2)
029516	CAN1 error interrupt status register	C1EISTR	XXXX X0002(2)
029616	CAN1 error factor register	C1EFR	0016(2)
029716	CAN1 baud rate prescaler	C1BRP	0000 00012(2)
029816			
029916	CAN1 mode register	C1MDR	XXXX XX002(2)
029A16			
029B16			
029C16			
029D16			
029E16			
029F16			
02A016 02A116	CAN1 single shot control register	C1SSCTLR	0016(2) 0016(2)
02A216			
02A316			
02A416 02A516	CAN1 single shot status register	C1SSSTR	0016(2) 0016(2)
02A616			
02A716			
02A816	CAN1 global mask register standard ID0	C1GMR0	XXX0 00002(2)
02A916	CAN1 global mask register standard ID1	C1GMR1	XX00 00002(2)
02AA16	CAN1 global mask register extended ID0	C1GMR2	XXXX 00002(2)
02AB16	CAN1 global mask register extended ID1	C1GMR3	0016(2)
02AC16	CAN1 global mask register extended ID2	C1GMR4	XX00 00002(2)
02AD16			
02AE16			
02AF16			
02B016	CAN1 message slot 0 control register / CAN1 local mask register A standard ID0	C1MCTL0/ C1LMAR0	0000 00002(2) XXX0 00002(2)
02B116	CAN1 message slot 1 control register / CAN1 local mask register A standard ID1	C1MCTL1/ C1LMAR1	0000 00002(2) XX00 00002(2)
02B216	CAN1 message slot 2 control register / CAN1 local mask register A extended ID0	C1MCTL2/ C1LMAR2	0000 00002(2) XXXX 00002(2)
02B316	CAN1 message slot 3 control register / CAN1 local mask register A extended ID1	C1MCTL3/ C1LMAR3	0016(2) 0016(2)
02B416	CAN1 message slot 4 control register / CAN1 local mask register A extended ID2	C1MCTL4/ C1LMAR4	0000 00002(2) XX00 00002(2)
02B516	CAN1 message slot 5 control register	C1MCTL5	0016(2)
02B616	CAN1 message slot 6 control register	C1MCTL6	0016(2)
02B716	CAN1 message slot 7 control register	C1MCTL7	0016(2)
02B816	CAN1 message slot 8 control register / CAN1 local mask register B standard ID0	C1MCTL8/ C1LMBR0	0000 00002(2) XXX0 00002(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 02A016 to 02BF16.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02B916	CAN1 message slot 9 control register / CAN1 local mask register B standard ID1	C1MCTL9/ C1LMBR1	0000 00002(2) XX00 00002(2)
02BA16	CAN1 message slot 10 control register / CAN1 local mask register B extended ID0	C1MCTL10/ C1LMBR2	0000 00002(2) XXXX 00002(2)
02BB16	CAN1 message slot 11 control register / CAN1 local mask register B extended ID1	C1MCTL11/ C1LMBR3	0016(2) 0016(2)
02BC16	CAN1 message slot 12 control register / CAN1 local mask register B extended ID2	C1MCTL12/ C1LMBR4	0000 00002(2) XX00 00002(2)
02BD16	CAN1 message slot 13 control register	C1MCTL13	0016(2)
02BE16	CAN1 message slot 14 control register	C1MCTL14	0016(2)
02BF16	CAN1 message slot 15 control register	C1MCTL15	0016(2)
02C016 02C116	X0 register Y0 register	X0R,Y0R	XX16 XX16
02C216 02C316	X1 register Y1 register	X1R,Y1R	XX16 XX16
02C416 02C516	X2 register Y2 register	X2R,Y2R	XX16 XX16
02C616 02C716	X3 register Y3 register	X3R,Y3R	XX16 XX16
02C816 02C916	X4 register Y4 register	X4R,Y4R	XX16 XX16
02CA16 02CB16	X5 register Y5 register	X5R,Y5R	XX16 XX16
02CC16 02CD16	X6 register Y6 register	X6R,Y6R	XX16 XX16
02CE16 02CF16	X7 register Y7 register	X7R,Y7R	XX16 XX16
02D016 02D116	X8 register Y8 register	X8R,Y8R	XX16 XX16
02D216 02D316	X9 register Y9 register	X9R,Y9R	XX16 XX16
02D416 02D516	X10 register Y10 register	X10R,Y10R	XX16 XX16
02D616 02D716	X11 register Y11 register	X11R,Y11R	XX16 XX16
02D816 02D916	X12 register Y12 register	X12R,Y12R	XX16 XX16
02DA16 02DB16	X13 register Y13 register	X13R,Y13R	XX16 XX16
02DC16 02DD16	X14 register Y14 register	X14R,Y14R	XX16 XX16
02DE16 02DF16	X15 register Y15 register	X15R,Y15R	XX16 XX16

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 02A016 to 02BF16.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02E0$_{16}$	XY control register	XYC	XXXX XX00$_2$
02E1$_{16}$			
02E2$_{16}$			
02E3$_{16}$			
02E4$_{16}$	UART1 special mode register 4	U1SMR4	00$_{16}$
02E5$_{16}$	UART1 special mode register 3	U1SMR3	00$_{16}$
02E6$_{16}$	UART1 special mode register 2	U1SMR2	00$_{16}$
02E7$_{16}$	UART1 special mode register	U1SMR	00$_{16}$
02E8$_{16}$	UART1 transmit/receive mode register	U1MR	00$_{16}$
02E9$_{16}$	UART1 baud rate register	U1BRG	XX$_{16}$
02EA$_{16}$ 02EB$_{16}$	UART1 transmit buffer register	U1TB	XX$_{16}$ XX$_{16}$
02EC$_{16}$	UART1 transmit/receive control register 0	U1C0	0000 1000$_2$
02ED$_{16}$	UART1 transmit/receive control register 1	U1C1	0000 0010$_2$
02EE$_{16}$ 02EF$_{16}$	UART1 receive buffer register	U1RB	XX$_{16}$ XX$_{16}$
02F0$_{16}$			
02F1$_{16}$			
02F2$_{16}$			
02F3$_{16}$			
02F4$_{16}$	UART4 special mode register 4	U4SMR4	00$_{16}$
02F5$_{16}$	UART4 special mode register 3	U4SMR3	00$_{16}$
02F6$_{16}$	UART4 special mode register 2	U4SMR2	00$_{16}$
02F7$_{16}$	UART4 special mode register	U4SMR	00$_{16}$
02F8$_{16}$	UART4 transmit/receive mode register	U4MR	00$_{16}$
02F9$_{16}$	UART4 baud rate register	U4BRG	XX$_{16}$
02FA$_{16}$ 02FB$_{16}$	UART4 transmit buffer register	U4TB	XX$_{16}$ XX$_{16}$
02FC$_{16}$	UART4 transmit/receive control register 0	U4C0	0000 1000$_2$
02FD$_{16}$	UART4 transmit/receive control register 1	U4C1	0000 0010$_2$
02FE$_{16}$ 02FF$_{16}$	UART4 receive buffer register	U4RB	XX$_{16}$ XX$_{16}$
0300$_{16}$	Timer B3,B4,B5 count start flag	TBSR	000X XXXX$_2$
0301$_{16}$			
0302$_{16}$ 0303$_{16}$	Timer A1-1 register	TA11	XX$_{16}$ XX$_{16}$
0304$_{16}$ 0305$_{16}$	Timer A2-1 register	TA21	XX$_{16}$ XX$_{16}$
0306$_{16}$ 0307$_{16}$	Timer A4-1 register	TA41	XX$_{16}$ XX$_{16}$
0308$_{16}$	Three-phase PWM control register 0	INVC0	00$_{16}$
0309$_{16}$	Three-phase PWM control register 1	INVC1	00$_{16}$
030A$_{16}$	Three-phase output buffer register 0	IDB0	XX11 1111$_2$
030B$_{16}$	Three-phase output buffer register 1	IDB1	XX11 1111$_2$
030C$_{16}$	Dead time timer	DTT	XX$_{16}$
030D$_{16}$	Timer B2 interrupt generating frequency set counter	ICTB2	XX$_{16}$
030E$_{16}$			
030F$_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0310₁₆	Timer B3 register	TB3	XX₁₆
0311₁₆			XX₁₆
0312₁₆	Timer B4 register	TB4	XX₁₆
0313₁₆			XX₁₆
0314₁₆	Timer B5 register	TB5	XX₁₆
0315₁₆			XX₁₆
0316₁₆			
0317₁₆			
0318₁₆			
0319₁₆			
031A₁₆			
031B₁₆	Timer B3 mode register	TB3MR	00XX 0000₂
031C₁₆	Timer B4 mode register	TB4MR	00XX 0000₂
031D₁₆	Timer B5 mode register	TB5MR	00XX 0000₂
031E₁₆			
031F₁₆	External interrupt cause select register	IFSR	00₁₆
0320₁₆			
0321₁₆			
0322₁₆			
0323₁₆			
0324₁₆	UART3 special mode register 4	U3SMR4	00₁₆
0325₁₆	UART3 special mode register 3	U3SMR3	00₁₆
0326₁₆	UART3 special mode register 2	U3SMR2	00₁₆
0327₁₆	UART3 special mode register	U3SMR	00₁₆
0328₁₆	UART3 transmit/receive mode register	U3MR	00₁₆
0329₁₆	UART3 baud rate register	U3BRG	XX₁₆
032A₁₆	UART3 transmit buffer register	U3TB	XX₁₆
032B₁₆			XX₁₆
032C₁₆	UART3 transmit/receive control register 0	U3C0	0000 1000₂
032D₁₆	UART3 transmit/receive control register 1	U3C1	0000 0010₂
032E₁₆	UART3 receive buffer register	U3RB	XX₁₆
032F₁₆			XX₁₆
0330₁₆			
0331₁₆			
0332₁₆			
0333₁₆			
0334₁₆	UART2 special mode register 4	U2SMR4	00₁₆
0335₁₆	UART2 special mode register 3	U2SMR3	00₁₆
0336₁₆	UART2 special mode register 2	U2SMR2	00₁₆
0337₁₆	UART2 special mode register	U2SMR	00₁₆
0338₁₆	UART2 transmit/receive mode register	U2MR	00₁₆
0339₁₆	UART2 baud rate register	U2BRG	XX₁₆
033A₁₆	UART2 transmit buffer register	U2TB	XX₁₆
033B₁₆			XX₁₆
033C₁₆	UART2 transmit/receive control register 0	U2C0	0000 1000₂
033D₁₆	UART2 transmit/receive control register 1	U2C1	0000 0010₂
033E₁₆	UART2 receive buffer register	U2RB	XX₁₆
033F₁₆			XX₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0340$_{16}$	Count start flag	TABSR	00$_{16}$
0341$_{16}$	Clock prescaler reset flag	CPSRF	0XXX XXXX$_2$
0342$_{16}$	One-shot start flag	ONSF	00$_{16}$
0343$_{16}$	Trigger select register	TRGSR	00$_{16}$
0344$_{16}$	Up-down flag	UDF	00$_{16}$
0345$_{16}$			
0346$_{16}$ 0347$_{16}$	Timer A0 register	TA0	XX$_{16}$ XX$_{16}$
0348$_{16}$ 0349$_{16}$	Timer A1 register	TA1	XX$_{16}$ XX$_{16}$
034A$_{16}$ 034B$_{16}$	Timer A2 register	TA2	XX$_{16}$ XX$_{16}$
034C$_{16}$ 034D$_{16}$	Timer A3 register	TA3	XX$_{16}$ XX$_{16}$
034E$_{16}$ 034F$_{16}$	Timer A4 register	TA4	XX$_{16}$ XX$_{16}$
0350$_{16}$ 0351$_{16}$	Timer B0 register	TB0	XX$_{16}$ XX$_{16}$
0352$_{16}$ 0353$_{16}$	Timer B1 register	TB1	XX$_{16}$ XX$_{16}$
0354$_{16}$ 0355$_{16}$	Timer B2 register	TB2	XX$_{16}$ XX$_{16}$
0356$_{16}$	Timer A0 mode register	TA0MR	0000 0X00$_2$
0357$_{16}$	Timer A1 mode register	TA1MR	0000 0X00$_2$
0358$_{16}$	Timer A2 mode register	TA2MR	0000 0X00$_2$
0359$_{16}$	Timer A3 mode register	TA3MR	0000 0X00$_2$
035A$_{16}$	Timer A4 mode register	TA4MR	0000 0X00$_2$
035B$_{16}$	Timer B0 mode register	TB0MR	00XX 0000$_2$
035C$_{16}$	Timer B1 mode register	TB1MR	00XX 0000$_2$
035D$_{16}$	Timer B2 mode register	TB2MR	00XX 0000$_2$
035E$_{16}$	Timer B2 special mode register	TB2SC	XXXX XXX0$_2$
035F$_{16}$	Count source prescaler register	TCSPR	0XXX 0000$_2$
0360$_{16}$			
0361$_{16}$			
0362$_{16}$			
0363$_{16}$			
0364$_{16}$	UART0 special mode register 4	U0SMR4	00$_{16}$
0365$_{16}$	UART0 special mode register 3	U0SMR3	00$_{16}$
0366$_{16}$	UART0 special mode register 2	U0SMR2	00$_{16}$
0367$_{16}$	UART0 special mode register	U0SMR	00$_{16}$
0368$_{16}$	UART0 transmit/receive mode register	U0MR	00$_{16}$
0369$_{16}$	UART0 baud rate register	U0BRG	XX$_{16}$
036A$_{16}$ 036B$_{16}$	UART0 transmit buffer register	U0TB	XX$_{16}$ XX$_{16}$
036C$_{16}$	UART0 transmit/receive control register 0	U0C0	0000 1000$_2$
036D$_{16}$	UART0 transmit/receive control register 1	U0C1	0000 0010$_2$
036E$_{16}$ 036F$_{16}$	UART0 receive buffer register	U0RB	XX$_{16}$ XX$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
037016			
037116			
037216			
037316			
037416			
037516			
037616			
037716			
037816	DMA0 cause select register	DM0SL	0X00 00002
037916	DMA1 cause select register	DM1SL	0X00 00002
037A16	DMA2 cause select register	DM2SL	0X00 00002
037B16	DMA3 cause select register	DM3SL	0X00 00002
037C16 037D16	CRC data register	CRCD	XX16 XX16
037E16	CRC input register	CRCIN	XX16
037F16			
038016 038116	A-D0 register 0	AD00	XXXX XXXX2 0000 00002
038216 038316	A-D0 register 1	AD01	XX16 XX16
038416 038516	A-D0 register 2	AD02	XX16 XX16
038616 038716	A-D0 register 3	AD03	XX16 XX16
038816 038916	A-D0 register 4	AD04	XX16 XX16
038A16 038B16	A-D0 register 5	AD05	XX16 XX16
038C16 038D16	A-D0 register 6	AD06	XX16 XX16
038E16 038F16	A-D0 register 7	AD07	XX16 XX16
039016			
039116			
039216	A-D0 control register 4	AD0CON4	XXXX 00XX2
039316			
039416	A-D0 control register 2	AD0CON2	XX0X X0002
039516	A-D0 control register 3	AD0CON3	XXXX X0002
039616	A-D0 control register 0	AD0CON0	0016
039716	A-D0 control register 1	AD0CON1	0016
039816	D-A register 0	DA0	XX16
039916			
039A16	D-A register 1	DA1	XX16
039B16			
039C16	D-A control register	DACON	XXXX XX002
039D16			
039E16			
039F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03A0$_{16}$	Function select register A8	PS8	X000 0000$_2$
03A1$_{16}$	Function select register A9	PS9	00$_{16}$
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function select register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$	Function select register C2	PSC2	XXXX X00X$_2$
03AD$_{16}$	Function select register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function select register C	PSC	00X0 0000$_2$
03B0$_{16}$	Function select register A0	PS0	00$_{16}$
03B1$_{16}$	Function select register A1	PS1	00$_{16}$
03B2$_{16}$	Function select register B0	PSL0	00$_{16}$
03B3$_{16}$	Function select register B1	PSL1	00$_{16}$
03B4$_{16}$	Function select register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function select register A3	PS3	00$_{16}$
03B6$_{16}$	Function select register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function select register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$	Function select register A5	PS5	XXX0 0000$_2$
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 register	P6	XX$_{16}$
03C1$_{16}$	Port P7 register	P7	XX$_{16}$
03C2$_{16}$	Port P6 direction register	PD6	00$_{16}$
03C3$_{16}$	Port P7 direction register	PD7	00$_{16}$
03C4$_{16}$	Port P8 register	P8	XX$_{16}$
03C5$_{16}$	Port P9 register	P9	XX$_{16}$
03C6$_{16}$	Port P8 direction register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 direction register	PD9	00$_{16}$
03C8$_{16}$	Port P10 register	P10	XX$_{16}$
03C9$_{16}$	Port P11 register	P11	XX$_{16}$
03CA$_{16}$	Port P10 direction register	PD10	00$_{16}$
03CB$_{16}$	Port P11 direction register	PD11	XXX0 0000$_2$
03CC$_{16}$	Port P12 register	P12	XX$_{16}$
03CD$_{16}$	Port P13 register	P13	XX$_{16}$
03CE$_{16}$	Port P12 direction register	PD12	00$_{16}$
03CF$_{16}$	Port P13 direction register	PD13	00$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03D0$_{16}$	Port P14 register	P14	XX$_{16}$
03D1$_{16}$	Port P15 register	P15	XX$_{16}$
03D2$_{16}$	Port P14 direction register	PD14	X000 0000$_2$
03D3$_{16}$	Port P15 direction register	PD15	00$_{16}$
03D4$_{16}$			
03D5$_{16}$			
03D6$_{16}$			
03D7$_{16}$			
03D8$_{16}$			
03D9$_{16}$			
03DA$_{16}$	Pull-up control register 2	PUR2	00$_{16}$
03DB$_{16}$	Pull-up control register 3	PUR3	00$_{16}$
03DC$_{16}$	Pull-up control register 4	PUR4	XXXX 0000$_2$
03DD$_{16}$			
03DE$_{16}$			
03DF$_{16}$			
03E0$_{16}$	Port P0 register	P0	XX$_{16}$
03E1$_{16}$	Port P1 register	P1	XX$_{16}$
03E2$_{16}$	Port P0 direction register	PD0	00$_{16}$
03E3$_{16}$	Port P1 direction register	PD1	00$_{16}$
03E4$_{16}$	Port P2 register	P2	XX$_{16}$
03E5$_{16}$	Port P3 register	P3	XX$_{16}$
03E6$_{16}$	Port P2 direction register	PD2	00$_{16}$
03E7$_{16}$	Port P3 direction register	PD3	00$_{16}$
03E8$_{16}$	Port P4 register	P4	XX$_{16}$
03E9$_{16}$	Port P5 register	P5	XX$_{16}$
03EA$_{16}$	Port P4 direction register	PD4	00$_{16}$
03EB$_{16}$	Port P5 direction register	PD5	00$_{16}$
03EC$_{16}$			
03ED$_{16}$			
03EE$_{16}$			
03EF$_{16}$			
03F0$_{16}$	Pull-up control register 0	PUR0	00$_{16}$
03F1$_{16}$	Pull-up control register 1	PUR1	XXXX 0000$_2$
03F2$_{16}$			
03F3$_{16}$			
03F4$_{16}$			
03F5$_{16}$			
03F6$_{16}$			
03F7$_{16}$			
03F8$_{16}$			
03F9$_{16}$			
03FA$_{16}$			
03FB$_{16}$			
03FC$_{16}$			
03FD$_{16}$			
03FE$_{16}$			
03FF$_{16}$	Port control register	PCR	XXXX XXX0$_2$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin package>

Address	Register	Symbol	Value after RESET
03A0$_{16}$			
03A1$_{16}$			
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function select register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$	Function select register C2	PSC2	XXXX X00X$_2$
03AD$_{16}$	Function select register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function select register C	PSC	0X00 0000$_2$
03B0$_{16}$	Function select register A0	PS0	00$_{16}$
03B1$_{16}$	Function select register A1	PS1	00$_{16}$
03B2$_{16}$	Function select register B0	PSL0	00$_{16}$
03B3$_{16}$	Function select register B1	PSL1	00$_{16}$
03B4$_{16}$	Function select register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function select register A3	PS3	00$_{16}$
03B6$_{16}$	Function select register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function select register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$			
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 register	P6	XX$_{16}$
03C1$_{16}$	Port P7 register	P7	XX$_{16}$
03C2$_{16}$	Port P6 direction register	PD6	00$_{16}$
03C3$_{16}$	Port P7 direction register	PD7	00$_{16}$
03C4$_{16}$	Port P8 register	P8	XX$_{16}$
03C5$_{16}$	Port P9 register	P9	XX$_{16}$
03C6$_{16}$	Port P8 direction register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 direction register	PD9	00$_{16}$
03C8$_{16}$	Port P10 register	P10	XX$_{16}$
03C9$_{16}$			
03CA$_{16}$	Port P10 direction register	PD10	00$_{16}$
03CB$_{16}$	Set default value to "FF$_{16}$"		
03CC$_{16}$			
03CD$_{16}$			
03CE$_{16}$	Set default value to "FF$_{16}$"		
03CF$_{16}$	Set default value to "FF$_{16}$"		

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin package>

Address	Register	Symbol	Value after RESET
03D0$_{16}$			
03D1$_{16}$			
03D2$_{16}$	Set default value to "FF$_{16}$"		
03D3$_{16}$	Set default value to "FF$_{16}$"		
03D4$_{16}$			
03D5$_{16}$			
03D6$_{16}$			
03D7$_{16}$			
03D8$_{16}$			
03D9$_{16}$			
03DA$_{16}$	Pull-up control register 2	PUR2	00$_{16}$
03DB$_{16}$	Pull-up control register 3	PUR3	00$_{16}$
03DC$_{16}$	Set default value to "00$_{16}$"		
03DD$_{16}$			
03DE$_{16}$			
03DF$_{16}$			
03E0$_{16}$	Port P0 register	P0	XX$_{16}$
03E1$_{16}$	Port P1 register	P1	XX$_{16}$
03E2$_{16}$	Port P0 direction register	PD0	00$_{16}$
03E3$_{16}$	Port P1 direction register	PD1	00$_{16}$
03E4$_{16}$	Port P2 register	P2	XX$_{16}$
03E5$_{16}$	Port P3 register	P3	XX$_{16}$
03E6$_{16}$	Port P2 direction register	PD2	00$_{16}$
03E7$_{16}$	Port P3 direction register	PD3	00$_{16}$
03E8$_{16}$	Port P4 register	P4	XX$_{16}$
03E9$_{16}$	Port P5 register	P5	XX$_{16}$
03EA$_{16}$	Port P4 direction register	PD4	00$_{16}$
03EB$_{16}$	Port P5 direction register	PD5	00$_{16}$
03EC$_{16}$			
03ED$_{16}$			
03EE$_{16}$			
03EF$_{16}$			
03F0$_{16}$	Pull-up control register 0	PUR0	00$_{16}$
03F1$_{16}$	Pull-up control register 1	PUR1	XXXX 0000$_2$
03F2$_{16}$			
03F3$_{16}$			
03F4$_{16}$			
03F5$_{16}$			
03F6$_{16}$			
03F7$_{16}$			
03F8$_{16}$			
03F9$_{16}$			
03FA$_{16}$			
03FB$_{16}$			
03FC$_{16}$			
03FD$_{16}$			
03FE$_{16}$			
03FF$_{16}$	Port control register	PCR	XXXX XXX0$_2$

X: Indeterminate

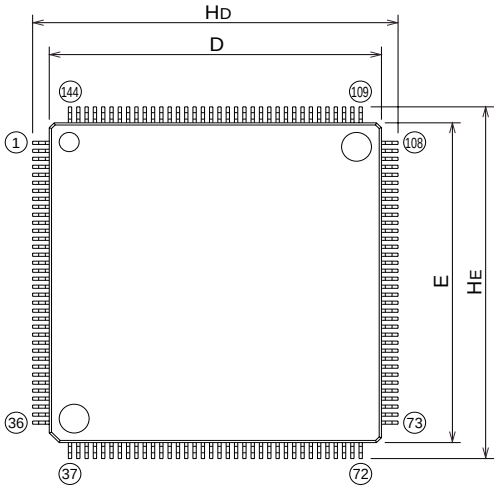
Blank spaces are reserved. No access is allowed.

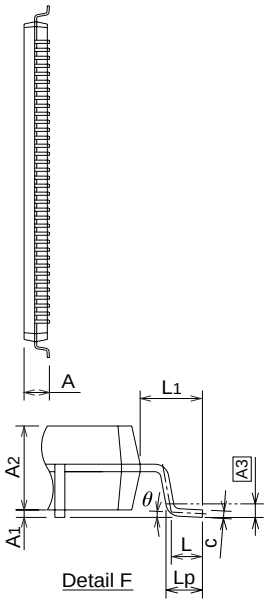
Package Dimensions

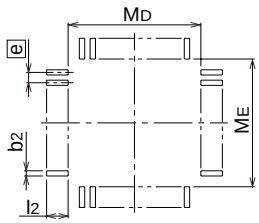
144P6Q-A

Plastic 144pin 20×20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP144-P-2020-0.50	–	1.23	Cu Alloy







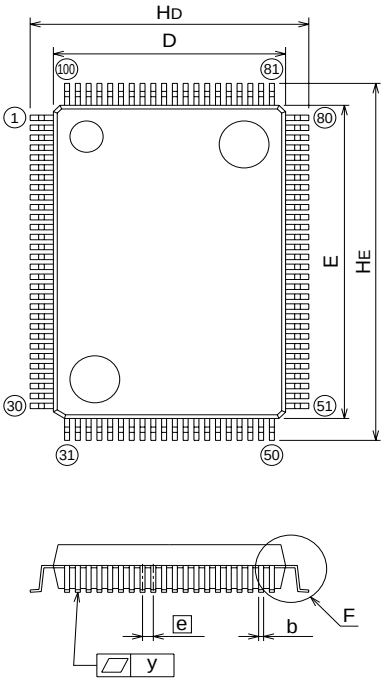
Recommended Mount Pad

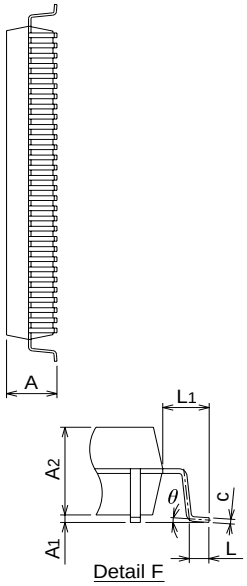
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0.05	0.125	0.2
A2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	–	0.5	–
HD	21.8	22.0	22.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
I2	0.95	–	–
MD	–	20.4	–
ME	–	20.4	–

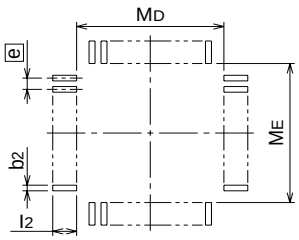
100P6S-A

Plastic 100pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	–	1.58	Alloy 42







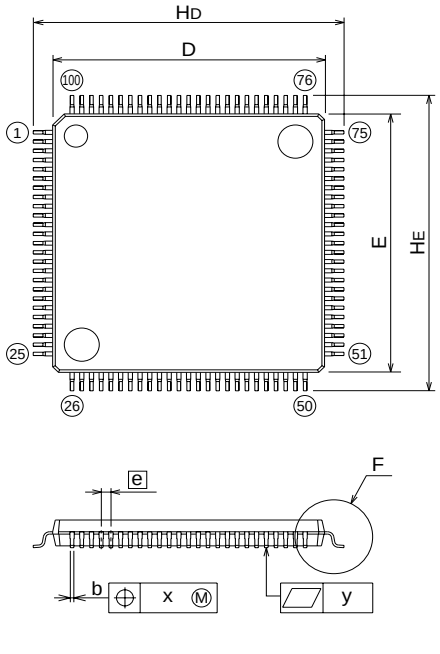
Recommended Mount Pad

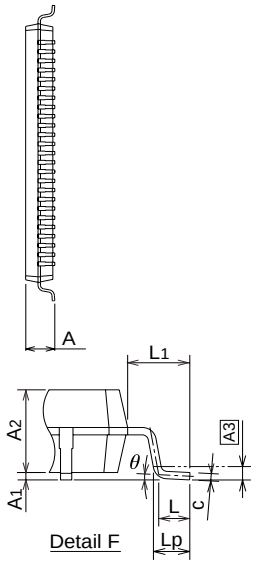
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	–	1.4	–
y	–	–	0.1
θ	0°	–	10°
b2	–	0.35	–
I2	1.3	–	–
MD	–	14.6	–
ME	–	20.6	–

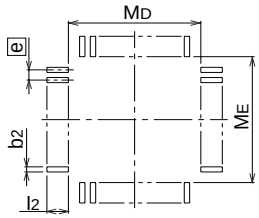
100P6Q-A (MMP)

Plastic 100pin 14×14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	–	0.63	Cu Alloy







Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.5	–
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
L	0.3	0.5	0.7
L_1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.225	–
l_2	0.9	–	–
M_D	–	14.4	–
M_E	–	14.4	–

REVISION HISTORY	M32C/85 Group Short Sheet/Data Sheet

Rev.	Date	Description	
		Page	Summary
0.30	18/07/2003	–	New document
0.40	30/09/2003		Overview
		2 to 3	- “Oscillator stop detect function” has been added to Tables 1.1 and 1.2
		5	- M30852ME-XXXGP and M30850ME-XXXGP/FP have been deleted in Figure 1.2 and Table 1.3.
		6	- “192K bytes” has been deleted from ROM capacity.
		7	- Note 2 has been added to Figures 1.4 to 1.6
		10,14	- V_{REF} pin has been changed from analog input pins to control pins.
		16 to 18	- SDA0 to SDA4 pins have been changed from output pins to I/O pins.
		17	- $TA4_{OUT}$ pin has been changed from input pin to I/O pin.
			- $TA4_{IN}$ pin has been changed from output pin to input pin.
			- ISRxD1 pin has been modified to ISRxD0 pin in port P8.
		18	- DA0 and DA1 pins have been changed from Output pins to input pins.
		19	- Symbol “$P11_7$” has been modified to “$P11_4$” and description from “8-bit” to “5-bit”.
			- Descriptions of ISTxD1 and $BE1_{IN}$ have been modified from “received data” to “transmit data”.
			SFR
		44,45	- Notes are written directly in the Tables.

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