

1. Overview

The M32C/86 is a single-chip microcomputer that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/86 group is available in 144-pin plastic molded QFP/LQFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It incorporates a multiplier and DMAC adequate for office automation, communication devices and industrial equipments and other high-speed processing applications.

1.1 Applications

Audio, cameras, office equipment, communications equipment, portable equipment, etc.

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error.

Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Outline

Table 1.1 lists performance outlines of the M32C/86 group.

Table 1.1 M32C/86 Group Performance

Item		Performance
CPU	Basic instructions	108 instructions
	Shortest instruction execution time	31.3 ns (f(BCLK)=32 MHz, VCC1=4.2 V to 5.5 V) 50 ns (f(BCLK)=20 MHz, VCC1=3.0 V to 5.5 V)
	Operation mode	Single-chip, memory expansion and microprocessor modes
	Address space	16 Mbytes
	Memory capacity	See Table 1.2
Peripheral function	Port	123 I/O pins and 1 input pin
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function or waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing) Stepping motor control circuit
	Serial I/O	5 channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus ⁽¹⁾ , I ² C bus ⁽²⁾
	CAN module	2 channels Supporting CAN 2.0B specification
	A-D converter	10-bit A-D converter: 1 circuit, 34 channels
	D-A converter	8-bit x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt factors Immediate transfer, calculation transfer and chain transfer functions
	CRC calculation circuit	CRC-CCITT
	X-Y converter	16 bits X 16 bits
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	39 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock generating circuit	4 circuits Main clock generating circuit(*), sub clock generating circuit(*), ring oscillator, PLL frequency synthesizer (*)Generating circuits include an internal feedback resistor and external ceramic resonator/crystal oscillator.
	Oscillator stop detect function	Main clock oscillator stop detect function
	Supply voltage detect circuit	Available (option)
Electric characteristics	Supply voltage	VCC1=4.2 V to 5.5 V, VCC2=3.0 V to VCC1 (f(BCLK)=32 MHz) VCC1=3.0 V to 5.5 V, VCC2=3.0 V to VCC1 (f(BCLK)=20 MHz)
	Power consumption	38 mA (VCC1=VCC2=5 V, f(BCLK)=32 MHz) 26 mA (VCC1=VCC2=3.3 V, f(BCLK)=20 MHz) TBD (VCC1=VCC2=3.3 V, f(XCIN)=32 kHz, wait mode)
Flash memory	Program/erase supply voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V
	Program and erase endurance	100 times
Operating ambient temperature		-20 to 85°C, -40 to 85°C (option)
Package		144-pin plastic mold QFP

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
 2. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
- All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/86 group microcomputer.

The M32C/86 group microcomputer contains ROM and RAM as memory to store instructions and data, CPU to execute calculations and peripheral functions such as interrupt, timer, serial I/O, DMAC, CRC calculation circuit, A-D converter, D-A converter, intelligent I/O and ports.

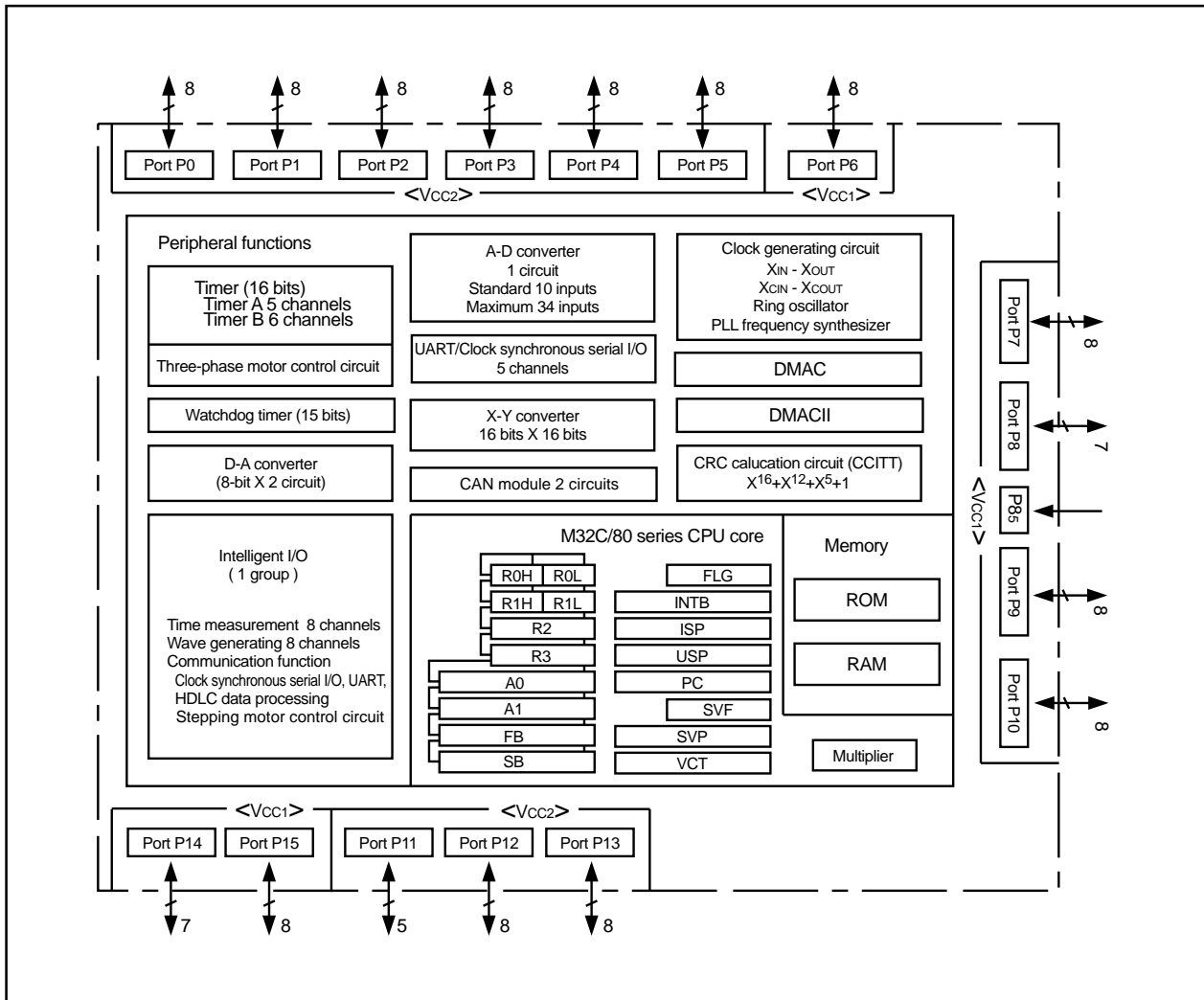


Figure 1.1 M32C/86 Group Block Diagram

1.4 Product Information

Renesas plans to release the following products in the M32C/86 group:

- (1) Support for the flash memory version
- (2) ROM/RAM capacity
- (3) Package

144P6Q-A : Plastic molded QFP

Table 1.2 M32C/86 Group

As of September, 2003

Type number	ROM capacity	RAM capacity	Package type	Remarks
M30865FJGP (D)	512K ⁽¹⁾	24K	144P6Q-A	Flash Memory

(D): Under development

NOTES:

- 1. Another 4-Kbyte space is provided to store data.

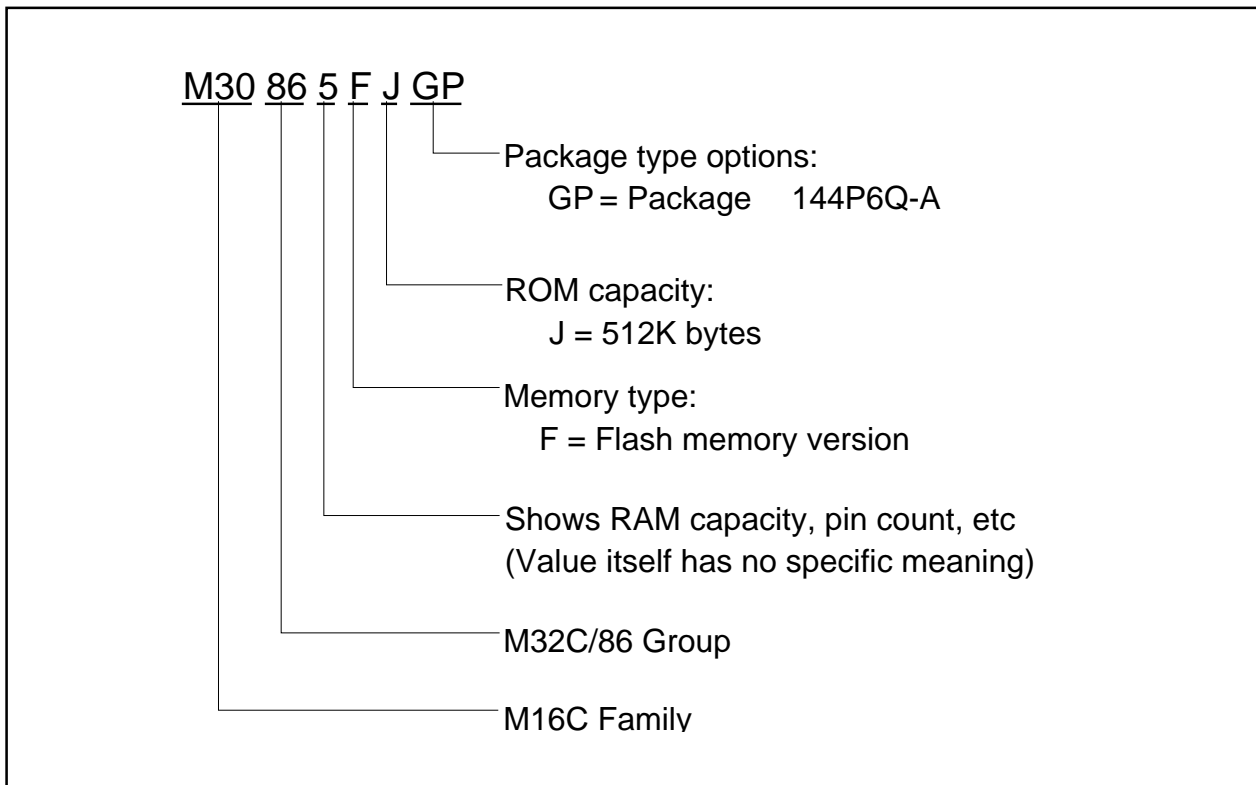


Figure 1.2 Product Numbering System

1.5 Pin Assignments and Descriptions

Figure 1.3 shows pin assignments (top view).

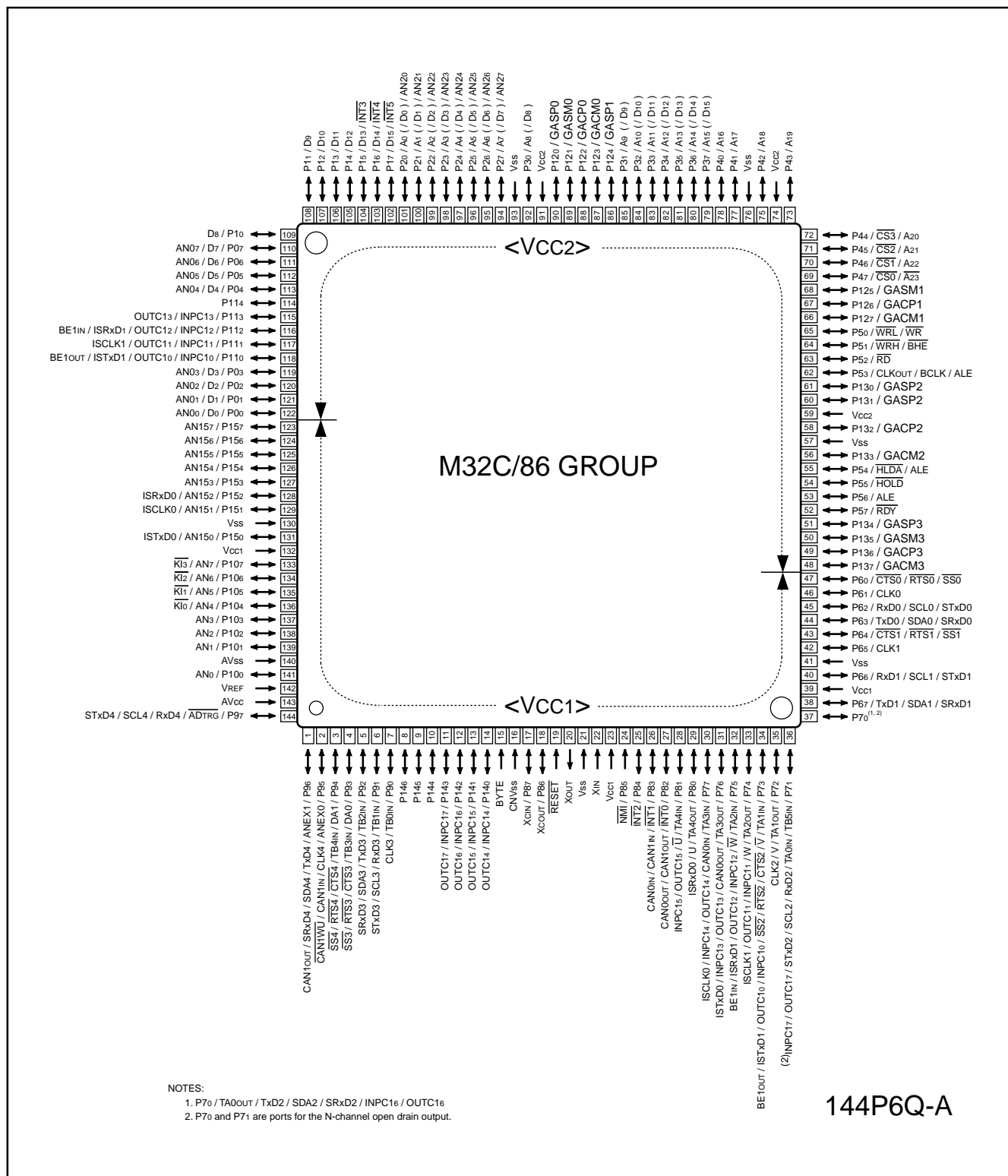


Figure 1.3 Pin Assignment

Table 1.3 Pin Characteristics

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
1		P96			TxD4/SDA4/SRxD4/CAN1out		ANEX1	
2		P95			CLK4/CAN1in/CAN1WU		ANEX0	
3		P94		TB4IN	CTS4/RTS4/SS4		DA1	
4		P93		TB3IN	CTS3/RTS3/SS3		DA0	
5		P92		TB2IN	TxD3/SDA3/SRxD3			
6		P91		TB1IN	RxD3/SCL3/STxD3			
7		P90		TB0IN	CLK3			
8		P146						
9		P145						
10		P144						
11		P143				INPC17/OUTC17		
12		P142				INPC16/OUTC16		
13		P141				INPC15/OUTC15		
14		P140				INPC14/OUTC14		
15	BYTE							
16	CNVSS							
17	X _{CIN}	P87						
18	X _{COU}	P86						
19	RESET							
20	X _{OUT}							
21	V _{SS}							
22	X _{IN}							
23	V _{CC1}							
24		P85	NMI					
25		P84	INT2					
26		P83	INT1		CAN0in/CAN1in			
27		P82	INT0		CAN0out/CAN1out			
28		P81		TA4in/U		INPC15/OUTC15		
29		P80		TA4out/U		ISRxD0		
30		P77		TA3in	CAN0in	INPC14/OUTC14/ISCLK0		
31		P76		TA3out	CAN0out	INPC13/OUTC13/ISTxD0		
32		P75		TA2in/W		INPC12/OUTC12/ISRxD1/BE1in		
33		P74		TA2out/W		INPC11/OUTC11/ISCLK1		
34		P73		TA1in/V	CTS2/RTS2/SS2	INPC10/OUTC10/ISTxD1/BE1out		
35		P72		TA1out/V	CLK2			
36		P71		TB5in/TA0in	RxD2/SCL2/STxD2	INPC17/OUTC17		
37		P70		TA0out	TxD2/SDA2/SRxD2	INPC16/OUTC16		
38		P67			TxD1/SDA1/SRxD1			
39	V _{CC1}							
40		P66			RxD1/SCL1/STxD1			
41	V _{SS}							
42		P65			CLK1			
43		P64			CTS1/RTS1/SS1			
44		P63			TxD0/SDA0/SRxD0			
45		P62			RxD0/SCL0/STxD0			
46		P61			CLK0			
47		P60			CTS0/RTS0/SS0			
48		P137				GACM3		

Table 1.3 Pin Characteristics (Continued)

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
49		P136				GACP3		
50		P135				GASM3		
51		P134				GASP3		
52		P57						RDY
53		P56						ALE
54		P55						HOLD
55		P54						HLDA/ALE
56		P133				GACM2		
57	Vss							
58		P132				GACP2		
59	Vcc2							
60		P131				GASM2		
61		P130				GASP2		
62		P53						CLKOUT/BCLK/ALE
63		P52						RD
64		P51						WRH/BHE
65		P50						WRL/WR
66		P127				GACM1		
67		P126				GACP1		
68		P125				GASM1		
69		P47						CS0/A23
70		P46						CS1/A22
71		P45						CS2/A21
72		P44						CS3/A20
73		P43						A19
74	Vcc2							
75		P42						A18
76	Vss							
77		P41						A17
78		P40						A16
79		P37						A15(/D15)
80		P36						A14(/D14)
81		P35						A13(/D13)
82		P34						A12(/D12)
83		P33						A11(/D11)
84		P32						A10(/D10)
85		P31						A9(/D9)
86		P124				GASP1		
87		P123				GACM0		
88		P122				GACP0		
89		P121				GASM0		
90		P120				GASP0		
91	Vcc2							
92		P30						A8(/D8)
93	Vss							
94		P27					AN27	A7(/D7)
95		P26					AN26	A6(/D6)
96		P25					AN25	A5(/D5)

Table 1.3 Pin Characteristics (Continued)

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
97		P24					AN24	A4(/D4)
98		P23					AN23	A3(/D3)
99		P22					AN22	A2(/D2)
100		P21					AN21	A1(/D1)
101		P20					AN20	A0(/D0)
102		P17	$\overline{\text{INT5}}$					D15
103		P16	$\overline{\text{INT4}}$					D14
104		P15	$\overline{\text{INT3}}$					D13
105		P14						D12
106		P13						D11
107		P12						D10
108		P11						D9
109		P10						D8
110		P07					AN07	D7
111		P06					AN06	D6
112		P05					AN05	D5
113		P04					AN04	D4
114		P114						
115		P113				INPC13/OUTC13		
116		P112				INPC12/OUTC12/ISRxD1/BE1IN		
117		P111				INPC11/OUTC11/ISCLK1		
118		P110				INPC10/OUTC10/ISTxD1/BE1OUT		
119		P03					AN03	D3
120		P02					AN02	D2
121		P01					AN01	D1
122		P00					AN00	D0
123		P157					AN157	
124		P156					AN156	
125		P155					AN155	
126		P154					AN154	
127		P153					AN153	
128		P152				ISRxD0	AN152	
129		P151				ISCLK0	AN151	
130	Vss							
131		P150				ISTxD0	AN150	
132	Vcc1							
133		P107	$\overline{\text{KI3}}$				AN7	
134		P106	$\overline{\text{KI2}}$				AN6	
135		P105	$\overline{\text{KI1}}$				AN5	
136		P104	$\overline{\text{KI0}}$				AN4	
137		P103					AN3	
138		P102					AN2	
139		P101					AN1	
140	AVss							
141		P100					AN0	
142	VREF							
143	AVcc							
144		P97			RxD4/SCL4/STxD4		$\overline{\text{ADTRG}}$	

1.6 Pin Description

Table 1.4 Pin Description

Symbol	Function	I/O type	Supply voltage	Description
VCC1, VCC2 VSS	Power supply input	I I	— —	Apply 3.0 to 5.5V to both VCC1 and VCC2 pins. Apply 0V to the VSS pin. VCC1 ≥ VCC2 ⁽¹⁾
CNVSS	CNVSS	I	VCC1	Switches processor mode. Connect this pin to VSS to start up in single-chip mode (memory expansion mode). Connect this pin to VCC to start up in microprocessor mode.
RESET	Reset input	I	VCC1	The microcomputer is in a reset state when applying "L" to the RESET pin.
XIN XOUT	Clock input Clock output	I O	VCC1	I/O pins for the main clock generating circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To use an external clock, input the clock to XIN and leave XOUT open.
BYTE	Input to switch external data bus width	I	VCC1	Switches the data bus in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when the BYTE pin is held "H". Set to either. Connect this pin to VSS when an external bus is not used.
AVCC	Analog power supply input	I	—	Applies power supply for the A-D converter and D-A converter. Connect this pin to VCC1.
AVSS	Analog power supply input	I	—	Applies power supply for the A-D converter and D-A converter. Connect this pin to VSS.
VREF	Reference voltage input	I	—	Applies reference voltage for the A-D converter.
P0 ₀ to P0 ₇	I/O port P0	I/O	VCC2	8-bit I/O ports in CMOS having a direction register to select input or output. Each pin is set as an input port or output port. An input port in single-chip mode can be set for a pull-up or for no pull-up in 4-bit unit by program. When these pins are used as bus control pins in memory expansion mode and microprocessor mode, internal pull-up resistor cannot be selected. Ports used as input ports can be set for a pull-up or for no pull-up in the modes above.
D0 to D7	Data bus	I/O		Inputs and outputs data (D0 to D7) when these pins are set as the separate bus.
AN0 ₀ to AN0 ₇	Analog input pin	I		Analog input pins for the A-D converter
P1 ₀ to P1 ₇	I/O port P1	I/O	VCC2	8-bit I/O ports having equivalent functions to P0
INT3 to INT5	INT interrupt input pin	I		Input pins for the INT interrupt
D8 to D15	Data bus	I/O		Inputs and outputs data (D8 to D15) when these pins are set as the separate bus.
P2 ₀ to P2 ₇	I/O port P2	I/O	VCC2	8-bit I/O ports having equivalent functions to P0
A0 to A7	Address bus	O		Outputs 8 low-order address bits (A0 to A7).
A0/D0 to A7/D7	Address bus/data bus	I/O		Inputs and outputs data (D0 to D7) and outputs 8 low-order address bits (A0 to A7) by time-sharing when these pins are set as the multiplexed bus.
AN2 ₀ to AN2 ₇	Analog input pin	I		Analog input pins for A-D converter
P3 ₀ to P3 ₇	I/O port P3	I/O	VCC2	8-bit I/O ports having equivalent functions to P0
A8 to A15	Address bus	O		Outputs 8 middle-order address bits (A8 to A15).
A8/D8 to A15/D15	Address bus/data bus	I/O		Inputs and outputs data (D8 to D15) and outputs 8 middle-order address bits (A8 to A15) by time-sharing when external 16-bit data bus is set as the multiplexed bus.
P4 ₀ to P4 ₇	I/O port P4	I/O	VCC2	8-bit I/O ports having equivalent functions to P0
A16 to A22, A23	Address bus	O		Outputs 8 high-order address bits (A16 to A22, A23). The highest-order bit (A23) inverted is also output.
CS0 to CS3	Chip-select	O		Output CS0 to CS3 signals. CS0 to CS3 are chip-select signals specifying an external space.

I : Input O : Output I/O : Input and output

NOTES:

1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.

Table 1.4 Pin Description (Continued)

Symbol	Function	I/O type	Supply voltage	Description
P50 to P57	I/O port P5	I/O	VCC2	8-bit I/O ports having equivalent functions to P0
CLKOUT	Clock output	O		Outputs the main clock divided by 8 or divided by 32 or the clock having the same frequency as the sub clock from P53.
WRL	Bus control pin	O		Output WRL, WRH, (WR, BHE), RD, BCLK, HLDA and ALE signals. WRL and WRH or BHE and WR can be switched by program. ■ WRL, WRH and RD are selected The WRL signal becomes "L" by writing data to an even address in an external memory space. The WRH signal becomes "L" by writing data to an odd address in an external memory space. The RD pin signal becomes "L" by reading data in an external memory space. ■ WR, BHE and RD are selected The WR signal becomes "L" by writing data to an external memory space. The RD signal becomes "L" by reading data in an external memory space. The BHE signal becomes "L" by accessing an odd address. Select WR, BHE and RD for an external 8-bit data bus. While the HOLD pin is held "L", the microcomputer is placed in a hold state. In a hold state, HLDA outputs a "L" signal. ALE is a signal latching the address. While the RDY pin is held "L", the microcomputer is placed in a wait state.
WR		O		
WRH		O		
BHE		O		
RD		O		
BCLK		O		
HLDA		O		
HOLD		I		
ALE		O		
RDY		I		
P60 to P67		I/O port P6	I/O	
CTS0, CTS1	UART pin	I		I/O pins for UART0 (P60 to P63) and UART1 (P64 to P67)
RTS0, RTS1		O		
SS0, SS1		I		
CLK0, CLK1		I/O		
RxD0, RxD1		I		
SCL0, SCL1		I/O		
STxD0, STxD1		O		
TxD0, TxD1		O		
SDA0, SDA1		I/O		
SRxD0, SRxD1		I		

I : Input O : Output I/O : Input and output

Table 1.4 Pin Description (Continued)

Symbol	Function	I/O type	Supply voltage	Description							
P70 to P77	I/O port P7	I/O	VCC1	8-bit I/O ports having equivalent functions to P0 (P70 and P71 are ports for the N-channel open drain output.)							
TA0OUT to TA3OUT TA0IN to TA3IN	Timer A pin	I/O I		I/O pins for timers A0 to A3							
TB5IN	Timer B pin	I		Input pin for timer B5							
V, \bar{V}	Three-phase motor control output pin	O		V-phase output pin							
W, \bar{W}		O		W-phase output pin							
CTS2 RTS2 SS2 CLK2 RxD2 SCL2 STxD2 TxD2 SDA2 SRxD2	UART pin	I O I I I I/O O O I/O I		I/O pins for UART2							
INPC10 to INPC14 INPC16, INPC17 OUTC10 to OUTC14 OUTC16, OUTC17 ISCLK0, ISCLK1 ISTxD0, ISTxD1 ISRxD1 BE1OUT BE1IN		Intelligent I/O pin	I O I/O O I O I		INPC10 to INPC14, INPC16 and INPC17 are input pins for the time measurement function. OUTC10 to OUTC14, OUTC16 and OUTC17 are output pins for the waveform generating function. ISCLK0 and ISCLK1 input and output the clock for the intelligent I/O communication function. ISRxD1 and BE1IN input received data for the intelligent I/O communication function. ISTxD0 and ISTxD1 and BE1OUT output transmit data for the intelligent I/O communication function.						
CAN0OUT CAN0IN				CAN pin	O I		I/O pins for the CAN communication function				
P80 to P84, P86, P87						I/O port P8	I/O	VCC1	I/O ports having equivalent functions to P0		
XcIN XcOUT				Sub clock	I O					I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XcIN and XcOUT.	
TA4OUT TA4IN									Timer A pin	I/O I	
U, \bar{U}				Three-phase motor control output pin	O						
INT0 to INT2									INT interrupt input pin	I	
INPC15 OUTC15 ISRxD0				Intelligent I/O pin	I O I						
CAN0OUT, CAN1OUT CAN0IN, CAN1IN									CAN pin	O I	
P85/NMI	NMI interrupt input pin										I

I : Input O : Output I/O : Input and output

Table 1.4 Pin Description (Continued)

Symbol	Function	I/O type	Supply voltage	Description		
P90 to P97	I/O port P9	I/O	VCC1	8-bit I/O ports having equivalent functions P0. The PRCR register prevents PD9 and PS3 registers from rewriting.		
TB0IN to TB4IN	Timer B pin	I		Input pins for timers B0 to B4		
CTS3, CTS4	UART pin	I		I/O pins for UART3 (P90 to P93) and UART4 (P94 to P97)		
RTS3, RTS4		O				
SS3, SS4		I				
CLK3, CLK4		I/O				
RxD3, RxD4		I				
SCL3, SCL4		I/O				
STxD3, STxD4		O				
TxD3, TxD4		O				
SDA3, SDA4		I/O				
SRxD3, SRxD4		I				
DA0, DA1		D-A output pin	O			Output pins for the D-A converter
ANEX0,		A-D related pin	I/O			ANEX0 is an extended analog I/O pin for the A-D converter.
ANEX1,	I			ANEX1 is an extended analog input pin for the A-D converter.		
ADTRG	I			ADTRG is an A-D trigger input pin.		
CAN1WU	CAN1 interrupt input pin	I		Input pin for the CAN1 wake-up interrupt.		
CAN1OUT, CAN1IN	CAN pin	O		Input pins for the CAN communication function		
		I				
P100 to P107	I/O port P10	I/O	VCC1	8-bit I/O ports having equivalent functions to P0		
KI0 to KI3	Key input interrupt pin	I		Input pins for the key input interrupt		
AN0 to AN7	Analog input pin	I		Analog input pins for the A-D converter		

I : Input O : Output I/O : Input and output

Table 1.4 Pin Description (Continued)

Symbol	Function	I/O type	Supply voltage	Description
P11 ₀ to P11 ₄	I/O port P11	I/O	VCC2	5-bit I/O ports having equivalent functions to P0.
INPC ₁₀ to INPC ₁₃	Intelligent I/O pin	I	VCC2	INPC ₁₀ to INPC ₁₃ are input pins for the time measurement function.
OUTC ₁₀ to OUTC ₁₃		O		OUTC ₁₀ to OUTC ₁₃ are output pins for the waveform generating function.
ISCLK1		I/O		ISCLK1 inputs and outputs the clock and is an I/O pin for the intelligent I/O communication function.
ISTxD1		O		ISTxD1 and BE1IN input received data for the intelligent I/O communication function.
ISRxD1		I		ISRxD1 and BE1IN input received data for the intelligent I/O communication function.
BE1OUT		O		ISTxD1 and BE1OUT output transmit data for the intelligent I/O communication function.
BE1IN		I		ISTxD1 and BE1OUT output transmit data for the intelligent I/O communication function.
P12 ₀ to P12 ₇	I/O port P12	I/O	VCC1	8-bit I/O ports having equivalent functions to P0
GASP ₀ , GASP ₁	Intelligent I/O pin	O	VCC1	GASP ₀ , GASP ₁ , GASM ₀ , GASM ₁ , GACP ₀ , GACP ₁ , GACM ₀ and GACM ₁ are output pins for the stepping motor control.
GASM ₀ , GASM ₁		O		
GACP ₀ , GACP ₁		O		
GACM ₀ , GACM ₁		O		
		O		
P13 ₀ to P13 ₇	I/O port P13	I/O	VCC1	8-bit I/O ports having equivalent functions to P0
GASP ₂ , GASP ₃	Intelligent I/O pin	O	VCC1	GASP ₂ , GASP ₃ , GASM ₂ , GASM ₃ , GACP ₂ , GACP ₃ , GACM ₂ and GACM ₃ are output pins for the stepping motor control.
GASM ₂ , GASM ₃		O		
GACP ₂ , GACP ₃		O		
GACM ₂ , GACM ₃		O		
		O		
P14 ₀ to P14 ₇	I/O port P14	I/O	VCC1	8-bit I/O ports having equivalent functions to P0
INPC ₁₄ to INPC ₁₇	Intelligent I/O pin	I	VCC1	INPC ₁₄ to INPC ₁₇ are input pins for the time measurement function.
OUTC ₁₄ to OUTC ₁₇		O		OUTC ₁₄ to OUTC ₁₇ are output pins for the waveform generating function.
P15 ₀ to P15 ₇	I/O port P15	I/O	VCC1	8-bit I/O ports having equivalent functions to P0
AN ₁₅₀ to AN ₁₅₇	Analog input port	I	VCC1	Analog input pins for the A-D converter
ISCLK0	Intelligent I/O pin	I/O		ISCLK0 inputs and outputs the clock for the intelligent I/O communication function.
ISRxD0		I		ISRxD0 inputs received data for the intelligent I/O communication function.
ISTxD0		O		ISTxD0 outputs transmit data for the intelligent I/O communication function.

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

A register bank comprises 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.

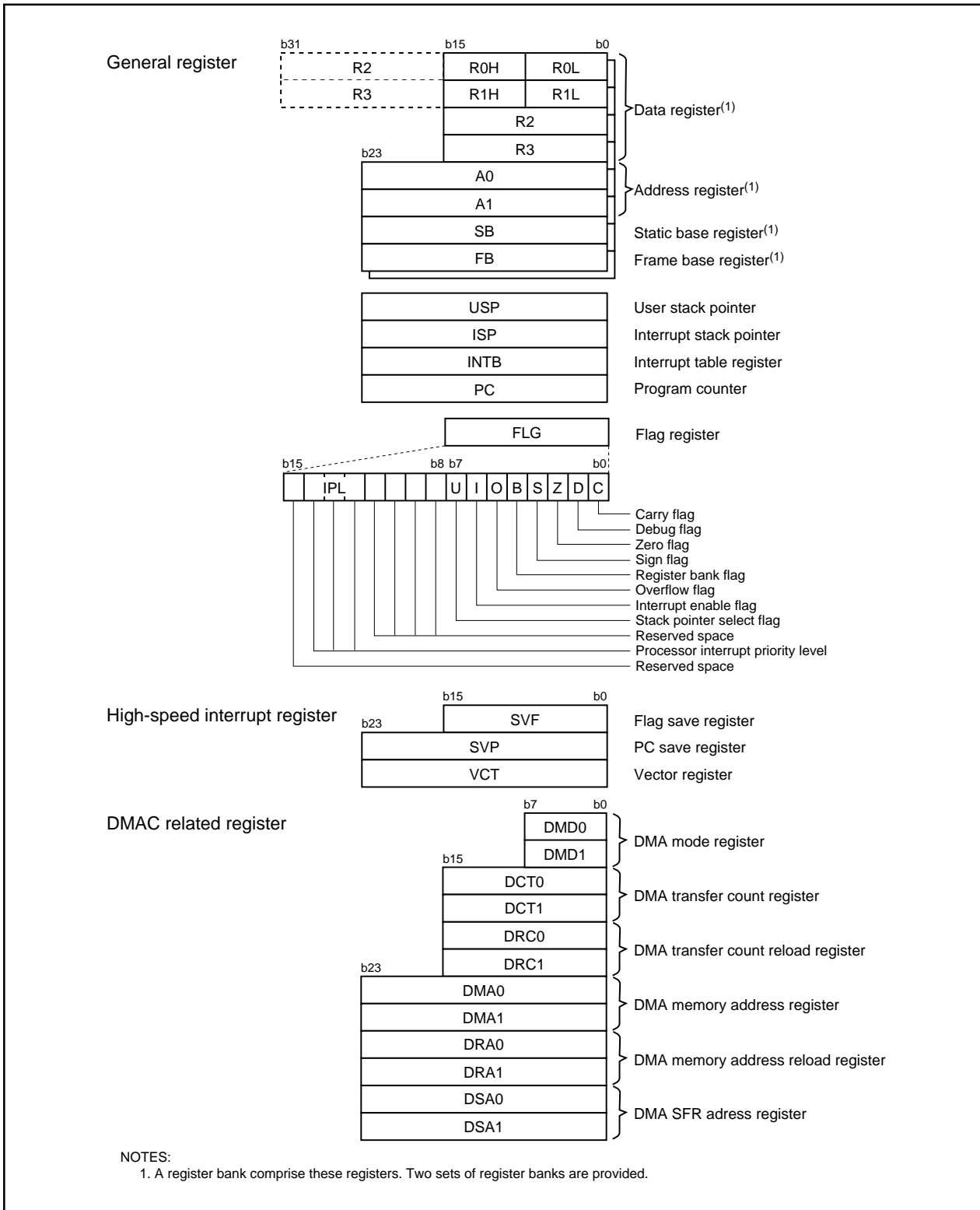


Figure 2.1 CPU Register

2.1 General Register

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R3R1.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC is 24 bits wide. It indicates an address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating a starting address of an interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

USP and ISP as the stack pointer are 24 bits wide. The U flag can switch USP to ISP and vice versa. Refer to "2.1.8 Flag Register (FLG)" about the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow occurs after an instruction is executed.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic calculation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic calculation; otherwise "0".

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when a result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0" and is enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".

The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide. It assigns an interrupt priority levels from level 0 to level 7.

If a requested interrupt has a greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to the reserved space, set to "0". When read, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows.

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-associated Registers

Registers associated with DMAC are as follows.

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/85 group.

The M32C/86 provides 16-Mbyte address space from addresses 000000₁₆ to FFFFFFF₁₆.

The internal ROM is allocated in lower addresses beginning with address FFFFFFF₁₆. For example, a 64-Kbyte internal ROM is allocated in addresses FF0000₁₆ to FFFFFFF₁₆.

The fixed interrupt vectors are allocated in addresses FFFFDC₁₆ to FFFFFFF₁₆. It stores the starting address of each interrupt routine.

The internal RAM is allocated in higher addresses beginning with address 000400₁₆. For example, a 10-Kbyte internal RAM is allocated in addresses 000400₁₆ to 002BFF₁₆. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

The SFR is allocated in addresses 000000₁₆ to 0003FF₁₆. The control registers for peripheral functions such as I/O port, A-D conversion, serial I/O, timer are allocated here. All addresses, which have nothing allocated within the SFR, are reserved space and cannot be accessed by users.

The special page vectors are allocated in addresses FFFE00₁₆ to FFFFDB₁₆. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **Software Manual** for details.

In memory expansion mode and microprocessor mode, some space are reserved and cannot be accessed by users.

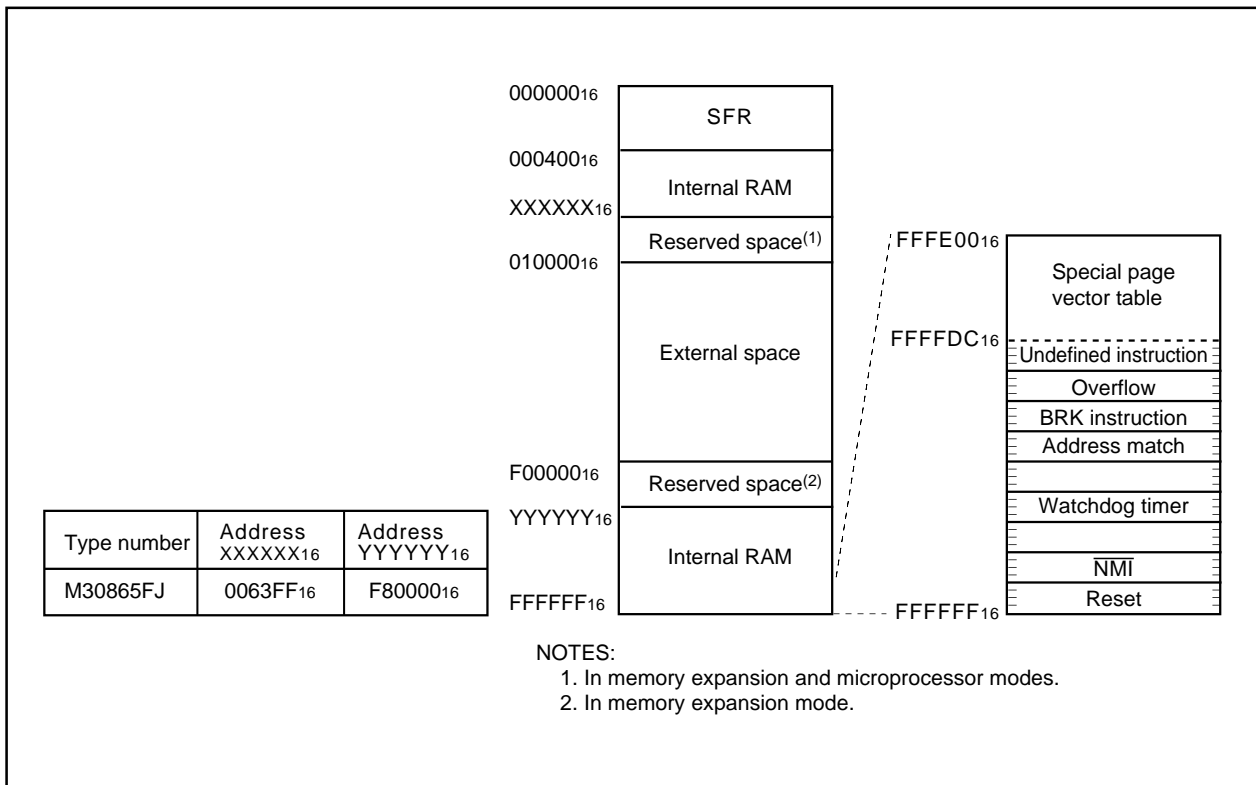


Figure 3.1 Memory Map

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0	PM0	1000 0000 ₂ (CNVss pin ="L") 0000 0011 ₂ (CNVss pin ="H")
0005 ₁₆	Processor mode register 1	PM1	0X00 0000 ₂
0006 ₁₆	System clock control register 0	CM0	0000 1000 ₂
0007 ₁₆	System clock control register 1	CM1	0010 0000 ₂
0008 ₁₆			
0009 ₁₆	Address match interrupt enable register	AIER	00 ₁₆
000A ₁₆	Protect register	PRCR	XXXX 0000 ₂
000B ₁₆	External data bus width control register	DS	XXXX 1000 ₂ (BYTE pin ="L") XXXX 0000 ₂ (BYTE pin ="H")
000C ₁₆	Main clock division register	MCD	XXX0 1000 ₂
000D ₁₆	Oscillation stop detect register	CM2	00 ₁₆
000E ₁₆	Watchdog timer start register	WDTS	XX ₁₆
000F ₁₆	Watchdog timer control register	WDC	000X XXXX ₂
0010 ₁₆			
0011 ₁₆	Address match interrupt register 0	RMAD0	000000 ₁₆
0012 ₁₆			
0013 ₁₆	Processor mode register 2	PM2	XXX0 0000 ₂
0014 ₁₆			
0015 ₁₆	Address match interrupt register 1	RMAD1	000000 ₁₆
0016 ₁₆			
0017 ₁₆	Voltage detection register 2	VCR2	00 ₁₆
0018 ₁₆			
0019 ₁₆	Address match interrupt register 2	RMAD2	000000 ₁₆
001A ₁₆			
001B ₁₆	Voltage detection register 1	VCR1	0000 1000 ₂
001C ₁₆			
001D ₁₆	Address match interrupt register 3	RMAD3	000000 ₁₆
001E ₁₆			
001F ₁₆			
0020 ₁₆			
0021 ₁₆			
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆			
0026 ₁₆	PLL control register 0	PLC0	0001 X010 ₂
0027 ₁₆	PLL control register 1	PLC1	000X 0000 ₂
0028 ₁₆			
0029 ₁₆	Address match interrupt register 4	RMAD4	000000 ₁₆
002A ₁₆			
002B ₁₆			
002C ₁₆			
002D ₁₆	Address match interrupt register 5	RMAD5	000000 ₁₆
002E ₁₆			
002F ₁₆	Voltage down detect interrupt register	D4INT	XX00 0000 ₂

X: Indeterminate

Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	Value after RESET
0030 ₁₆			
0031 ₁₆			
0032 ₁₆			
0033 ₁₆			
0034 ₁₆			
0035 ₁₆			
0036 ₁₆			
0037 ₁₆			
0038 ₁₆	Address match interrupt register 6	RMAD6	000000 ₁₆
0039 ₁₆			
003A ₁₆			
003B ₁₆			
003C ₁₆	Address match interrupt register 7	RMAD7	000000 ₁₆
003D ₁₆			
003E ₁₆			
003F ₁₆			
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆			
0045 ₁₆			
0046 ₁₆			
0047 ₁₆			
0048 ₁₆	External space wait control register 0	EWCR0	X0X0 0011 ₂
0049 ₁₆	External space wait control register 1	EWCR1	X0X0 0011 ₂
004A ₁₆	External space wait control register 2	EWCR1	X0X0 0011 ₂
004B ₁₆	External space wait control register 3	EWCR3	X0X0 0011 ₂
004C ₁₆	Page mode wait control register 0	PWCR0	0001 0001 ₂
004D ₁₆	Page mode wait control register 1	PWCR1	0001 0001 ₂
004E ₁₆			
004F ₁₆			
0050 ₁₆			
0051 ₁₆			
0052 ₁₆			
0053 ₁₆			
0054 ₁₆			
0055 ₁₆	Flash memory control register 1	FMR1	0000 0101 ₂
0056 ₁₆			
0057 ₁₆	Flash memory control register 0	FMR0	0000 0001 ₂
0058 ₁₆			
0059 ₁₆			
005A ₁₆			
005B ₁₆			
005C ₁₆			
005D ₁₆			
005E ₁₆			
005F ₁₆			

X: Indeterminate

Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	Value after RESET
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆	DMA0 interrupt control register	DM0IC	XXXX X000 ₂
0069 ₁₆	Timer B5 interrupt control register	TB5IC	XXXX X000 ₂
006A ₁₆	DMA2 interrupt control register	DM2IC	XXXX X000 ₂
006B ₁₆	UART2 receive /ACK interrupt control register	S2RIC	XXXX X000 ₂
006C ₁₆	Timer A0 interrupt control register	TA0IC	XXXX X000 ₂
006D ₁₆	UART3 receive /ACK interrupt control register	S3RIC	XXXX X000 ₂
006E ₁₆	Timer A2 interrupt control register	TA2IC	XXXX X000 ₂
006F ₁₆	UART4 receive /ACK interrupt control register	S4RIC	XXXX X000 ₂
0070 ₁₆	Timer A4 interrupt control register	TA4IC	XXXX X000 ₂
0071 ₁₆	UART0/UART3 bus conflict detect interrupt control register	BCN0IC/BCN3IC	XXXX X000 ₂
0072 ₁₆	UART0 receive/ACK interrupt control register	S0RIC	XXXX X000 ₂
0073 ₁₆	A-D0 conversion interrupt control register	AD0IC	XXXX X000 ₂
0074 ₁₆	UART1 receive/ACK interrupt control register	S1RIC	XXXX X000 ₂
0075 ₁₆	Intelligent I/O interrupt control register 0 CAN interrupt 3 control register	IIO0IC CAN3IC	XXXX X000 ₂
0076 ₁₆	Timer B1 interrupt control register	TB1IC	XXXX X000 ₂
0077 ₁₆	Intelligent I/O interrupt control register 2	IIO2IC	XXXX X000 ₂
0078 ₁₆	Timer B3 interrupt control register	TB3IC	XXXX X000 ₂
0079 ₁₆	Intelligent I/O interrupt control register 4	IIO4IC	XXXX X000 ₂
007A ₁₆	INT5 interrupt control register	INT5IC	XX00 X000 ₂
007B ₁₆			
007C ₁₆	INT3 interrupt control register	INT3IC	XX00 X000 ₂
007D ₁₆	Intelligent I/O interrupt control register 8	IIO8IC	XXXX X000 ₂
007E ₁₆	INT1 interrupt control register	INT1IC	XX00 X000 ₂
007F ₁₆	Intelligent I/O interrupt control register 10/ CAN interrupt 1 control register	IIO10IC CAN1IC	XXXX X000 ₂
0080 ₁₆			
0081 ₁₆	CAN interrupt 2 control register	CAN2IC	XXXX X000 ₂
0082 ₁₆			
0083 ₁₆			
0084 ₁₆			
0085 ₁₆			
0086 ₁₆			
0087 ₁₆			
0088 ₁₆	DMA1 interrupt control register	DM1IC	XXXX X000 ₂
0089 ₁₆	UART2 transmit /NACK interrupt control register	S2TIC	XXXX X000 ₂
008A ₁₆	DMA3 interrupt control register	DM3IC	XXXX X000 ₂
008B ₁₆	UART3 transmit /NACK interrupt control register	S3TIC	XXXX X000 ₂
008C ₁₆	Timer A1 interrupt control register	TA1IC	XXXX X000 ₂
008D ₁₆	UART4 transmit /NACK interrupt control register	S4TIC	XXXX X000 ₂
008E ₁₆	Timer A3 interrupt control register	TA3IC	XXXX X000 ₂
008F ₁₆	UART2 bus conflict detect interrupt control register	BCN2IC	XXXX X000 ₂

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Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	Value after RESET
0090 ₁₆	UART0 transmit /NACK interrupt control register	S0TIC	XXXX X000 ₂
0091 ₁₆	UART1/UART4 bus conflict detect interrupt control register	BCN11C/BCN41C	XXXX X000 ₂
0092 ₁₆	UART1 transmit/NACK interrupt control register	S1TIC	XXXX X000 ₂
0093 ₁₆	Key input interrupt control register	KUPIC	XXXX X000 ₂
0094 ₁₆	Timer B0 interrupt control register	TB01C	XXXX X000 ₂
0095 ₁₆	Intelligent I/O interrupt control register 1 CAN interrupt 4 control register	IIO11C CAN41C	XXXX X000 ₂
0096 ₁₆	Timer B2 interrupt control register	TB21C	XXXX X000 ₂
0097 ₁₆	Intelligent I/O interrupt control register 3	IIO31C	XXXX X000 ₂
0098 ₁₆	Timer B4 interrupt control register	TB41C	XXXX X000 ₂
0099 ₁₆	CAN interrupt 5 control register	CAN51C	XXXX X000 ₂
009A ₁₆	INT4 interrupt control register	INT41C	XX00 X000 ₂
009B ₁₆			
009C ₁₆	INT2 interrupt control register	INT21C	XX00 X000 ₂
009D ₁₆	Intelligent I/O interrupt control register 9/ CAN interrupt 0 control register	IIO91C CAN01C	XXXX X000 ₂
009E ₁₆	INT0 interrupt control register	INT01C	XX00 X000 ₂
009F ₁₆	Exit priority control register	RLVL	XXXX 0000 ₂
00A0 ₁₆	Interrupt request register 0	IIO01R	0000 X00X ₂
00A1 ₁₆	Interrupt request register 1	IIO11R	0000 X00X ₂
00A2 ₁₆	Interrupt request register 2	IIO21R	0000 X00X ₂
00A3 ₁₆	Interrupt request register 3	IIO31R	0000 X00X ₂
00A4 ₁₆	Interrupt request register 4	IIO41R	0000 X00X ₂
00A5 ₁₆	Interrupt request register 5	IIO51R	0000 X00X ₂
00A6 ₁₆			
00A7 ₁₆			
00A8 ₁₆	Interrupt request register 8	IIO81R	0000 X00X ₂
00A9 ₁₆	Interrupt request register 9	IIO91R	0000 X00X ₂
00AA ₁₆	Interrupt request register 10	IIO101R	0000 X00X ₂
00AB ₁₆	Interrupt request register 11	IIO111R	0000 X00X ₂
00AC ₁₆			
00AD ₁₆			
00AE ₁₆			
00AF ₁₆			
00B0 ₁₆	Interrupt enable register 0	IIO01E	0000 X000 ₂
00B1 ₁₆	Interrupt enable register 1	IIO11E	0000 X000 ₂
00B2 ₁₆	Interrupt enable register 2	IIO21E	0000 X000 ₂
00B3 ₁₆	Interrupt enable register 3	IIO31E	0000 X000 ₂
00B4 ₁₆	Interrupt enable register 4	IIO41E	0000 X000 ₂
00B5 ₁₆	Interrupt enable register 5	IIO51E	0000 X000 ₂
00B6 ₁₆			
00B7 ₁₆			
00B8 ₁₆	Interrupt enable register 8	IIO81E	0000 X000 ₂
00B9 ₁₆	Interrupt enable register 9	IIO91E	0000 X000 ₂
00BA ₁₆	Interrupt enable register 10	IIO101E	0000 X000 ₂
00BB ₁₆	Interrupt enable register 11	IIO111E	0000 X000 ₂
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

X: Indeterminate

Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0 ₁₆			
00C1 ₁₆			
00C2 ₁₆			
00C3 ₁₆			
00C4 ₁₆			
00C5 ₁₆			
00C6 ₁₆			
00C7 ₁₆			
00C8 ₁₆			
00C9 ₁₆			
00CA ₁₆			
00CB ₁₆			
00CC ₁₆			
00CD ₁₆			
00CE ₁₆			
00CF ₁₆			
00D0 ₁₆			
00D1 ₁₆			
00D2 ₁₆			
00D3 ₁₆			
00D4 ₁₆			
00D5 ₁₆			
00D6 ₁₆			
00D7 ₁₆			
00D8 ₁₆			
00D9 ₁₆			
00DA ₁₆			
00DB ₁₆			
00DC ₁₆			
00DD ₁₆			
00DE ₁₆			
00DF ₁₆			
00E0 ₁₆			
00E1 ₁₆			
00E2 ₁₆			
00E3 ₁₆			
00E4 ₁₆			
00E5 ₁₆			
00E6 ₁₆			
00E7 ₁₆			
00E8 ₁₆ 00E9 ₁₆	SI/O receive buffer register 0	G0RB	XXXX XXXX ₂ XX00 XXXX ₂
00EA ₁₆ 00EB ₁₆	Transmit buffer/receive data register 0	G0TB	XX ₁₆
00EC ₁₆	Receive input register 0	G0RI	XX ₁₆
00ED ₁₆	SI/O communication mode register 0	G0MR	00 ₁₆
00EE ₁₆	Transmit output register 0	G0TO	XX ₁₆
00EF ₁₆	SI/O communication control register 0	G0CR	0000 X011 ₂

X: Indeterminate

Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	Value after RESET
00F0 ₁₆	Data compare register 00	G0CMP0	XX ₁₆
00F1 ₁₆	Data compare register 01	G0CMP1	XX ₁₆
00F2 ₁₆	Data compare register 02	G0CMP2	XX ₁₆
00F3 ₁₆	Data compare register 03	G0CMP3	XX ₁₆
00F4 ₁₆	Data mask register 00	G0MSK0	XX ₁₆
00F5 ₁₆	Data mask register 01	G0MSK1	XX ₁₆
00F6 ₁₆	Communication clock select register	CCS	XXXX 0000 ₂
00F7 ₁₆			
00F8 ₁₆ 00F9 ₁₆	Receive CRC code register 0	G0RCRC	XX ₁₆ XX ₁₆
00FA ₁₆ 00FB ₁₆	Transmit CRC code register 0	G0TCRC	00 ₁₆ 00 ₁₆
00FC ₁₆	SI/O extended mode register 0	G0EMR	00 ₁₆
00FD ₁₆	SI/O extended receive control register 0	G0ERC	00 ₁₆
00FE ₁₆	SI/O special communication interrupt detect register 0	G0IRF	0000 00XX ₂
00FF ₁₆	SI/O extended transmit control register 0	G0ETC	0000 0XXX ₂
0100 ₁₆ 0101 ₁₆	Time measurement/waveform generating register 10	G1TM0/G1PO0	XX ₁₆ XX ₁₆
0102 ₁₆ 0103 ₁₆	Time measurement/waveform generating register 11	G1TM1/G1PO1	XX ₁₆ XX ₁₆
0104 ₁₆ 0105 ₁₆	Time measurement/waveform generating register 12	G1TM2/G1PO2	XX ₁₆ XX ₁₆
0106 ₁₆ 0107 ₁₆	Time measurement/waveform generating register 13	G1TM3/G1PO3	XX ₁₆ XX ₁₆
0108 ₁₆ 0109 ₁₆	Time measurement/waveform generating register 14	G1TM4/G1PO4	XX ₁₆ XX ₁₆
010A ₁₆ 010B ₁₆	Time measurement/waveform generating register 15	G1TM5/G1PO5	XX ₁₆ XX ₁₆
010C ₁₆ 010D ₁₆	Time measurement/waveform generating register 16	G1TM6/G1PO6	XX ₁₆ XX ₁₆
010E ₁₆ 010F ₁₆	Time measurement/waveform generating register 17	G1TM7/G1PO7	XX ₁₆ XX ₁₆
0110 ₁₆	Waveform generating control register 10	G1POCR0	0000 X000 ₂
0111 ₁₆	Waveform generating control register 11	G1POCR1	0X00 X000 ₂
0112 ₁₆	Waveform generating control register 12	G1POCR2	0X00 X000 ₂
0113 ₁₆	Waveform generating control register 13	G1POCR3	0X00 X000 ₂
0114 ₁₆	Waveform generating control register 14	G1POCR4	0X00 X000 ₂
0115 ₁₆	Waveform generating control register 15	G1POCR5	0X00 X000 ₂
0116 ₁₆	Waveform generating control register 16	G1POCR6	0X00 X000 ₂
0117 ₁₆	Waveform generating control register 17	G1POCR7	0X00 X000 ₂
0118 ₁₆	Time measurement control register 10	G1TMCR0	00 ₁₆
0119 ₁₆	Time measurement control register 11	G1TMCR1	00 ₁₆
011A ₁₆	Time measurement control register 12	G1TMCR2	00 ₁₆
011B ₁₆	Time measurement control register 13	G1TMCR3	00 ₁₆
011C ₁₆	Time measurement control register 14	G1TMCR4	00 ₁₆
011D ₁₆	Time measurement control register 15	G1TMCR5	00 ₁₆
011E ₁₆	Time measurement control register 16	G1TMCR6	00 ₁₆
011F ₁₆	Time measurement control register 17	G1TMCR7	00 ₁₆

X: Indeterminate

Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	Value after RESET
0120 ₁₆	Base timer register 1	G1BT	XX ₁₆
0121 ₁₆			XX ₁₆
0122 ₁₆	Base timer control register 10	G1BCR0	00 ₁₆
0123 ₁₆	Base timer control register 11	G1BCR1	00 ₁₆
0124 ₁₆	Time measurement prescaler register 16	G1TPR6	00 ₁₆
0125 ₁₆	Time measurement prescaler register 17	G1TPR7	00 ₁₆
0126 ₁₆	Function enable register 1	G1FE	00 ₁₆
0127 ₁₆	Function select register 1	G1FS	00 ₁₆
0128 ₁₆	SI/O receive buffer register 1	G1RB	XXXX XXXX ₂
0129 ₁₆			XX00 XXXX ₂
012A ₁₆	Transmit buffer/receive data register 1	G1TB	XX ₁₆
012B ₁₆			
012C ₁₆	Receive input register 1	G1RI	XX ₁₆
012D ₁₆	SI/O communication mode register 1	G1MR	00 ₁₆
012E ₁₆	Transmit output register 1	G1TO	XX ₁₆
012F ₁₆	SI/O communication control register 1	G1CR	0000 X01 ₁₂
0130 ₁₆	Data compare register 10	G1CMP0	XX ₁₆
0131 ₁₆	Data compare register 11	G1CMP1	XX ₁₆
0132 ₁₆	Data compare register 12	G1CMP2	XX ₁₆
0133 ₁₆	Data compare register 13	G1CMP3	XX ₁₆
0134 ₁₆	Data mask register 10	G1MSK0	XX ₁₆
0135 ₁₆	Data mask register 11	G1MSK1	XX ₁₆
0136 ₁₆			
0137 ₁₆			
0138 ₁₆	Receive CRC code register 1	G1RCRC	XX ₁₆
0139 ₁₆			XX ₁₆
013A ₁₆	Transmit CRC code register 1	G1TCRC	00 ₁₆
013B ₁₆			00 ₁₆
013C ₁₆	SI/O extended mode register 1	G1EMR	00 ₁₆
013D ₁₆	SI/O extended receive control register 1	G1ERC	00 ₁₆
013E ₁₆	SI/O special communication interrupt detect register 1	G1IRF	0000 00XX ₂
013F ₁₆	SI/O extended transmit control register 1	G1ETC	0000 0XXX ₂
0140 ₁₆			
0141 ₁₆			
0142 ₁₆			
0143 ₁₆			
0144 ₁₆			
0145 ₁₆			
0146 ₁₆			
0147 ₁₆			
0148 ₁₆			
0149 ₁₆			
014A ₁₆			
014B ₁₆			
014C ₁₆			
014D ₁₆			
014E ₁₆			
014F ₁₆			

X: Indeterminate

Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	Value after RESET
0150 ₁₆			
0151 ₁₆			
0152 ₁₆			
0153 ₁₆			
0154 ₁₆			
0155 ₁₆			
0156 ₁₆			
0157 ₁₆			
0158 ₁₆			
0159 ₁₆			
015A ₁₆			
015B ₁₆			
015C ₁₆			
015D ₁₆			
015E ₁₆			
015F ₁₆			
0160 ₁₆			
0161 ₁₆			
0162 ₁₆			
0163 ₁₆			
0164 ₁₆			
0165 ₁₆			
0166 ₁₆			
0167 ₁₆			
0168 ₁₆			
0169 ₁₆			
016A ₁₆			
016B ₁₆			
016C ₁₆			
016D ₁₆			
016E ₁₆			
016F ₁₆			
0170 ₁₆			
0171 ₁₆			
0172 ₁₆			
0173 ₁₆			
0174 ₁₆			
0175 ₁₆			
0176 ₁₆			
0177 ₁₆			
0178 ₁₆	Input function select register	IPS	00 ₁₆
0179 ₁₆	Input function select register A	IPSA	00 ₁₆
017A ₁₆			
017B ₁₆			
017C ₁₆			
017D ₁₆ to 01DF ₁₆			

X: Indeterminate

Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	Value after RESET
01E0 ₁₆	CAN0 message slot buffer 0 standard ID0	C0SLOT0_0	XX ₁₆
01E1 ₁₆	CAN0 message slot buffer 0 standard ID1	C0SLOT0_1	XX ₁₆
01E2 ₁₆	CAN0 message slot buffer 0 extended ID0	C0SLOT0_2	XX ₁₆
01E3 ₁₆	CAN0 message slot buffer 0 extended ID1	C0SLOT0_3	XX ₁₆
01E4 ₁₆	CAN0 message slot buffer 0 extended ID2	C0SLOT0_4	XX ₁₆
01E5 ₁₆	CAN0 message slot buffer 0 data length code	C0SLOT0_5	XX ₁₆
01E6 ₁₆	CAN0 message slot buffer 0 data 0	C0SLOT0_6	XX ₁₆
01E7 ₁₆	CAN0 message slot buffer 0 data 1	C0SLOT0_7	XX ₁₆
01E8 ₁₆	CAN0 message slot buffer 0 data 2	C0SLOT0_8	XX ₁₆
01E9 ₁₆	CAN0 message slot buffer 0 data 3	C0SLOT0_9	XX ₁₆
01EA ₁₆	CAN0 message slot buffer 0 data 4	C0SLOT0_10	XX ₁₆
01EB ₁₆	CAN0 message slot buffer 0 data 5	C0SLOT0_11	XX ₁₆
01EC ₁₆	CAN0 message slot buffer 0 data 6	C0SLOT0_12	XX ₁₆
01ED ₁₆	CAN0 message slot buffer 0 data 7	C0SLOT0_13	XX ₁₆
01EE ₁₆	CAN0 message slot buffer 0 time stamp high-order	C0SLOT0_14	XX ₁₆
01EF ₁₆	CAN0 message slot buffer 0 time stamp low-order	C0SLOT0_15	XX ₁₆
01F0 ₁₆	CAN0 message slot buffer 1 standard ID0	C0SLOT1_0	XX ₁₆
01F1 ₁₆	CAN0 message slot buffer 1 standard ID1	C0SLOT1_1	XX ₁₆
01F2 ₁₆	CAN0 message slot buffer 1 extended ID0	C0SLOT1_2	XX ₁₆
01F3 ₁₆	CAN0 message slot buffer 1 extended ID1	C0SLOT1_3	XX ₁₆
01F4 ₁₆	CAN0 message slot buffer 1 extended ID2	C0SLOT1_4	XX ₁₆
01F5 ₁₆	CAN0 message slot buffer 1 data length code	C0SLOT1_5	XX ₁₆
01F6 ₁₆	CAN0 message slot buffer 1 data 0	C0SLOT1_6	XX ₁₆
01F7 ₁₆	CAN0 message slot buffer 1 data 1	C0SLOT1_7	XX ₁₆
01F8 ₁₆	CAN0 message slot buffer 1 data 2	C0SLOT1_8	XX ₁₆
01F9 ₁₆	CAN0 message slot buffer 1 data 3	C0SLOT1_9	XX ₁₆
01FA ₁₆	CAN0 message slot buffer 1 data 4	C0SLOT1_10	XX ₁₆
01FB ₁₆	CAN0 message slot buffer 1 data 5	C0SLOT1_11	XX ₁₆
01FC ₁₆	CAN0 message slot buffer 1 data 6	C0SLOT1_12	XX ₁₆
01FD ₁₆	CAN0 message slot buffer 1 data 7	C0SLOT1_13	XX ₁₆
01FE ₁₆	CAN0 message slot buffer 1 time stamp high-order	C0SLOT1_14	XX ₁₆
01FF ₁₆	CAN0 message slot buffer 1 time stamp low-order	C0SLOT1_15	XX ₁₆
0200 ₁₆	CAN0 control register 0	C0CTRL0	XX01 0X01 ₂ ⁽¹⁾
0201 ₁₆			XXXX 0000 ₂ ⁽¹⁾
0202 ₁₆	CAN0 status register	C0STR	0000 0000 ₂ ⁽¹⁾
0203 ₁₆			X000 0X01 ₂ ⁽¹⁾
0204 ₁₆	CAN0 extended ID register	C0IDR	00 ₁₆ ⁽¹⁾
0205 ₁₆			00 ₁₆ ⁽¹⁾
0206 ₁₆	CAN0 configuration register	C0CONR	0000 XXXX ₂ ⁽¹⁾
0207 ₁₆			0000 0000 ₂ ⁽¹⁾
0208 ₁₆	CAN0 time stamp register	C0TSR	00 ₁₆ ⁽¹⁾
0209 ₁₆			00 ₁₆ ⁽¹⁾
020A ₁₆	CAN0 transmit error count register	C0TEC	00 ₁₆ ⁽¹⁾
020B ₁₆	CAN0 receive error count register	C0REC	00 ₁₆ ⁽¹⁾
020C ₁₆	CAN0 slot interrupt status register	C0SISTR	00 ₁₆ ⁽¹⁾
020D ₁₆			00 ₁₆ ⁽¹⁾
020E ₁₆			
020F ₁₆			

X: Indeterminate

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NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
0210 ₁₆	CAN0 slot interrupt mask register	C0SIMKR	00 ₁₆ ⁽²⁾
0211 ₁₆			00 ₁₆ ⁽²⁾
0212 ₁₆			
0213 ₁₆			
0214 ₁₆	CAN0 error interrupt mask register	C0EIMKR	XXXX X000 ₂ ⁽²⁾
0215 ₁₆	CAN0 error interrupt status register	C0EISTR	XXXX X000 ₂ ⁽²⁾
0216 ₁₆	CAN0 error cause register	C0EFR	00 ₁₆ ⁽²⁾
0217 ₁₆	CAN0 baud rate prescaler	C0BRP	0000 0001 ₂ ⁽²⁾
0218 ₁₆			
0219 ₁₆	CAN0 mode register	C0MDR	XXXX XX00 ₂ ⁽²⁾
021A ₁₆			
021B ₁₆			
021C ₁₆			
021D ₁₆			
021E ₁₆			
021F ₁₆			
0220 ₁₆	CAN0 single shot control register	C0SSCTLR	00 ₁₆ ⁽²⁾
0221 ₁₆			00 ₁₆ ⁽²⁾
0222 ₁₆			
0223 ₁₆			
0224 ₁₆	CAN0 single shot status register	C0SSSTR	00 ₁₆ ⁽²⁾
0225 ₁₆			00 ₁₆ ⁽²⁾
0226 ₁₆			
0227 ₁₆			
0228 ₁₆	CAN0 global mask register standard ID0	C0GMR0	XXX0 0000 ₂ ⁽²⁾
0229 ₁₆	CAN0 global mask register standard ID1	C0GMR1	XX00 0000 ₂ ⁽²⁾
022A ₁₆	CAN0 global mask register extended ID0	C0GMR2	XXXX 0000 ₂ ⁽²⁾
022B ₁₆	CAN0 global mask register extended ID1	C0GMR3	00 ₁₆ ⁽²⁾
022C ₁₆	CAN0 global mask register extended ID2	C0GMR4	XX00 0000 ₂ ⁽²⁾
022D ₁₆			
022E ₁₆			
022F ₁₆			
0230 ₁₆	CAN0 message slot 0 control register /	C0MCTL0/	0000 0000 ₂ ⁽²⁾
	CAN0 local mask register A standard ID0	C0LMAR0	XXX0 0000 ₂ ⁽²⁾
0231 ₁₆	CAN0 message slot 1 control register /	C0MCTL1/	0000 0000 ₂ ⁽²⁾
	CAN0 local mask register A standard ID1	C0LMAR1	XX00 0000 ₂ ⁽²⁾
0232 ₁₆	CAN0 message slot 2 control register /	C0MCTL2/	0000 0000 ₂ ⁽²⁾
	CAN0 local mask register A extended ID0	C0LMAR2	XXXX 0000 ₂ ⁽²⁾
0233 ₁₆	CAN0 message slot 3 control register /	C0MCTL3/	00 ₁₆ ⁽²⁾
	CAN0 local mask register A extended ID1	C0LMAR3	00 ₁₆ ⁽²⁾
0234 ₁₆	CAN0 message slot 4 control register /	C0MCTL4/	0000 0000 ₂ ⁽²⁾
	CAN0 local mask register A extended ID2	C0LMAR4	XX00 0000 ₂ ⁽²⁾
0235 ₁₆	CAN0 message slot 5 control register	C0MCTL5	00 ₁₆ ⁽²⁾
0236 ₁₆	CAN0 message slot 6 control register	C0MCTL6	00 ₁₆ ⁽²⁾
0237 ₁₆	CAN0 message slot 7 control register	C0MCTL7	00 ₁₆ ⁽²⁾
0238 ₁₆	CAN0 message slot 8 control register /	C0MCTL8/	0000 0000 ₂ ⁽²⁾
	CAN0 local mask register B standard ID0	C0LMBR0	XXX0 0000 ₂ ⁽²⁾

(Note 1)

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NOTES:

- Addresses 0230₁₆ to 023F₁₆ are switched its function in the BankSel bit of COCTLR1 register.
- Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
0239 ₁₆	CAN0 message slot 9 control register / CAN0 local mask register B standard ID1	C0MCTL9/ C0LMBR1	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
023A ₁₆	CAN0 message slot 10 control register / CAN0 local mask register B extended ID0	C0MCTL10/ C0LMBR2	0000 0000 ₂ ⁽²⁾ XXXX 0000 ₂ ⁽²⁾
023B ₁₆	CAN0 message slot 11 control register / CAN0 local mask register B extended ID1	C0MCTL11/ C0LMBR3	00 ₁₆ ⁽²⁾ 00 ₁₆ ⁽²⁾
023C ₁₆	CAN0 message slot 12 control register / CAN0 local mask register B extended ID2	C0MCTL12/ C0LMBR4	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
023D ₁₆	CAN0 message slot 13 control register	C0MCTL13	00 ₁₆ ⁽²⁾
023E ₁₆	CAN0 message slot 14 control register	C0MCTL14	00 ₁₆ ⁽²⁾
023F ₁₆	CAN0 message slot 15 control register	C0MCTL15	00 ₁₆ ⁽²⁾
0240 ₁₆	CAN0 slot buffer select register	C0SBS	00 ₁₆ ⁽²⁾
0241 ₁₆	CAN0 control register 1	C0CTLR1	X000 00XX ₂ ⁽²⁾
0242 ₁₆	CAN0 sleep control register	C0SLPR	XXXX XXX0 ₂
0243 ₁₆			
0244 ₁₆	CAN0 acceptance filter support register	C0AFS	00 ₁₆ ⁽²⁾
0245 ₁₆			01 ₁₆ ⁽²⁾
0246 ₁₆			
0247 ₁₆			
0248 ₁₆			
0249 ₁₆			
024A ₁₆			
024B ₁₆			
024C ₁₆			
024D ₁₆			
024E ₁₆			
024F ₁₆			
0250 ₁₆	CAN1 slot buffer select register	C1SBS	00 ₁₆ ⁽³⁾
0251 ₁₆	CAN1 control register 1	C1CTLR1	X000 00XX ₂ ⁽³⁾
0252 ₁₆	CAN1 sleep control register	C1SLPR	XXXX XXX0 ₂ ⁽³⁾
0253 ₁₆			
0254 ₁₆	CAN1 acceptance filter support register	C1AFS	0100 ₁₆ ⁽³⁾
0255 ₁₆			
0256 ₁₆			
0257 ₁₆			
0258 ₁₆			
0259 ₁₆			
025A ₁₆			
025B ₁₆			
025C ₁₆			
025D ₁₆			
025E ₁₆			
025F ₁₆			

(Note 1)

X: Indeterminate

Blank columns are all reserved space. No access is allowed.

NOTES:

- Addresses 0230₁₆ to 023F₁₆ are switched its function in the BANKSEL bit in the C0CTLR1 register.
- Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.
- Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
0260 ₁₆	CAN1 message slot buffer 0 standard ID0	C1SLOT0_0	XX ₁₆
0261 ₁₆	CAN1 message slot buffer 0 standard ID1	C1SLOT0_1	XX ₁₆
0262 ₁₆	CAN1 message slot buffer 0 extended ID0	C1SLOT0_2	XX ₁₆
0263 ₁₆	CAN1 message slot buffer 0 extended ID1	C1SLOT0_3	XX ₁₆
0264 ₁₆	CAN1 message slot buffer 0 extended ID2	C1SLOT0_4	XX ₁₆
0265 ₁₆	CAN1 message slot buffer 0 data length code	C1SLOT0_5	XX ₁₆
0266 ₁₆	CAN1 message slot buffer 0 data 0	C1SLOT0_6	XX ₁₆
0267 ₁₆	CAN1 message slot buffer 0 data 1	C1SLOT0_7	XX ₁₆
0268 ₁₆	CAN1 message slot buffer 0 data 2	C1SLOT0_8	XX ₁₆
0269 ₁₆	CAN1 message slot buffer 0 data 3	C1SLOT0_9	XX ₁₆
026A ₁₆	CAN1 message slot buffer 0 data 4	C1SLOT0_10	XX ₁₆
026B ₁₆	CAN1 message slot buffer 0 data 5	C1SLOT0_11	XX ₁₆
026C ₁₆	CAN1 message slot buffer 0 data 6	C1SLOT0_12	XX ₁₆
026D ₁₆	CAN1 message slot buffer 0 data 7	C1SLOT0_13	XX ₁₆
026E ₁₆	CAN1 message slot buffer 0 time stamp high-order	C1SLOT0_14	XX ₁₆
026F ₁₆	CAN1 message slot buffer 0 time stamp low-order	C1SLOT0_15	XX ₁₆
0270 ₁₆	CAN1 message slot buffer 1 standard ID0	C1SLOT1_0	XX ₁₆
0271 ₁₆	CAN1 message slot buffer 1 standard ID1	C1SLOT1_1	XX ₁₆
0272 ₁₆	CAN1 message slot buffer 1 extended ID0	C1SLOT1_2	XX ₁₆
0273 ₁₆	CAN1 message slot buffer 1 extended ID1	C1SLOT1_3	XX ₁₆
0274 ₁₆	CAN1 message slot buffer 1 extended ID2	C1SLOT1_4	XX ₁₆
0275 ₁₆	CAN1 message slot buffer 1 data length code	C1SLOT1_5	XX ₁₆
0276 ₁₆	CAN1 message slot buffer 1 data 0	C1SLOT1_6	XX ₁₆
0277 ₁₆	CAN1 message slot buffer 1 data 1	C1SLOT1_7	XX ₁₆
0278 ₁₆	CAN1 message slot buffer 1 data 2	C1SLOT1_8	XX ₁₆
0279 ₁₆	CAN1 message slot buffer 1 data 3	C1SLOT1_9	XX ₁₆
027A ₁₆	CAN1 message slot buffer 1 data 4	C1SLOT1_10	XX ₁₆
027B ₁₆	CAN1 message slot buffer 1 data 5	C1SLOT1_11	XX ₁₆
027C ₁₆	CAN1 message slot buffer 1 data 6	C1SLOT1_12	XX ₁₆
027D ₁₆	CAN1 message slot buffer 1 data 7	C1SLOT1_13	XX ₁₆
027E ₁₆	CAN1 message slot buffer 1 time stamp high-order	C1SLOT1_14	XX ₁₆
027F ₁₆	CAN1 message slot buffer 1 time stamp low-order	C1SLOT1_15	XX ₁₆
0280 ₁₆	CAN1 control register 0	C1CTLR0	XX01 0X01 ₂ ⁽¹⁾
0281 ₁₆			XXXX 0000 ₂ ⁽¹⁾
0282 ₁₆	CAN1 status register	C1STR	0000 0000 ₂ ⁽¹⁾
0283 ₁₆			X000 0X01 ₂ ⁽¹⁾
0284 ₁₆	CAN1 extended ID register	C1IDR	00 ₁₆ ⁽¹⁾
0285 ₁₆			00 ₁₆ ⁽¹⁾
0286 ₁₆	CAN1 configuration register	C1CONR	0000 XXXX ₂ ⁽¹⁾
0287 ₁₆			0000 0000 ₂ ⁽¹⁾
0288 ₁₆	CAN1 time stamp register	C1TSR	00 ₁₆ ⁽¹⁾
0289 ₁₆			00 ₁₆ ⁽¹⁾
028A ₁₆	CAN1 transmit error count register	C1TEC	00 ₁₆ ⁽¹⁾
028B ₁₆	CAN1 receive error count register	C1REC	00 ₁₆ ⁽¹⁾
028C ₁₆	CAN1 slot interrupt status register	C1SISTR	00 ₁₆ ⁽¹⁾
028D ₁₆			00 ₁₆ ⁽¹⁾
028E ₁₆			
028F ₁₆			

X: Indeterminate

Blank columns are all reserved space. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
0290 ₁₆	CAN1 slot interrupt mask register	C1SIMKR	00 ₁₆ ⁽²⁾
0291 ₁₆			00 ₁₆ ⁽²⁾
0292 ₁₆			
0293 ₁₆			
0294 ₁₆	CAN1 error interrupt mask register	C1EIMKR	XXXX X000 ₂ ⁽²⁾
0295 ₁₆	CAN1 error interrupt status register	C1EISTR	XXXX X000 ₂ ⁽²⁾
0296 ₁₆	CAN1 error factor register	C1EFR	00 ₁₆ ⁽²⁾
0297 ₁₆	CAN1 baud rate prescaler	C1BRP	0000 0001 ₂ ⁽²⁾
0298 ₁₆			
0299 ₁₆	CAN1 mode register	C1MDR	XXXX XX00 ₂ ⁽²⁾
029A ₁₆			
029B ₁₆			
029C ₁₆			
029D ₁₆			
029E ₁₆			
029F ₁₆			
02A0 ₁₆	CAN1 single shot control register	C1SSCTLR	00 ₁₆ ⁽²⁾
02A1 ₁₆			00 ₁₆ ⁽²⁾
02A2 ₁₆			
02A3 ₁₆			
02A4 ₁₆	CAN1 single shot status register	C1SSSTR	00 ₁₆ ⁽²⁾
02A5 ₁₆			00 ₁₆ ⁽²⁾
02A6 ₁₆			
02A7 ₁₆			
02A8 ₁₆	CAN1 global mask register standard ID0	C1GMR0	XXX0 0000 ₂ ⁽²⁾
02A9 ₁₆	CAN1 global mask register standard ID1	C1GMR1	XX00 0000 ₂ ⁽²⁾
02AA ₁₆	CAN1 global mask register extended ID0	C1GMR2	XXXX 0000 ₂ ⁽²⁾
02AB ₁₆	CAN1 global mask register extended ID1	C1GMR3	00 ₁₆ ⁽²⁾
02AC ₁₆	CAN1 global mask register extended ID2	C1GMR4	XX00 0000 ₂ ⁽²⁾
02AD ₁₆			
02AE ₁₆			
02AF ₁₆			
02B0 ₁₆	CAN1 message slot 0 control register /	C1MCTL0/	0000 0000 ₂ ⁽²⁾
	CAN1 local mask register A standard ID0	C1LMAR0	XXX0 0000 ₂ ⁽²⁾
02B1 ₁₆	CAN1 message slot 1 control register /	C1MCTL1/	0000 0000 ₂ ⁽²⁾
	CAN1 local mask register A standard ID1	C1LMAR1	XX00 0000 ₂ ⁽²⁾
02B2 ₁₆	CAN1 message slot 2 control register /	C1MCTL2/	0000 0000 ₂ ⁽²⁾
	CAN1 local mask register A extended ID0	C1LMAR2	XXXX 0000 ₂ ⁽²⁾
02B3 ₁₆	CAN1 message slot 3 control register /	C1MCTL3/	00 ₁₆ ⁽²⁾
	CAN1 local mask register A extended ID1	C1LMAR3	00 ₁₆ ⁽²⁾
02B4 ₁₆	CAN1 message slot 4 control register /	C1MCTL4/	0000 0000 ₂ ⁽²⁾
	CAN1 local mask register A extended ID2	C1LMAR4	XX00 0000 ₂ ⁽²⁾
02B5 ₁₆	CAN1 message slot 5 control register	C1MCTL5	00 ₁₆ ⁽²⁾
02B6 ₁₆	CAN1 message slot 6 control register	C1MCTL6	00 ₁₆ ⁽²⁾
02B7 ₁₆	CAN1 message slot 7 control register	C1MCTL7	00 ₁₆ ⁽²⁾
02B8 ₁₆	CAN1 message slot 8 control register /	C1MCTL8/	0000 0000 ₂ ⁽²⁾
	CAN1 local mask register B standard ID0	C1LMBR0	XXX0 0000 ₂ ⁽²⁾

(Note 1)

X: Indeterminate

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NOTES:

- Addresses 02A0₁₆ to 02BF₁₆ are switched its function in the BANKSEL bit of the C1CTLR1 register.
- Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02B9 ₁₆	CAN1 message slot 9 control register / CAN1 local mask register B standard ID1	C1MCTL9/ C1LMBR1	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
02BA ₁₆	CAN1 message slot 10 control register / CAN1 local mask register B extended ID0	C1MCTL10/ C1LMBR2	0000 0000 ₂ ⁽²⁾ XXXX 0000 ₂ ⁽²⁾
02BB ₁₆	CAN1 message slot 11 control register / CAN1 local mask register B extended ID1	C1MCTL11/ C1LMBR3	00 ₁₆ ⁽²⁾ 00 ₁₆ ⁽²⁾
02BC ₁₆	CAN1 message slot 12 control register / CAN1 local mask register B extended ID2	C1MCTL12/ C1LMBR4	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
02BD ₁₆	CAN1 message slot 13 control register	C1MCTL13	00 ₁₆ ⁽²⁾
02BE ₁₆	CAN1 message slot 14 control register	C1MCTL14	00 ₁₆ ⁽²⁾
02BF ₁₆	CAN1 message slot 15 control register	C1MCTL15	00 ₁₆ ⁽²⁾
02C0 ₁₆ 02C1 ₁₆	X0 register Y0 register	X0R, Y0R	XX ₁₆ XX ₁₆
02C2 ₁₆ 02C3 ₁₆	X1 register Y1 register	X1R, Y1R	XX ₁₆ XX ₁₆
02C4 ₁₆ 02C5 ₁₆	X2 register Y2 register	X2R, Y2R	XX ₁₆ XX ₁₆
02C6 ₁₆ 02C7 ₁₆	X3 register Y3 register	X3R, Y3R	XX ₁₆ XX ₁₆
02C8 ₁₆ 02C9 ₁₆	X4 register Y4 register	X4R, Y4R	XX ₁₆ XX ₁₆
02CA ₁₆ 02CB ₁₆	X5 register Y5 register	X5R, Y5R	XX ₁₆ XX ₁₆
02CC ₁₆ 02CD ₁₆	X6 register Y6 register	X6R, Y6R	XX ₁₆ XX ₁₆
02CE ₁₆ 02CF ₁₆	X7 register Y7 register	X7R, Y7R	XX ₁₆ XX ₁₆
02D0 ₁₆ 02D1 ₁₆	X8 register Y8 register	X8R, Y8R	XX ₁₆ XX ₁₆
02D2 ₁₆ 02D3 ₁₆	X9 register Y9 register	X9R, Y9R	XX ₁₆ XX ₁₆
02D4 ₁₆ 02D5 ₁₆	X10 register Y10 register	X10R, Y10R	XX ₁₆ XX ₁₆
02D6 ₁₆ 02D7 ₁₆	X11 register Y11 register	X11R, Y11R	XX ₁₆ XX ₁₆
02D8 ₁₆ 02D9 ₁₆	X12 register Y12 register	X12R, Y12R	XX ₁₆ XX ₁₆
02DA ₁₆ 02DB ₁₆	X13 register Y13 register	X13R, Y13R	XX ₁₆ XX ₁₆
02DC ₁₆ 02DD ₁₆	X14 register Y14 register	X14R, Y14R	XX ₁₆ XX ₁₆
02DE ₁₆ 02DF ₁₆	X15 register Y15 register	X15R, Y15R	XX ₁₆ XX ₁₆

(Note 1)

X: Indeterminate

Blank columns are all reserved space. No access is allowed.

NOTES:

- Addresses 02A0₁₆ to 02BF₁₆ are switched its function in the BANKSEL bit of the C1CLR1 register.
- Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02E0 ₁₆	XY control register	XYC	XXXX XX00 ₂
02E1 ₁₆			
02E2 ₁₆			
02E3 ₁₆			
02E4 ₁₆	UART1 special mode register 4	U1SMR4	00 ₁₆
02E5 ₁₆	UART1 special mode register 3	U1SMR3	00 ₁₆
02E6 ₁₆	UART1 special mode register 2	U1SMR2	00 ₁₆
02E7 ₁₆	UART1 special mode register	U1SMR	00 ₁₆
02E8 ₁₆	UART1 transmit/receive mode register	U1MR	00 ₁₆
02E9 ₁₆	UART1 baud rate register	U1BRG	XX ₁₆
02EA ₁₆	UART1 transmit buffer register	U1TB	XX ₁₆
02EB ₁₆			XX ₁₆
02EC ₁₆	UART1 transmit/receive control register 0	U1C0	0000 1000 ₂
02ED ₁₆	UART1 transmit/receive control register 1	U1C1	0000 0010 ₂
02EE ₁₆	UART1 receive buffer register	U1RB	XX ₁₆
02EF ₁₆			XX ₁₆
02F0 ₁₆			
02F1 ₁₆			
02F2 ₁₆			
02F3 ₁₆			
02F4 ₁₆	UART4 special mode register 4	U4SMR4	00 ₁₆
02F5 ₁₆	UART4 special mode register 3	U4SMR3	00 ₁₆
02F6 ₁₆	UART4 special mode register 2	U4SMR2	00 ₁₆
02F7 ₁₆	UART4 special mode register	U4SMR	00 ₁₆
02F8 ₁₆	UART4 transmit/receive mode register	U4MR	00 ₁₆
02F9 ₁₆	UART4 baud rate register	U4BRG	XX ₁₆
02FA ₁₆	UART4 transmit buffer register	U4TB	XX ₁₆
02FB ₁₆			XX ₁₆
02FC ₁₆	UART4 transmit/receive control register 0	U4C0	0000 1000 ₂
02FD ₁₆	UART4 transmit/receive control register 1	U4C1	0000 0010 ₂
02FE ₁₆	UART4 receive buffer register	U4RB	XX ₁₆
02FF ₁₆			XX ₁₆
0300 ₁₆	Timer B3,B4,B5 count start flag	TBSR	000X XXXX ₂
0301 ₁₆			
0302 ₁₆	Timer A1-1 register	TA11	XX ₁₆
0303 ₁₆			XX ₁₆
0304 ₁₆	Timer A2-1 register	TA21	XX ₁₆
0305 ₁₆			XX ₁₆
0306 ₁₆	Timer A4-1 register	TA41	XX ₁₆
0307 ₁₆			XX ₁₆
0308 ₁₆	Three-phase PWM control register 0	INVC0	00 ₁₆
0309 ₁₆	Three-phase PWM control register 1	INVC1	00 ₁₆
030A ₁₆	Three-phase output buffer register 0	IDB0	XX11 1111 ₂
030B ₁₆	Three-phase output buffer register 1	IDB1	XX11 1111 ₂
030C ₁₆	Dead time timer	DTT	XX ₁₆
030D ₁₆	Timer B2 interrupt generating frequency set counter	ICTB2	XX ₁₆
030E ₁₆			
030F ₁₆			

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Address	Register	Symbol	Value after RESET
0310 ₁₆ 0311 ₁₆	Timer B3 register	TB3	XX ₁₆ XX ₁₆
0312 ₁₆ 0313 ₁₆	Timer B4 register	TB4	XX ₁₆ XX ₁₆
0314 ₁₆ 0315 ₁₆	Timer B5 register	TB5	XX ₁₆ XX ₁₆
0316 ₁₆			
0317 ₁₆			
0318 ₁₆			
0319 ₁₆			
031A ₁₆			
031B ₁₆	Timer B3 mode register	TB3MR	00XX 0000 ₂
031C ₁₆	Timer B4 mode register	TB4MR	00XX 0000 ₂
031D ₁₆	Timer B5 mode register	TB5MR	00XX 0000 ₂
031E ₁₆			
031F ₁₆	External interrupt cause select register	IFSR	00 ₁₆
0320 ₁₆			
0321 ₁₆			
0322 ₁₆			
0323 ₁₆			
0324 ₁₆	UART3 special mode register 4	U3SMR4	00 ₁₆
0325 ₁₆	UART3 special mode register 3	U3SMR3	00 ₁₆
0326 ₁₆	UART3 special mode register 2	U3SMR2	00 ₁₆
0327 ₁₆	UART3 special mode register	U3SMR	00 ₁₆
0328 ₁₆	UART3 transmit/receive mode register	U3MR	00 ₁₆
0329 ₁₆	UART3 baud rate register	U3BRG	XX ₁₆
032A ₁₆ 032B ₁₆	UART3 transmit buffer register	U3TB	XX ₁₆ XX ₁₆
032C ₁₆	UART3 transmit/receive control register 0	U3C0	0000 1000 ₂
032D ₁₆	UART3 transmit/receive control register 1	U3C1	0000 0010 ₂
032E ₁₆ 032F ₁₆	UART3 receive buffer register	U3RB	XX ₁₆ XX ₁₆
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆	UART2 special mode register 4	U2SMR4	00 ₁₆
0335 ₁₆	UART2 special mode register 3	U2SMR3	00 ₁₆
0336 ₁₆	UART2 special mode register 2	U2SMR2	00 ₁₆
0337 ₁₆	UART2 special mode register	U2SMR	00 ₁₆
0338 ₁₆	UART2 transmit/receive mode register	U2MR	00 ₁₆
0339 ₁₆	UART2 baud rate register	U2BRG	XX ₁₆
033A ₁₆ 033B ₁₆	UART2 transmit buffer register	U2TB	XX ₁₆ XX ₁₆
033C ₁₆	UART2 transmit/receive control register 0	U2C0	0000 1000 ₂
033D ₁₆	UART2 transmit/receive control register 1	U2C1	0000 0010 ₂
033E ₁₆ 033F ₁₆	UART2 receive buffer register	U2RB	XX ₁₆ XX ₁₆

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Address	Register	Symbol	Value after RESET
0340 ₁₆	Count start flag	TABSR	00 ₁₆
0341 ₁₆	Clock prescaler reset flag	CPSRF	0XXX XXXX ₂
0342 ₁₆	One-shot start flag	ONSF	00 ₁₆
0343 ₁₆	Trigger select register	TRGSR	00 ₁₆
0344 ₁₆	Up-down flag	UDF	00 ₁₆
0345 ₁₆			
0346 ₁₆ 0347 ₁₆	Timer A0 register	TA0	XX ₁₆ XX ₁₆
0348 ₁₆ 0349 ₁₆	Timer A1 register	TA1	XX ₁₆ XX ₁₆
034A ₁₆ 034B ₁₆	Timer A2 register	TA2	XX ₁₆ XX ₁₆
034C ₁₆ 034D ₁₆	Timer A3 register	TA3	XX ₁₆ XX ₁₆
034E ₁₆ 034F ₁₆	Timer A4 register	TA4	XX ₁₆ XX ₁₆
0350 ₁₆ 0351 ₁₆	Timer B0 register	TB0	XX ₁₆ XX ₁₆
0352 ₁₆ 0353 ₁₆	Timer B1 register	TB1	XX ₁₆ XX ₁₆
0354 ₁₆ 0355 ₁₆	Timer B2 register	TB2	XX ₁₆ XX ₁₆
0356 ₁₆	Timer A0 mode register	TA0MR	0000 0X00 ₂
0357 ₁₆	Timer A1 mode register	TA1MR	0000 0X00 ₂
0358 ₁₆	Timer A2 mode register	TA2MR	0000 0X00 ₂
0359 ₁₆	Timer A3 mode register	TA3MR	0000 0X00 ₂
035A ₁₆	Timer A4 mode register	TA4MR	0000 0X00 ₂
035B ₁₆	Timer B0 mode register	TB0MR	00XX 0000 ₂
035C ₁₆	Timer B1 mode register	TB1MR	00XX 0000 ₂
035D ₁₆	Timer B2 mode register	TB2MR	00XX 0000 ₂
035E ₁₆	Timer B2 special mode register	TB2SC	XXXX XXX0 ₂
035F ₁₆	Count source prescaler register	TCSPR	0XXX 0000 ₂
0360 ₁₆			
0361 ₁₆			
0362 ₁₆			
0363 ₁₆			
0364 ₁₆	UART0 special mode register 4	U0SMR4	00 ₁₆
0365 ₁₆	UART0 special mode register 3	U0SMR3	00 ₁₆
0366 ₁₆	UART0 special mode register 2	U0SMR2	00 ₁₆
0367 ₁₆	UART0 special mode register	U0SMR	00 ₁₆
0368 ₁₆	UART0 transmit/receive mode register	U0MR	00 ₁₆
0369 ₁₆	UART0 baud rate register	U0BRG	XX ₁₆
036A ₁₆ 036B ₁₆	UART0 transmit buffer register	U0TB	XX ₁₆ XX ₁₆
036C ₁₆	UART0 transmit/receive control register 0	U0C0	0000 1000 ₂
036D ₁₆	UART0 transmit/receive control register 1	U0C1	0000 0010 ₂
036E ₁₆ 036F ₁₆	UART0 receive buffer register	U0RB	XX ₁₆ XX ₁₆

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Address	Register	Symbol	Value after RESET
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆			
0375 ₁₆			
0376 ₁₆			
0377 ₁₆			
0378 ₁₆	DMA0 cause select register	DM0SL	0X00 0000 ₂
0379 ₁₆	DMA1 cause select register	DM1SL	0X00 0000 ₂
037A ₁₆	DMA2 cause select register	DM2SL	0X00 0000 ₂
037B ₁₆	DMA3 cause select register	DM3SL	0X00 0000 ₂
037C ₁₆	CRC data register	CRCD	XX ₁₆
037D ₁₆			XX ₁₆
037E ₁₆	CRC input register	CRCIN	XX ₁₆
037F ₁₆			
0380 ₁₆	A-D0 register 0	AD00	XXXX XXXX ₂
0381 ₁₆			0000 0000 ₂
0382 ₁₆	A-D0 register 1	AD01	XX ₁₆
0383 ₁₆			XX ₁₆
0384 ₁₆	A-D0 register 2	AD02	XX ₁₆
0385 ₁₆			XX ₁₆
0386 ₁₆	A-D0 register 3	AD03	XX ₁₆
0387 ₁₆			XX ₁₆
0388 ₁₆	A-D0 register 4	AD04	XX ₁₆
0389 ₁₆			XX ₁₆
038A ₁₆	A-D0 register 5	AD05	XX ₁₆
038B ₁₆			XX ₁₆
038C ₁₆	A-D0 register 6	AD06	XX ₁₆
038D ₁₆			XX ₁₆
038E ₁₆	A-D0 register 7	AD07	XX ₁₆
038F ₁₆			XX ₁₆
0390 ₁₆			
0391 ₁₆			
0392 ₁₆	A-D0 control register 4	AD0CON4	XXXX 00XX ₂
0393 ₁₆			
0394 ₁₆	A-D0 control register 2	AD0CON2	XX0X X000 ₂
0395 ₁₆	A-D0 control register 3	AD0CON3	XXXX X000 ₂
0396 ₁₆	A-D0 control register 0	AD0CON0	00 ₁₆
0397 ₁₆	A-D0 control register 1	AD0CON1	00 ₁₆
0398 ₁₆	D-A register 0	DA0	XX ₁₆
0399 ₁₆			
039A ₁₆	D-A register 1	DA1	XX ₁₆
039B ₁₆			
039C ₁₆	D-A control register	DACON	XXXX XX00 ₂
039D ₁₆			
039E ₁₆			
039F ₁₆			

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Address	Register	Symbol	Value after RESET
03A0 ₁₆	Function select register A8	PS8	X000 0000 ₂
03A1 ₁₆	Function select register A9	PS9	00 ₁₆
03A2 ₁₆			
03A3 ₁₆			
03A4 ₁₆			
03A5 ₁₆			
03A6 ₁₆			
03A7 ₁₆	Function select register D1	PSD1	X0XX XX00 ₂
03A8 ₁₆			
03A9 ₁₆			
03AA ₁₆			
03AB ₁₆			
03AC ₁₆	Function select register C2	PSC2	XXXX X00X ₂
03AD ₁₆	Function select register C3	PSC3	X0XX XXXX ₂
03AE ₁₆			
03AF ₁₆	Function select register C	PSC	00X0 0000 ₂
03B0 ₁₆	Function select register A0	PS0	00 ₁₆
03B1 ₁₆	Function select register A1	PS1	00 ₁₆
03B2 ₁₆	Function select register B0	PSL0	00 ₁₆
03B3 ₁₆	Function select register B1	PSL1	00 ₁₆
03B4 ₁₆	Function select register A2	PS2	00X0 0000 ₂
03B5 ₁₆	Function select register A3	PS3	00 ₁₆
03B6 ₁₆	Function select register B2	PSL2	00X0 0000 ₂
03B7 ₁₆	Function select register B3	PSL3	00 ₁₆
03B8 ₁₆			
03B9 ₁₆	Function select register A5	PS5	XXX0 0000 ₂
03BA ₁₆			
03BB ₁₆			
03BC ₁₆	Function select register A6	PS6	00 ₁₆
03BD ₁₆	Function select register A7	PS7	00 ₁₆
03BE ₁₆	Function select register B6	PSL6	00 ₁₆
03BF ₁₆	Function select register B7	PSL7	00 ₁₆
03C0 ₁₆	Port P6 register	P6	XX ₁₆
03C1 ₁₆	Port P7 register	P7	XX ₁₆
03C2 ₁₆	Port P6 direction register	PD6	00 ₁₆
03C3 ₁₆	Port P7 direction register	PD7	00 ₁₆
03C4 ₁₆	Port P8 register	P8	XX ₁₆
03C5 ₁₆	Port P9 register	P9	XX ₁₆
03C6 ₁₆	Port P8 direction register	PD8	00X0 0000 ₂
03C7 ₁₆	Port P9 direction register	PD9	00 ₁₆
03C8 ₁₆	Port P10 register	P10	XX ₁₆
03C9 ₁₆	Port P11 register	P11	XX ₁₆
03CA ₁₆	Port P10 direction register	PD10	00 ₁₆
03CB ₁₆	Port P11 direction register	PD11	XXX0 0000 ₂
03CC ₁₆	Port P12 register	P12	XX ₁₆
03CD ₁₆	Port P13 register	P13	XX ₁₆
03CE ₁₆	Port P12 direction register	PD12	00 ₁₆
03CF ₁₆	Port P13 direction register	PD13	00 ₁₆

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Address	Register	Symbol	Value after RESET
03D0 ₁₆	Port P14 register	P14	XX ₁₆
03D1 ₁₆	Port P15 register	P15	XX ₁₆
03D2 ₁₆	Port P14 direction register	PD14	X000 0000 ₂
03D3 ₁₆	Port P15 direction register	PD15	00 ₁₆
03D4 ₁₆			
03D5 ₁₆			
03D6 ₁₆			
03D7 ₁₆			
03D8 ₁₆			
03D9 ₁₆			
03DA ₁₆	Pull-up control register 2	PUR2	00 ₁₆
03DB ₁₆	Pull-up control register 3	PUR3	00 ₁₆
03DC ₁₆	Pull-up control register 4	PUR4	XXXX 0000 ₂
03DD ₁₆			
03DE ₁₆	Output port switch register	OPS	00 ₁₆
03DF ₁₆			
03E0 ₁₆	Port P0 register	P0	XX ₁₆
03E1 ₁₆	Port P1 register	P1	XX ₁₆
03E2 ₁₆	Port P0 direction register	PD0	00 ₁₆
03E3 ₁₆	Port P1 direction register	PD1	00 ₁₆
03E4 ₁₆	Port P2 register	P2	XX ₁₆
03E5 ₁₆	Port P3 register	P3	XX ₁₆
03E6 ₁₆	Port P2 direction register	PD2	00 ₁₆
03E7 ₁₆	Port P3 direction register	PD3	00 ₁₆
03E8 ₁₆	Port P4 register	P4	XX ₁₆
03E9 ₁₆	Port P5 register	P5	XX ₁₆
03EA ₁₆	Port P4 direction register	PD4	00 ₁₆
03EB ₁₆	Port P5 direction register	PD5	00 ₁₆
03EC ₁₆			
03ED ₁₆			
03EE ₁₆			
03EF ₁₆			
03F0 ₁₆	Pull-up control register 0	PUR0	00 ₁₆
03F1 ₁₆	Pull-up control register 1	PUR1	XXXX 0000 ₂
03F2 ₁₆			
03F3 ₁₆			
03F4 ₁₆			
03F5 ₁₆			
03F6 ₁₆			
03F7 ₁₆			
03F8 ₁₆			
03F9 ₁₆			
03FA ₁₆			
03FB ₁₆			
03FC ₁₆			
03FD ₁₆			
03FE ₁₆			
03FF ₁₆	Port control register	PCR	XXXX XXX0 ₂

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Package Dimensions

144P6Q-A

Plastic 144pin 20X20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP144-P-2020-0.50	-	1.23	Cu Alloy

