PEREGRINE SEMICONDUCTOR

AN11: Application Note

Replacing Qualcomm's Q3236 with Peregrine Semiconductor's PE3236

Features

- PE3236 Replaces Q3236
- Better phase noise performance
- Substantially lower power consumption

Introduction

The Peregrine PE3236 PLL was designed as a replacement for the Qualcomm Q3236 PLL, providing better phase noise performance and substantially lower power consumption.

Although every effort has been taken to make the PE3236 a drop-in replacement for the Q3236, several differences need to be addressed when changing from the Q3236 to the PE3236. This application note is intended to help designers understand these differences, allowing smooth integration and optimization of the PE3236 in their application.

Power Supply

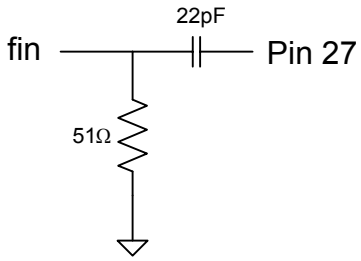
The biggest difference between the Q3236 and the PE3236 is in the operating power supply voltages. The Q3236 operates with a nominal 5-volt supply, while the PE3236 operates with a 3-volt supply. If a 3-volt supply is not available, a voltage regulator should be added to supply the PE3236 with 3 volts.

Pin Functional Considerations

Several pins require minor changes to their external circuitry. These changes (outlined below) are relatively simple, and easily accommodated in most Q3236 designs. See Table 2 for a summary of these changes.

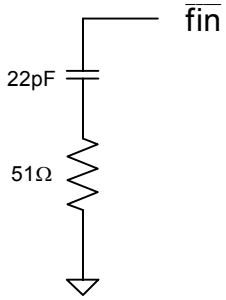
Pin 27 (f_{in})

This pin requires a change in the value of one external resistor. The Q3236 requires a series capacitor followed by a 100 Ω resistor to ground. The PE3236 requires a series capacitor followed by a 51 Ω resistor to ground:



Pin 28 ($\overline{fin}$)

The Q3236 recommends only a capacitor to ground from this pin. The PE3236 requires a capacitor and a 51 Ω resistor in series to ground:



Pin 31 (V_{DD}_f_p) & Pin 38 (V_{DD}_f_c)

On the Q3236 these pins are connected to V_{cc}. On the PE3236, they provide power to the f_c and f_p test point buffer circuits. In normal operation these test points are not used, and Pins 31 and 38 should be left open (floating) to disable the buffer circuits. Disabling these test points improves overall phase noise performance.

Pin 30 (f_p) & Pin 39 (f_c)

The VCO divided output (f_c) and reference divided output (f_p) signals are monitored on these pins. The Q3236 design will have a resistor to ground from each of these outputs when they are used.

The PE3236 will not use these pins in normal operation. Any resistors can be left in place, or the pins can be left open (floating).

Pins 36 (PD_$\overline{D}$) & 37 (PD_$\overline{U}$)

These pins provide the phase detector up/down pulses to the loop filter circuit. The Q3236 requires a 240 Ω resistor to ground. The PE3236 requires removal of this resistor. No action is required

Please note that on the PE3236 the Pin 36 & 37 designations have been reversed from the Q3236. This was done because pins 36 and 37 of the PE3236 are active low, while the Q3236 pins are active high. Switching the pin designation allows the same active loop filter circuit to be used for both parts.

Pin 41 ($\overline{REFin}$)

In Q3236 circuits Pin 41 ($\overline{REFin}$) is connected to ground through a capacitor. With the PE3236, pin 41 (GND) must be connected directly to ground.

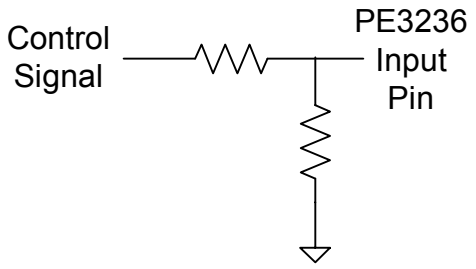
Pin 44 ($\overline{Enh}$)

Grounding Pin 44 places the Q3236 into Q3036 mode. This function is not supported in the PE3236; grounding Pin 44 enables a factory test mode. For normal operation, Pin 44 must be tied to V_{DD}.

All Digital Inputs (Pins 2-5, 7-10, 13-16, 18-22, 24-26)

The Q3236 has internal pull-down resistors on all of the digital input pins. The PE3236 does not have internal resistors, and precautions must be taken to ensure no digital inputs are allowed to float. If a pin is driven by a programming source such as a microcontroller, no action is needed. If any digital input pin is not used, it must be tied to either ground or $V_{DD.}$

The PE3236 also requires that the external control signals be a maximum of 3.3 volts. If the programming levels are greater than this (typical when using a 5-volt microcontroller), level shifting is required. This can be accomplished by using a simple resistor divider:



Phase Detector Gain

The PE3236 has a phase detector gain of 430 mV / radian, while the Q3236 gain is 302 mV / radian. This difference will affect loop filter calculations, which may require changes to the active loop filter circuit. A loop filter calculation tool is available from Peregrine.

Table 1. Pin Comparisons between the PE3236 and Q3236

Pin Number	Peregrine Function	Qualcomm Function
1	3-volt Power Supply Input	5-volt Power Supply Input
2	Bit R0	Bit R0
3	Bit R1	Bit R1
4	Bit R2	Bit R2
5	Bit R3	Bit R3
6	GND	Vee (ground)
7	D0 (Parallel); M0 (Direct)	M0 (Parallel); DBUS0 (Data Bus)
8	D1 (Parallel); M1 (Direct)	M1 (Parallel); DBUS1 (Data Bus)
9	D2 (Parallel); M2 (Direct)	M2 (Parallel); DBUS2 (Data Bus)
10	D3 (Parallel); M3 (Direct)	M3 (Parallel); DBUS3 (Data Bus)
11	V_{DD}	Vcc
12	V_{DD}	Vcc
13	S_WR (Serial; D4 (Parallel); M4 (Direct)	SEN / (Serial); M4 (Parallel); DBUS4 (Data Bus)
14	Sdata (Serial); D5 (Parallel); M5 (Direct)	SDATA / (Serial); M5 (Parallel); DBUS5 (Data Bus)
15	SClk (Serial); D6 (Parallel); M6 (Direct)	SCLK / (Serial); M6 (Parallel); DBUS6 (Data Bus)
16	FSELS (Serial); D7 (Parallel); $\overline{\text{Pre-en}}$ (Direct)	FSELS / (Serial); $\overline{\text{PRE\_EN}}$ (Parallel); DBUS7 (Data Bus)
17	GND	Vee (ground)
18	FSELP (Parallel); A0 (Direct)	FSELP (Data Bus); A0 (Parallel)
19	E_WR (Serial); A1 (Direct)	A1 (Parallel)
20	M2_WR (Parallel); A2 (Direct)	M2 WR (Data Bus); A2 (Parallel)
21	Smode (Serial, Parallel); A3 (Direct)	SMODE (Data Bus); A3 (Parallel)
22	$\overline{\text{Bmode}}$	$\overline{\text{BUSMODE}}$
23	V_{DD}	Vcc
24	M1_WR (Parallel)	M1 WR
25	A_WR (Parallel)	A WR
26	Hop_WR (Serial, Parallel)	HOP WR (Serial, Data Bus)
27	fin	VCO IN
28	$\overline{\text{fin}}$	$\overline{\text{VCO\_IN}}$
29	GND	Vee (ground)
30	f_p	VCO DIV
31	$V_{DD}\_f_p$	Vcco1
32	Dout (Serial, Parallel)	N/C
33	V_{DD}	Vcc
34	Cext	CEXT
35	V_{DD}	Vcc
36	PD_$\overline{\text{D}}$	PD U
37	PD_$\overline{\text{U}}$	PD D
38	$V_{DD}\_f_c$	Vcco2
39	f_c	REF DIV
40	GND	Vee (ground)

Pin Number	Peregrine Function	Qualcomm Function
41	GND	REF $\overline{IN}$
42	f_r	REF IN
43	LD	LD OUT
44	$\overline{Enh}$ (Serial, Parallel)	Q3236 $\overline{MODE}$

Table 2. Pin Change Summary

Pin Number	Qualcomm	Peregrine	Solution
All Power Supply Pins	5 Volts	3 Volts	Add Voltage Regulator if necessary
Pin 28 ($\overline{fin}$)	Capacitor to GND	Capacitor and Resistor to GND	Add 51 Ω resistor
Pin 27 (fin)	Series Cap and 100 Ω to GND	Series Cap and 51 Ω to GND	Change resistor value
Pins 36 & 37	240 Ω Resistor to GND	No Resistor	Remove resistor
Pins 31 & 38	Vdd	Power supply for f_c & f_p buffer circuits	Leave pins floating
Pins 30 & 39	Output (possible resistor to GND)	Disabled test points (f_c & f_p)	No changes required
Pin 41	Capacitor to GND	Connect directly to GND	Replace capacitor with jumper
Pin 44	Q3236 mode select	Factory test mode select pin; must be tied to V_{DD}	Connect to V_{DD}
Digital Inputs	Internal pull-down resistors	No internal resistors	Connect unused pins to GND
	5-volt logic compatible	3-volt logic compatible	Add resistor divider networks
Phase Detector Gain	302 mV / radian	430 mV / radian	Adjust loop filter design

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Application Note Identification

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