DATA SHEET

PR31700
32-bit RISC microprocessor

Preliminary specification
Supersedes data of 1997 Dec 15

1998 May 13

Philips
Semiconductors

PHILIPS

SUNSTAR

商斯达电子

射频、微波、光纤、光电、通讯产品

索　　引

2003 年

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射频、微波、光纤、光电产品目录

深圳商斯达电子有限公司成立于 1992 年。公司主要服务于电子通讯、导航、电子战、雷达、广播电视、仪器等军、民用高技术市场，旨在把世界先进的微波、射频、光纤、光电产品介绍给中国的工程师，以帮助他们改进系统设计水平，跟上世界高技术产品发展的步伐。

公司现在是十几家美国、日本、欧洲著名高科技公司在华的独家代理，所提供的产品涉及微波、射频、光电元器件、部件、子系统、仪器和通讯设备，同时也为客户的产品 设计提供技术咨询，综合解决方案等相关技术服务。公司还经常和国外厂商一起访问客户，举办技术讲座等。作为保证，对所有销售的产品， 我们都有一年的质量承诺。

我们对自己的要求是：让每一个客户从商斯达得到他们想要的一切！

特价、特色现货产品种类介绍：

1、 **高频、微波、卫星、光纤、光电、电视、CATV 元器件：**晶振、VCO、连接器、PIN 开关、变容二极管、开关二极管、低噪晶体管、功率电阻及电容、放大器、功率管、MMIC、混频器、耦合器、功分器、振荡器、合成器、衰减器、滤波器、隔离器、环行器、移相器、调制解调器；

2、 **光电子元器件和组件：红外发射管、红外接收管、光电开关、光敏管、发光二极管和发光二极管组件、半导体激光二极管和激光器组件、光电探测器和光接收组件、光发射接收模块、光纤激光器和光放大器、光调制器、光开关、DWDM 用光发射和接收器件、用户接入系统光光收发器件与模块、光纤连接器、光纤跳线/尾纤、光衰减器、光纤适配器、光隔离器、光耦合器、光环行器、光复用器/转换器；**

3、 **无线收发芯片和模组、蓝牙芯片和模组；**

4、 OKI(冲电气)IC：M81C55、M82C55、MSM7512B、M6882、MSM6927、M6722、M514262 等；

5、 军品级、工业级、民品级、新特优、停产、冷门、偏难电子元器件；

6、 单片机、ASIC、DSP 和各种语音电路：四位、八位、16 位、TMS 系列、ADSP 系列、ISD 系列等；

7、 通信用电路和 MODEM IC：FX 系列、73K 系列、MSM 系列、MC145 系列等

8、 自动控制用 IC：AD、BB 公司、XTR 系列、各种传感器专用配套电路；

9、 防盗、报警、监控专用电路、传感器及配件，如：HT7610、WT8072、RE200B、KDS 系列、菲涅尔透镜等；

10、温度、湿度、计时、计步、测速、调光、游戏、报警、语音等专用芯片和模组；

11、其它各类传感器、敏感开关、变送器、仪表、执行器；

主要代理品牌：

1、Mini-Circuits

混频器，功分器/合路器，放大器，电调衰减器，数字步进衰减器，固定衰减器，负载，定向耦合器，滤波器，倍频器，限幅器，VCO，L&Q 调制解调器，相位检波器，开关，RF 阻抗变阻器

2、General Microwave Corporation

电压电流控制衰减器，数控衰减器，调制器，开关，BPSK 调制器，L&Q 矢量调制器，模拟/数字移相器，频率翻译器，介质振荡器，压控振荡器，数控振荡器，宽带毫米波器件，仪器：功率密度计，功率探头，辐射探测仪和告警计

3、Bliley Electric Company

高稳晶振，恒温晶振，压控晶振，温补晶振，AT 及 SC 切割晶体

4、Osicom Technology,Inc...(Formerly Scitep Communication)

DDS 频率综合器，线性跳频 DDS 频率综合器（DC—230MHz），DDS+PLL 频率综合器，直接模拟式频率综合器（DC—1000MHz），ALL，2—10，2—12GHz 固定分频器

5、OMNIYIG Inc.

YIG 滤波器，YIG 振荡器，YIG 倍频器，限幅器，检波器，谐波发生器，YIG 前端

6、 Norsal Export Ltd.

微波双平衡/三平衡混频器，定向耦合器，功分器，90°电桥，隔离器

7、Micronetics Wireless

噪声二极管，噪声模块，噪声标准，宽带噪声仪，可编程噪声仪

8、SSI Cable

微波半钢性、柔性电缆，稳相电缆组件，延迟线

9、 RLC Electronics，Inc.

机电开关：表面贴装开关、小型开关、带负载开关、高功率开关、转换开关，
滤波器：表面贴装滤波器、低通、高通、带通、带阻滤波器、多功器（频分器），高功率负载，定向耦合器，低频宽带功分器，宽带测试用晶体检波器，滤波器设计选型软件（可根据用户要求给出滤波器频响和外形）

10、Barry Industries,Inc.

微波射频功率电阻，负载，应用：商用，军用，宇航

11、Dielectric Laborarories Inc.

多层微波片式电容，MMIC 去耦电容，功率电容，高压电容，微波毫米波芯片电容、毫米波封装、应用：商用，军用，宇航

12、GHz Technology

射频/微波双极功率晶体管、LDMOS 晶体管
应用分类：航空电子设备，广播电视，通讯，雷达，宇航

13、ARRA Inc.

同轴器件：连续可变衰减器、固定衰减器、PIN 二极管可变衰减器、RF 短路器、隔直模块、耦合器、功分器/合成器、滤波器、线延伸器、路径模拟器、移相器、PIN 开关、负载；波导器件：转接头、衰减器、波导弯头、扭波导、直波导、耦合器、柔性波导、喇叭、移相器、压力窗（密封窗）、短路器、开关、魔 T、负载

14、 PENDEL

宽带大功率行波管，行波管放大器：0.5—2，2—4，4—8，2.5—7.5，7.5—18GHz，CW 功率 20，30，50，100，200，500 和 1000W，脉冲功率直到 2KW

15、Filtronetics Inc.

晶体，晶体滤波器，时钟晶体振荡器

16、CTT Inc.

低噪声放大器（0.5—40GHz），中功率放大器（0.5—40GHz，0.2—2W），功率放大器（0.5—41GHz，3—100W），毫米波放大器（18—40GHz），限幅放大器（0.5—18GHz），有源倍频器和三倍频器。

17、EMF System

DRO PDRO，频率综合器

18、MDL(Microwave Development Laboratories Inc.)

波导器件，包括：转接头、衰减器、波导弯头、扭波导、环型器、耦合器，检波器、双脊波导器件、法兰、滤波器、密封圈、电桥、镜像抑制混频器、隔离器、环型器、单脉冲比较器、旋转关节、负载、混频器和晶体支架、调制器、单脉冲耦合器、相位移相器、功率分配器、压力窗、单边带产生器、开关、魔T、极化波变换器、阻抗变换器、波导管

19、MicroKim

Radar 信号模拟器，高度表测试仪，频率综合器，VXI 开关矩阵，PCS 放大器，天线

20、Advanced Test Technology Inc.

数字、模拟、微波、光电自动测试仪器

Advanced Power Technology
(Worldwide)

- Diodes, Rectifiers
- FREDs
- IGBTs
- MOSFETs, Switching

AEM
(Worldwide)

- Chip Bead Arrays
- Ferrite Chip Beads
- Ferrite Chip RF Inductors
- Multilayer Ceramic Inductors
- Wirewound Chip RF Inductors

AMP
(Asia, Europe, North America)

- Adapters, RF
- Attenuators, Coaxial
- Cable & Assemblies
- Connectors, Coax
- Lightning Products (EMPs)
- Terminations

Amphenol
(Worldwide)

- Adapters, RF
- Cable & Assemblies
- Connectors, Coax

GO UP

ANADIGICS
(Worldwide)

- Amplifiers, Broadband
- Amplifiers, Drop
- Amplifiers, Return Path
- Detector Pre-Amps, Integrated
- Downconverters, Broadband
- RF Power ICs
- Switches, MMIC
- TIAs - Transimpedance Amplifiers
- Tuners, Broadband
- Unconverters, Broadband

Bussman
(Worldwide)

- Fuses

GO UP

Cornell-Dubilier
(Worldwide)

- Capacitors, Film
- Capacitors, Aluminum Electrolytic
- Capacitors, High Voltage, Snubber
- Capacitors, High Voltage, Oil Filled
- Capacitors, Mica

Draloric
(Worldwide)

- Capacitors, High Voltage, RF Ceramic

GO UP

Ericsson
(Europe, North America)

- Amplifiers
- Transistors, RF

EZ Form
(North America)

- Cable & Assemblies
- Connectors, Coax

GO UP

Ferraz
(Worldwide)

- Fuses
- Thermal Management Products

Filtronic
(Worldwide)

- Amplifiers, Low Noise & Gain Blocks
- Transistors, Phemt

GO UP

General Electric
(Worldwide)

- Capacitors, Aluminum Electrolytic
- Capacitors, Film
- Capacitors, High Voltage, Frequency Induction
- Capacitors, High Voltage, Microwave
- Capacitors, High Voltage, Oil Filled
- Capacitors, High Voltage, Snubber

GHz Technology
(Worldwide)

- Transistors, RF

GO UP

High Energy
(Worldwide)

- Capacitors, High Voltage, Frequency Induction
- Capacitors, High Voltage, Oil Filled
- Capacitors, High Voltage, RF Ceramic

Hitachi
(North America)

- IGBTs

GO UP

Huber & Suhner
(Europe, North America)

- Adapters, RF
- Antennas
- Attenuators, Coaxial
- Cable & Assemblies
- Connectors, Coax
- Lightning Products (EMPs)
- Terminations

ITT GaAsTEK
(Worldwide)

- Amplifiers
- Attenuators, MMIC
- Switches (RF)

GO UP

Jennings
(Asia, Europe, North America)

- Capacitors and Relays, High Voltage, Vacuum

Johanson Manufacturing
(Worldwide)

- Capacitors, Low Voltage, Variable

GO UP

Johnson Components
(Worldwide)

- Adapters, RF
- Cable & Assemblies
- Connectors, Coax

KDI/Triangle
(Worldwide)

- Attenuators, Coaxial
- Circulators & Isolators
- Couplers
- Resistors, RF Power
- Splitters/Combiners
- Switches (RF)
- Terminations

GO UP

LEM
(North America)

- Transducers

M/A-COM
(Europe, Asia, North America)

- Accessories, Antenna
- Amplifiers, Low Noise & Gain Blocks
- Amplifiers, RF/Microwave High Power
- Attenuators, Coaxial
- Attenuators, Digital
- Attenuators, Variable, Testboard
- Attenuators, Voltage Variable
- Bias Tees
- Capacitors, Low Voltage, Fixed
- Circulators and Isolators
- Components, Radar
- Connectors, Coaxial
- Couplers, Directional
- Couplers, Hybrid Coaxial
- Detectors, RF & Microwave
- Diodes, Gunn
- Diodes, PIN
- Diodes, Schottky
- Diodes, Varactor
- Diodes/Rectifiers
- Diplexers
- Dividers
- Doublers, Frequency
- Drivers, MMIC
- Filters, Band Pass
- Filters, Low Pass
- Inductors
- Integrated Circuits, Multi-Function
- Isolators, RF Components
- Limiters, Coaxial
- Limiters, Waveguide
- Miscellaneous RF & Microwave
- Mixers
- Modulators & Demodulators
- Modules, Hybrid Power
- Oscillators, Other
- Oscillators, Voltage-Controlled
- RF Power ICs
- Splitters, Hybrid
- Splitters/Combiners
- Splitters/Combiners, Coaxial
- Stretchers, Line
- Switches, Coaxial
- Switches, MMIC
- Terminations, Coaxial
- Test Cables, Coaxial
- Transcievers
- Transformers, RF
- Transistors, RF Power Bipolar

- Transistors, RF Power MOSFET
- Transistors, Small Signal

GO UP

MAXRAD
(Worldwide)

- Antennas
- Connectors, Coaxial

Microsemi
(North America)

- Transistors, RF

GO UP

Motorola
(Worldwide)

- Amplifiers
- Up- and Downconverters
- Mixers
- Modulations & Demodulators
- Oscillators, Voltage Controlled
- Phase Lock Loops
- Receivers
- RF Power Transistors
- RF ICs
- Synthesizers
- Transceivers
- Transistors, RF

MTE
(North America)

- Chokes/Reactors

GO UP

MTI
(Worldwide)

- Switches (RF)

National Electronics
(Worldwide)

- Assemblies & Heatsinks
- Diodes, Rectifiers
- SCRs & SCR Modules
- Thermal Management Products

GO UP

NordicVLSI
(Worldwide)

- Transceivers

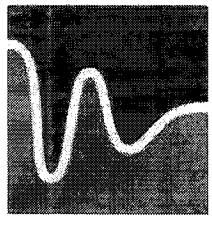
Pacific Monolithics
(Worldwide)

- Amplifiers, Low Noise & Gain Blocks
- Antennas
- Attenuators, Voltage Variable
- Oscillators, Voltage Controlled
- RF Power ICs
- Switches, MMIC

GO UP

Pacific Wireless
(Worldwide)

- Antennas



Peregrine

- Mixers
- Prescalers
- Synthesizers

- Switches

GO UP

Powerex
(North America)

- Assemblies & Heatsinks
- Diodes, Rectifiers
- Drivers, Gate
- IGBTs
- MOSFETs, Switching
- SCRs & SCR Modules

QMI
(Worldwide)

- Cable & Assemblies
- Connectors, Coax

GO UP

RF Gain
(Worldwide)

- Adapters, RF
- Amplifiers
- Attenuators, Coaxial
- Cable & Assemblies
- Circulators & Isolators
- Connectors, Coax
- Couplers
- Filters, RF
- Mixers
- Oscillators, Crystal
- Oscillators, Voltage Controlled
- Resistors, RF Power
- Splitters/Combiners
- Switches (RF)
- Synthesizers
- Terminations
- Transformers, RF
- Transistors, RF

RF Power Components
(Worldwide)

- Couplers
- Resistors, RF Power
- Splitters/Combiners
- Terminations

GO UP

Radiall
(Europe, North America)

- Attenuators, Coaxial
- Connectors, RF Coaxial
- Switches, Coaxial
- Terminations, Coaxial

SDP Components, Inc.
(Worldwide)

- Connectors, Coax

GO UP

Semelab
(Worldwide)

- Transistors, RF

Semtech
(Worldwide)

- Capacitors, High Voltage Ceramic
- Converters, DC-DC
- Diodes, Transient Voltage Suppression
- Diodes/Rectifiers
- Regulators, Voltage
- Semiconductors, Close-Out

GO UP

Siward
(Worldwide)

- Oscillators, Crystal
- Oscillators, Voltage Controlled

Spectrum Control
(Worldwide)

- Capacitors, Low Voltage, Fixed
- Connectors, Coax
- Filters, RF
- Filters & Gaskets, EMI/RFI

GO UP

Sirenza Microdevices (formerly Stanford Microdevices)
(Worldwide)

- Amplifiers, Low Noise & Gain Blocks
- RF Power ICs
- Switches, MMIC
- Transistors, GaAs Fet
- Transistors, Phemt

Stellex/Phoenix
(Worldwide)

- Amplifiers, Low Noise & Gain Blocks
- Attenuators, Coaxial
- Attenuators, Voltage Variable
- Doublers, Frequency
- Limiters, Waveguide
- Mixers
- RF Power ICs

GO UP

ST-Microelectronics
(Europe, North America)

- Amplifiers
- Transistors, RF

Times/Polyphaser
(Worldwide)

- Cable & Assemblies
- Connectors, Coax
- Lightning Products (EMPs)

TOKO
(North America, Latin America, Caribbean)

- Analog ICs
- Ceramic Filters
- Ceramic Patch Antennas
- Couplers
- Dielectric Filters
- Duplexers
- Fixed Inductors
- Helical Coil Filters
- LC Filters
- Multilayer Ceramic Inductors
- Photo Etched Chip Inductors
- Varactor Diodes
- Variable Coils

- Wirewound Chip RF Inductors

GO UP

UMS
(Worldwide)

- Amplifiers, Low Noise & Gain Blocks
- Attenuators, Voltage Variable
- Diodes, Schottky
- Dividers
- Integrated Circuits, Multi-Function
- Mixers
- Multipliers, Frequency
- Oscillators, Voltage-Controlled
- Phase Shifters
- RF Power ICs
- Switches, MMIC
- Transistors, GaAs Fet
- Transistors, Phemt

Unilator
(Worldwide)

- Capacitors, High Voltage, RF Ceramic

GO UP

United Chemi-Con, Inc.
(North America)

- Aluminum Electrolytics
- Film Capacitors
- Metal Oxide Varistors
- Multilayer Ceramic Capacitors
- Tantalum Chip Capacitors

WJ Communications
(Europe, North America)

- Amplifiers, Low Noise & Gain Blocks
- Mixers
- Transistors, GaAs Fet

GO UP

W.L. Gore
(North America)

- Filters & Gaskets, EMI/RFI

Wakefield Engineering
(North America)

- Assemblies & Heatsinks
- Thermal Management Products

WAKEFIELD ENGINEERING

HAWKER WESTCODE SEMICONDUCTORS SIDDELEY

GO UP

Westcode
(Europe)

- Diodes, Rectifiers
- SCRs & SCR Modules

常备型号 ————CATV 高频元件高频头、卫星接收机、发射机、调制器等配套元器件

PHILIPS

BGD702 BGD702D BGD704 BGD712 BGD714 BGD802 BGD804
BGD812 BGD814 BGD885 BGD902 BGD906 BGD914
BGE67BO BGE787B BGE788 BGE847BO
BGY66B BGY67A BGY68 BGY685A/04 BGY587 BGY587B BGY588N
BGY785A BGY787 BGY885A BGY885B BGY887 BGY887A BGY887B BGY888
BF904R BF998R
BFG97 BFG135 BFG403 BFG410W BFG425W BFG520/XR BFG540 BFG541 BFG591
BFR92A BFS520 BFQ34 BFQ67 BFQ135 BFQ136 BFQ270 BFQ540
BFQ18A BFQ19 1
NE592N14 74HCT14D 74HCT86D BT136 BT138 BT151

NEC

2SC2570 2SC3355 2SC3356 2SC3357 2SC4094 2SC4226 2SC4228
NE32584C NE3210S01 NE325S01 NE42484C NE76038C NE425S01 NE429M01 2SA812 2SC1623
UPB1507GV UPC1676 UPC1688 UPC2708 UPC2709T

TOSHIBA

TA1243F TA1297 TA7673P TA8637 TA8804F

MOTOROLA

BAV99 MHW6181 MHW6185 MHW6222 MHW6272 MHW6342T
MHW707 MHW7182 MHW7205C MHW7222
4N25 4N35 LM339D 74HC 4046AD
MC145106 MC145151 MC145152 MC145162 MC7805 MC7812 MC7824

AGILENT

AT41511 AT41533
MSA0611 MSA0886
INA10386 INA5082-2811 INA5082-2800 INA5082-2900 INA5082-2812
ATF10136 ATF10736 ATF13736 ATF36136
IAM81008 IAM82008
HSMS8202 HSMS2822
MSA0185 MSA1105

商斯达高频微波器件

MRF136	MRF137	MRF138	MRF139
MRF140	MRF141	MRF142	MRF143
MRF145	MRF146	MRF147	MRF148
MRF149	MRF150	MRF151	MRF152
MRF153	MRF154	MRF155	MRF156
MRF157	MRF158	MRF159	MRF160
MRF161	MRF162	MRF163	MRF164
MRF165	MRF166	MRF167	MRF168
MRF169	MRF170	MRF171	MRF172
MRF173	MRF174	MRF175	MRF176
MRF177	MRF178	MRF179	MRF180
MRF181	MRF182	MRF183	MRF184
MRF185	MRF186	MRF227	MRF237
MRF247	MRF275	MRF314	MRF392
MRF420	MRF421	MRF422	MRF426
MRF450	MRF454	MRF401	MRF553
MRF555	MRF557	MRF559	MRF571
MRF581	MRF607	MRF630	MRF650
MRF658	MRF4427	MRF6404	MRF6522-70
MHW6182	MHW6185	MHW7182	MHW7185
MHW707	MHW803	MHW1810-1	MHW1810-2
MHL9838	MHL9236		
MGF1323	MGF1607	BFGF97	BFG540
MGF1801	MGF2407	BFG425	BFG591
MGF2430	MGF16	BFG520	BLW76
BLW83	BLW86	BLW97	BLW98
BLT278	BLV910	BLT80	BLT81
AT27LV12A90TS	2SB1204	2SC2625	2N5109
2SA1300	2SD669	2SK168	2SK 系列
3SK 系列			

常备现货型号：CATV 高频元器件、高频头、卫星接收机、发射机、调制器、微波通讯、光纤通讯等配套元器件、电信、数据通讯元器件、军工级、冷门、停产元器件

微波二极管

IT32 变容
IT33 变容
SD113 变容
BB910 变容
ISV68 变容
ISV161
1N60 检波
HV-80 PIN
ISV99 PIN
ISV128 PIN
ISS86 混频
ISS106 混频
MT105
MV2105

射频管 功率器件

KPSH10 1.1G
C1906 UHF 1.1G
C1907 UHF 1.1G
C1215 1.2G
C1923 500M
C2026 2G
C2570 5G
LP1001 1.2G
C2369 4.5G
C3355 6.5G
C3356 7G
C3358 7G
C4226
BFR91A. BFR96S
BFR96S（飞利浦）
A0686 放大 惠普
A0886 放大 惠普
AT41511 2.4G
MRF571 8G1W
MRF581 5G2.5W
MRF586
MRF587 5.5G10W
BFW16 1.3G1.5W
2N5179 1G
2N5109 1.5G2.5W
BFQ34 4G2。5W
BFQ347
P3 2.2G 2.5W 功放
DC7 前置放大
MRF9282 900M 功放
MRF136
MRF151G 175M40A500W
BLF278 175M40A500W
MRF233 90M3.5A50W
MRF247 175M20A250W
BLV75/12 175M20A250W
MRF317 200M12A270W
MRF392A

高频场效应管

2SK596 单栅
2SK168 单栅
2SK192A 单栅
2SK241 单栅
BFR964S 双栅
BFR966S 双栅
3SK74 双栅
3SK80 双栅
3SK122 3SK123 双栅
3SK131 双栅

三菱功放模块

M57704L 400-420M 13W
M57704H 450-470M 13W
M57706 145-175M 10W
M57710A 156-160M 30W
M57715 144-148M 13W
M57719 145-175M 14W
M57721L 350-400M 7W
M57721M 400-450M 7W
M57726 144-148M 46W
M57729EL 335-360M 30W
M57729L 400-420M 30W
M57729H 450-470M 33W
M57729UL 470-490M 30W
M57732 135-150M 8 W
M57741UL 135-148M 28 W
M57741L 148-160M 28W
M57741M 156-168M 28W
M57752 430-450M 13W
M57774 220-225M 30W
M57788L 400-430M 40W
M57788M 430-450M 45W
M57788H 450-470M 40W
M57789 889-915M 12W
M57796MA 144-148M 8W
M57797MA 430-450M 8W
M57797H 450-470M 8W
M67702 150-175M 60W
M67723 220-225M 8W
M67741L 136-160M 30W
M67741H 150-175M 30W
M67743H 77-88M 7W
M67748L 135-150M 8W
M67748H 150-175M 8W
M67749L 400-430M 8W
M67749H 400-470M 8W
M67781L 135-160M 40W
M67781H 150-175M 40W
AV-21H 150-175M 30W
AV-21L 136-160M 30W
M67776H 896-941M 5W
M67799MA 430-460M 8W
M68702L 135-160M 60W
M68703HA 440-470M 50W
M68706 250-270M 30W
M68706H 300-308M 20W
M68707L 250-270M 7W
M68710EL 290-330M 2W
M68711 889-915M 3.8W
M68729M 220-245M 30W
M68732SL 330-380M 7W
M68732SH 490-512M 7W
M68745L 806-870M 3.8W
M68745H 896-941M 3.8W
S-AV17 144-148M 60W
PF0310 135-150M 8W
PF0311 150-175M 8W
PF0341A 400-430M 8W
MHW803-3 870-905M 3W

传真机电路

M51997P
M51978P
M51995P
M54523
M54519
M54566

三菱高频发射管

C1162 2.5A10W37M
C1239 4A10W27M
C2314 1A5W37M
C1945 6A20W30M
C1946A 7A50W175M
C1947 1A10W175M
C1969 6A20W30M
C1970 0.6A5W175M
C1971 2A13W175M
C1972 4A25W175M
C2053 0.3A0.6W175M
C2078 3A10W30M
C2131 0.6A4W520M
C2237 2A20W175M
C2407 0.2A0.6W500M
C2538 0.4A3W175M
C2539 4A35W175M
C2630 14A100W175M
C2694 20A140W175M
C2904 22A200W37M
C2905 15A12W520M
C3022 7A50W520M
C3101 1A10W520M
C3102 18A170W520M
C3133 6A20W30M
C3240 25A270W30M

遥控编译码电路

VD5012/VD5013/VD5014
VD5026/VD5027/VD5028
PT2240/PT2260
PT2262
PT2262 贴片
PT2262-TR/S 红外
PT2272L4 锁存输出
PT2272L4 贴片
PT2272M4 暂存输出
PT2272M4 贴片
PT2272-L6
PT2272M6
PT2272M6 贴片
HT12C 2 址 10 数据
HT12D 8 址 4 数据
HT12E 12 址 1 数据
HT12F
UM3758-108A 编解码一体
UM3758-108AM 贴片

霍尔磁敏元件

A3045LU
UGN3102U
UGN3140EU UNG3144EU
UGN2981A UNG2916LB
UGN3119U
UGN3175 UNG3172
SS411A SS413A SS443A
HAL6851
UGN3501 UGN3503
UGN3505 UGN3506

CATV 模块

BGY588/587
BGY88
BGY787/BGY788
BGY702D
MHW6342
MHW7272

分频器 频率合成

MC12013
MC12016
MC12019
MC12022A
MC12022TSA 贴片
MC12022A 贴片
MC12032A
MB501 1。G 分频器
MB501L 1。1G 贴片
MB1502F
MB1504L 频率合成
MB1505PF 600M
MB1506F
MB1508F
MB1511F
MB1519PF
MC145151P 频率合成
MC145151DW
MC145152P 频率合成
MC145152DW
MC145162DW
MC145145P 频率合成
MC145146 频率合成
MC145106P 频率合成
LMX2337 500/550M 频率合成
UPB562 分频器
UPB569C 分频器
UPB571C 分频器
MC145166 锁相环
MC145168 锁相环
MC145170D 锁相环

混频器 振荡器

MC1648 振荡器
NE602 500M 混频
NE605 SA605 SA615

高频通信电路

UPC1676 天线放大
TA7673 调制器
FX469 FFSK 调制解调
BA4116FN
TC8832 语音
TDA5666
MC1377 彩色编码
MC2831 调频发射
MC2833 调频发射
BA1404 调频发射
BA1404F 贴片
MC145162DW
MC3357P 调频中频
MC3361 调频中频
MC3362 调频接收
MC3363DW 调频接收
MC3367DW 调频接收
MC3371P 调频接收
TDA7010T 调频接收
TDA7021T 调频接收
TDA7040 立体声解码
TDA7050 立体声放大
TDA7050 贴片
TDA7088T 调频接收
CX20106A 功放
TA7376 功放
NE571C 扩展
MC33110P 压扩
MC33110D 压扩

DTMF 发生器

HT9170 串行
HT9200A 贴片
HT9170B 串行/并行

DTMF 接受清单

HT9170 三态有效
HT9170B 数据
HT9170B 输出信号

DTMF 编解码

MC14546
CM8870PI
MT8870CE
MT8880
TCM5087
TP5088
TP5088WM
UM3750

红外遥控接收电路

SC9148A 发射
SC9149A 接收
SC9150A 接收
BA5104 BA5204
CX20106
SM5021B 8 通道 发射
SM5032B 8 通道 接收
SM5022 10 通道
SM5033A10 通道

低功耗三端稳压管

HT1015 1.5V
HT1030 3V
HT1033 3.3V
HT1036 3.6V
HT1038 3.8V
HT1044 4.4V
HT1050/7150A 5V
HT7260 6V
HT1070 7V
HT7280 8V
HT7190 9V
HT71C0 12V

高频声表面谐振器

150MHZ
229、325MHZ
265MHZ
303、825MHZ
310MHZ
315MHZ
418MHZ
423.22MHZ
433.92MHZ
535.25MHZ
607.25MHZ
615MHZ

高频声表滤波

138.5MHZ 窄带
315MHZ 窄带
418MHZ
420.62MHZ
433.92MHZ 窄带
479.5MHZ
480MHZ 图像稳频
903MHZ
927MHZ
可调 2-7P 电容

电话机电路

UM91214A
UM91214C
UM91215A
UM91215B
UM91215C
UM91260A
MC34014
MC34018
MC34114
MC34119
HM9110
HM9102C
HM9102D
HM9114
HM9121C
HM91510A
HM91510B
HM91550A
HM91550B
HM91560A
TEA1062
TEA1062A
KA2410
LS1240A
W91312A
W91314A
W91330 W91330A
W91340
W91350
W91351
W91530
W91531

HOLTEK

HT9302D HT9302G
HT9305D
HT9312
HT9315
HT9246DL
HT24LC01/01/04
HT24LC08/16
HT93LC46/56/66
HT27PC512
HT1300/A/B/C
HT1301A
HT1315
HT1330 HT1340
HT1350
HT1370 HT1380
HT1504
HT7606 HT7610
HT7620 HT7630
HT2030 HT2040A
HT2111L
HT2021

发声 IC

PT010 单音警报 8P
RT0618 6 音警报
RT0302 门钟声
UM66T 音乐管

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32-bit RISC microprocessor PR31700

GENERAL DESCRIPTION

The PR31700 is a single-chip digital ASSP (Application Specific Stand Product) used in HPCs (Handheld Personal Computers), Palm-size PCs, Screenphones, Smartphones, and other vertical market applications in the mobile computing and communication markets. The PR31700 consists of system support logic, integrated with the PR3901 Processor Core designed by Philips Semiconductors.

FEATURES

- R3000A-based PR3901 Processor Core
  - RISC architecture developed by MIPS Technologies, Inc.
  - Philips has added its own multiply-add and branch-likely instructions.
  - A single-cycle multiply/accumulate module to allow integrated DSP functions, such as a software modem for high-performance standard data and fax protocols
  - Instruction cache: 4K bytes; data cache: 1K bytes
  - On-chip Translation Lookaside Buffer (TLB) with 3264-bit wide entries, each of which maps 4KByte page Max 75MHz operation
- Built-in peripheral circuit
  - Clock generator with built-in eightfold-frequency phase-locked loop (PLL)
  - Four-stage write buffer
  - A high performance and flexible Bus Interface Unit
  - Multiple DMA channels
  - Memory controller for DRAM, HDRAM, SDRAM, SRAM, ROM, Flash Memory and PCMCIA
  - Power management unit
  - Big / Little endian
- Low power dissipation
  - 3.3V operation
  - Standby Current 10A(typ)
  - CPU clock stop mode
  - Power down modes for individual internal peripheral modules
- Plastic LQFP 208-pin package

SYSTEM CONFIGURATION

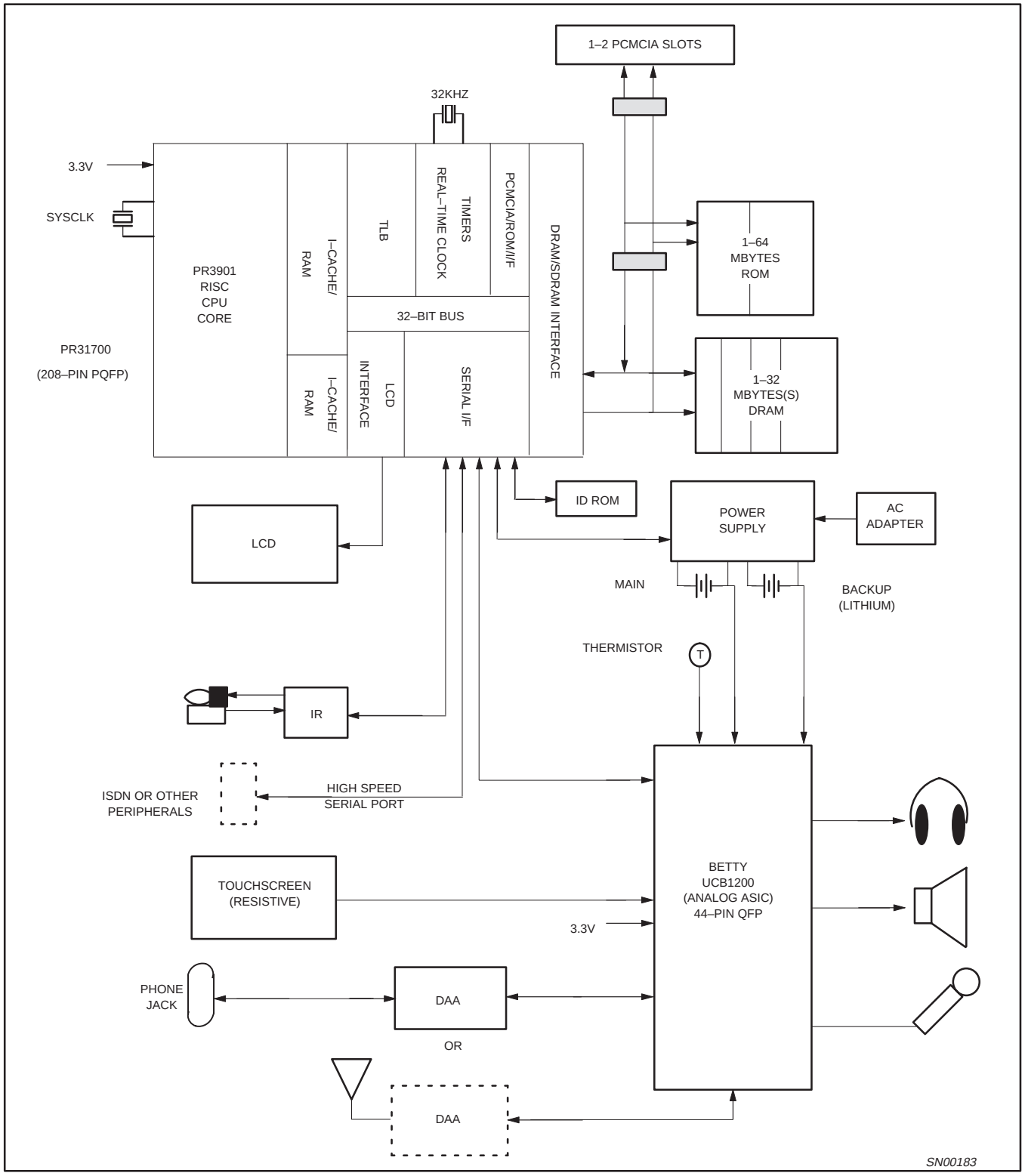


Figure 1. System Block Diagram

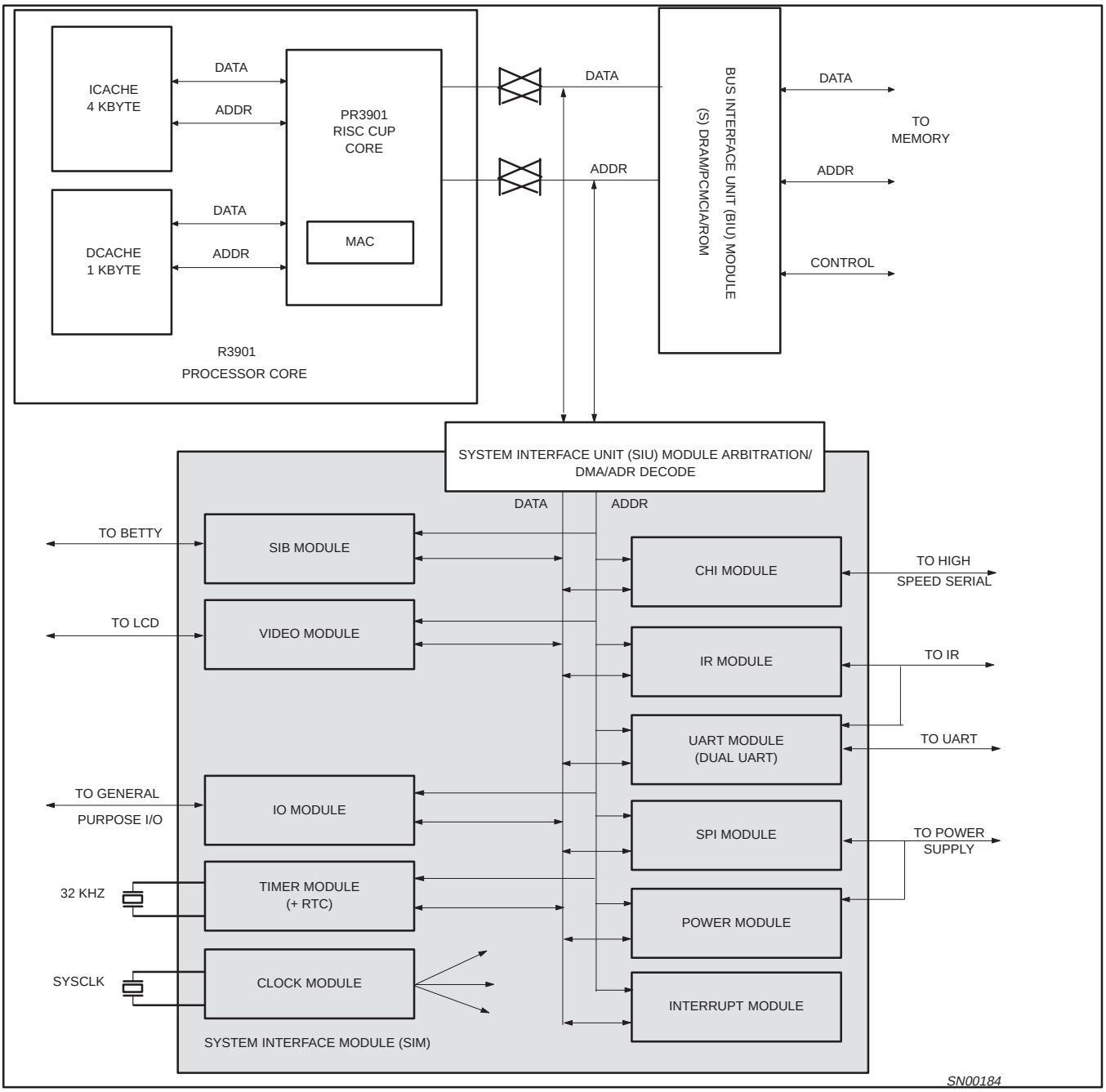


Figure 2. PR31700 Block Diagram

MEMORY CONNECTIONS

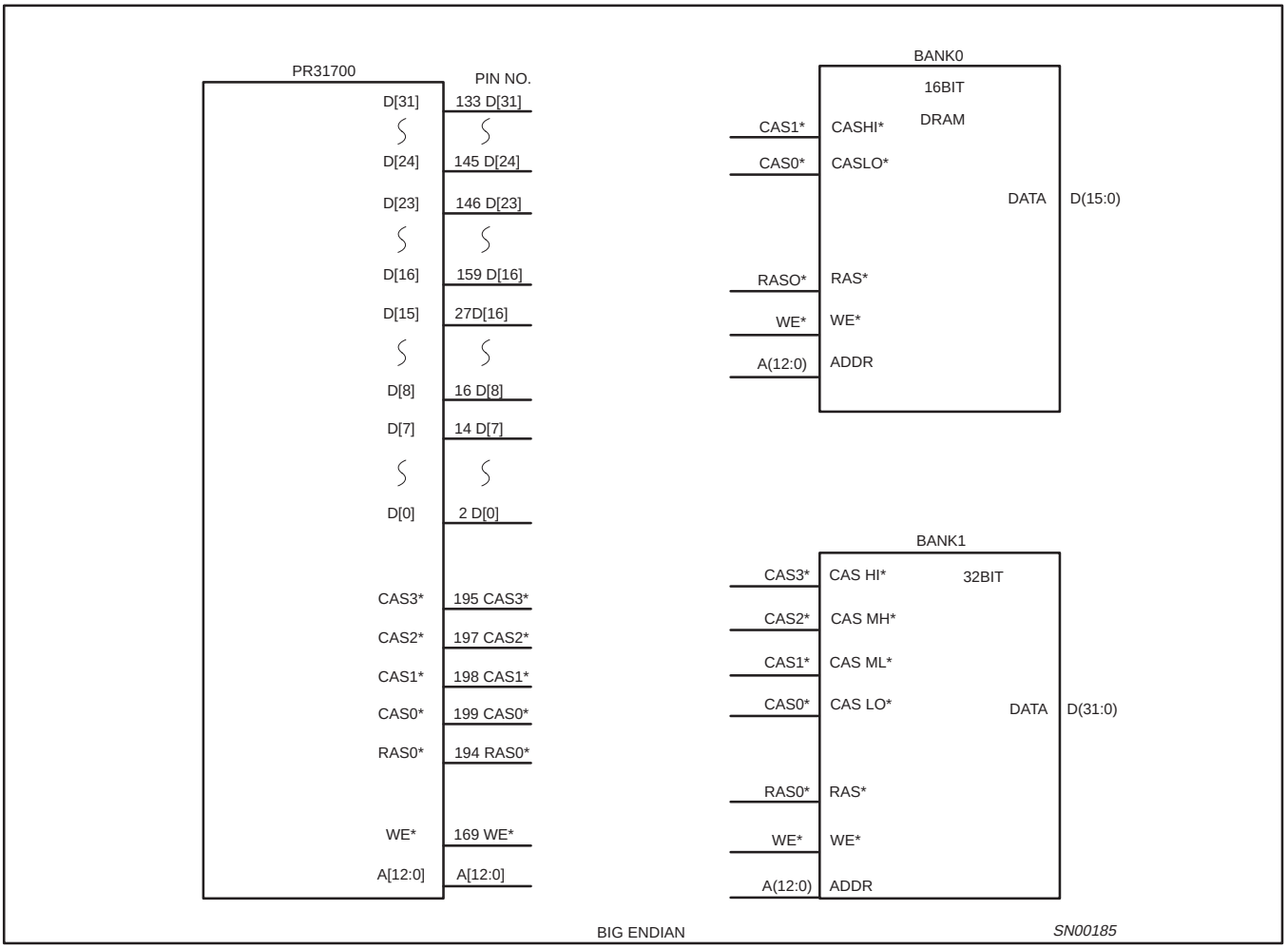


Figure 3. Memory Connections

PIN ASSIGNMENTS

NO.	I/O	SIGNAL NAME	NO.	I/O	SIGNAL NAME	NO.	I/O	SIGNAL NAME
1		VDD	41	I	SIBDIN	81		VSS
2	I/O	D[0]	42	O	SIBDOUT	82	O	PWRCS
3		VSS	43		VDD	83	I	PWRINT
4	I/O	D[1]	44	I	SIBIRQ	84	I	PWROK
5	I/O	D[2]	45	I/O	MIOX[0]	85		NC
6		VDD	46	I/O	IO[6]	86	I	ONBUTN
7	I/O	D[3]	47	I/O	IO[5]	87	I	PON[1]
8		VSS	48		VSS	88	I	CPURES*
9	I/O	D[4]	49	I/O	CHICLK	89		VDD
10		VDD	50	I/O	CHIFS	90	O	DISPON
11	I/O	D[5]	51	I	CHIDIN	91	O	FRAME
12	I/O	D[6]	52	O	CHIDOUT	92		VSS
13		VSS	53		VDD	93	O	DF
14	I/O	D[7]	54	I	RXD	94	O	LOAD
15		VSS	55	O	TXD	95	O	CP
16	I/O	D[8]	56	I/O	IO[4]	96		VSS
17		VDD	57		NC	97		VDD
18	I/O	D[9]	58	I	IRIN	98	O	VDAT[0]
19	I/O	D[10]	59	O	IROUT	99	O	VDAT[1]
20		VSS	60		VSS	100	O	VDAT[2]
21	I/O	D[11]	61		VDD	101	O	VDAT[3]
22		VDD	62	I	CARDET	102		VSS
23	I/O	D[12]	63	O	RXPWR	103	I/O	IO[1]
24	I/O	D[13]	64	I/O	IO[3]	104		VDD
25		VSS	65	I/O	IO[2]	105	I	CARD2WAIT[8]
26	I/O	D[14]	66		VSS	106	O	CARD2CSH*
27	I/O	D[15]	67	O	SPICLK	107	O	CARD2CSL*
28		VDD	68	I	SPIIN	108	I/O	IO[0]
29	I	ENDIAN	69	O	SPIOUT	109		VSS (PLL)
30	I/O	MIOX[1]	70		VDD	110	O	CARDIORD*
31	I	RSRV1	71	I	TESTCPU	111	O	CARDIOWR*
32	I/O	NC	72	I	TESTIN	112	O	CARDREG*
33		VSS	73	O	VIDDONE	113	I	CARD1WAIT*
34	I/O	NC	74	I	TESTAIU	114		VDD (PLL)
35		VDD	75		VSS	115	O	CARDDIR*
36		VDD	76	I	VCC3	116		VDD
37	O	SIBMCLK	77	O	BC32K	117	O	CARD1CSL*
38		VSS	78		VDD	118	O	CARD1CSH*
39	O	SIBSCLK	79	I	C32KIN	119		VSS
40	O	SIBSYNC	80	O	C32KOUT	120	O	MCS3[1]

PIN ASSIGNMENTS (Continued)

NO.	I/O	SIGNAL NAME	NO.	I/O	SIGNAL NAME	NO.	I/O	SIGNAL NAME
121	O	MCS2[2]	161	-	NC	201	-	VDD
122	O	MCS1[2]	162	O	CS0*	202	O	DCKE
123	O	MCS0[2]	163	O	RD*	203	-	VSS
124	O	CS3[2]	164	-	VSS	204	I	DCLKIN
125	O	CS2[2]	165	-	VDD	205	O	DCLKOUT
126	O	CS1[2]	166	O	DGRNT*	206	-	VDD
127	-	VDD	167	I	DREQ*	207	O	DQMH
128	I	SYSCLKIN	168	O	ALE	208	O	DQML
129	O	SYSCLKOUT	169	O	WE*			
130	-	VSS	170	-	VDD			
131	-	VSS	171	I/O	A[12]			
132	-	VDD	172	I/O	A[11]			
133	I/O	D[31]	173	-	VSS			
134	I/O	D[30]	174	I/O	A[10]			
135	-	VSS	175	I/O	A[9]			
136	I/O	D[29]	176	-	VDD			
137	-	VDD	177	I/O	A[8]			
138	I/O	D[28]	178	I/O	A[7]			
139	I/O	D[27]	179	-	VSS			
140	-	VSS	180	I/O	A[6]			
141	I/O	D[26]	181	I/O	A[5]			
142	-	VSS	182	-	VDD			
143	I/O	D[25]	183	I/O	A[4]			
144	-	VDD	184	-	VSS			
145	I/O	D[24]	185	I/O	A[3]			
146	I/O	D[23]	186	I/O	A[2]			
147	-	VDD	187	-	VDD			
148	I/O	D[22]	188	I/O	A[1]			
149	-	VSS	189	I/O	A[0]			
150	I/O	D[21]	190	-	VSS			
151	-	VDD	191	-	VSS			
152	I/O	D[20]	192	O	DCS0*			
153	I/O	D[19]	193	O	RAS1[8]			
154	-	VSS	194	O	RAS0*			
155	I/O	D[18]	195	O	CAS3* (CAS0*)			
156	-	VDD	196	-	VDD			
157	I/O	D[17]	197	O	CAS2* (CAS1*)			
158	-	VSS	198	O	CAS1* (CAS2[8])			
159	I/O	D[16]	199	O	CAS0[8] (CAS3*)			
160	-	VDD	200	-	VSS			

PIN FUNCTIONS

NAME	I/O	FUNCTIONS
Memory Pins		
D(31:0)	I/O	These pins are the data bus for the system. 8-bit SDRAMs should be connected to bits 7:0 and 16-bit SDRAMs and DRAMs should be connected to bits 15:0. All other 16-bit ports should be connected to bits 31:16. Of course, 32-bit ports should be connected to bits 31:0. These pins are normally outputs and only become inputs during reads, thus no resistors are required since the bus will only float for a short period of time during bus turn-around.
A(12:0)	O	These pins are the address bus for the system. The address lines are multiplexed and can be connected directly to SDRAM and DRAM devices. To generate the full 26-bit address for static devices, an external latch must be used to latch the signals using the ALE signal. For static devices, address bits 25:13 are provided by the external latch and address bits 12:0 (directly connected from PR31700's address bus) are held afterward by PR31700 processor for the remainder of the address bus cycle.
ALE	O	This pin is used as the address latch enable to latch A(12:0) using an external latch, for generating the upper address bits 25:13.
RD*	O	This pin is used as the read signal for static devices. This signal is asserted for reads from /MCS3*-0*, /CS3*-0*, /CARD2CS* and /CARD1CS* for memory and attribute space, and for reads from PR31700 processor accesses if SHOWPOSEIDON is enabled (for debugging purposes).
WE*	O	This pin is used as the write signal for the system. This signal is asserted for writes to /MCS3*-0*, /CS3*-0*, /CARD2CS* and /CARD1CS* for memory and attribute space, and for writes to DRAM and SDRAM.
CAS0* (/WE0)*	O	This pin is used as the CAS signal for SDRAMs, the CAS signal for D(7:0) for DRAMs, and the write enable signal for D(7:0) for static devices.
CAS* (/WE1)*	O	This pin is used as the CAS signal for D(15:8) for DRAMs and the write enable signal for D(15:8) for static devices.
CAS2* (/WE2)*	O	This pin is used as the CAS signal for D(23:16) for DRAMs and the write enable signal for D(23:16) for static devices.
CAS3* (/WE3)*	O	This pin is used as the CAS signal for D(31:24) for DRAMs and the write enable signal for D(31:24) for static devices.
RAS0*	O	This pin is used as the RAS signal for SDRAMs and the RAS signal for Bank0 DRAMs.
RAS1* (/DCS1)*	O	This pin is used as the chip select signal for Bank1 SDRAMs and the RAS signal for Bank1 DRAMs.
DCS0*	O	This pin is used as the chip select signal for Bank0 SDRAMs.
DCKE	O	This pin is used as the clock enable for SDRAMs.
DCLKIN	I	This pin must be tied externally to the DCLKOUT signal and is used to match skew for the data input when reading from SDRAM and DRAM devices.
DCLKOUT	O	This pin is the (nominal) 73.728 MHz clock for the SDRAMs.
DQMH	O	This pin is the upper data mask for a 16-bit SDRAM configuration.
DQML	O	This pin is the lower data mask for a 16-bit SDRAM or 8-bit SDRAM configuration.
CS3–0*	O	These pins are the Chip Select 3 through 0 signals. They can be configured to support either 32-bit or 16-bit ports.
MCS3–0*	O	These pins are the Memory Card Chip Select 3 through 0 signals. They only support 16-bit ports.
CARD2CSH*,L*	O	These pins are the Chip Select signals for PCMCIA card slot 2.
/CARD1CSH*,L*	O	These pins are the Chip Select signals for PCMCIA card slot 1.
CARDREG*	O	This pin is the /REG* signal for the PCMCIA cards.
CARDIORD*	O	This pin is the /IORD* signal for the PCMCIA IO cards.
CARDIOWR*	O	This pin is the /IOWR* signal for the PCMCIA IO cards.
CARDDIR*	O	This pin is used to provide the direction control for bi-directional data buffers used for the PCMCIA slot(s). This signal will assert whenever /CARD2CSH* or /CARD2CSL* or /CARD1CSH* or /CARD1CSL* is asserted and a read transaction is taking place.
CARD2WAIT*	I	This pin is the card wait signal from PCMCIA card slot 2.
CARD1WAIT*	I	This pin is the card wait signal from PCMCIA card slot 1.

*Active-low signal

NAME	I/O	FUNCTIONS
Bus Arbitration Pins		
DREQ*	I	This pin is used to request external arbitration. If the TESTSIU signal is high and the TESTSIU function has been enabled, then once /DGRNT* is asserted, external logic can initiate reads or writes to PR31700 processor registers by driving the appropriate input signals. If the TESTSIU signal is low or the TESTSIU function has not been enabled, then PR31700 memory transactions are halted and certain memory signals will be tri-stated when /DGRNT* is asserted in order to allow an external master to access memory.
DGRNT*	O	This pin is asserted in response to /DREQ* to inform the external test logic or bus master that it can now begin to drive signals.

*Active-low signal

NAME	I/O	FUNCTIONS
Clock Pins		
SYSCLKIN	I	This pin should be connected along with SYSCLKOUT to an external crystal which is the main PR31700 clock source.
SYSCLKOUT	O	This pin should be connected along with SYSCLKIN to an external crystal which is the main PR31700 clock source.
C32KIN	I	This pin along with C32KOUT should be connected to a 32.768 KHz crystal.
C32KOUT	O	This pin along with C32KIN should be connected to a 32.768 KHz crystal.
BC32K	O	This pin is a buffered output of the 32.768 KHz clock.

NAME	I/O	FUNCTIONS
CHI Pins		
CHIFS	I/O	This pin is the CHI frame synchronization signal. This pin is available for use in one of two modes. As an output, this pin allows PR31700 to be the master CHI sync source. As an input, this pin allows an external peripheral to be the master CHI sync source and the PR31700 CHI module will slave to this external sync.
CHICLK	I/O	This pin is the CHI clock signal. This pin is available for use in one of two modes. As an output, this pin allows PR31700 to be the master CHI clock source. As an input, this pin allows an external peripheral to be the master CHI clock source and the PR31700 CHI module will slave to this external clock.
CHIDOUT	O	This pin is the CHI serial data output signal.
CHIDIN	I	This pin is the CHI serial data input signal.

NAME	I/O	FUNCTIONS
IO Pins		
IO(6:0)	I/O	These pins are general purpose input/output ports. Each port can be independently programmed as an input or output port. Each port can generate a separate positive and negative edge interrupt. Each port can also be independently programmed to use a 16 to 24 msec debouncer.
MIO(1:0)	I/O	These pins are multi-function input/output ports. Each port can be independently programmed as an input or output port, or can be programmed for multi-function use to support test signals (for debugging purposes only). Each port can generate a separate positive and negative edge interrupt. Note that 30 other multi-function pins are available for usage as multi-function input/output ports. These pins are named after their respective standard/normal function and are not listed here.

NAME	I/O	FUNCTIONS
Reset Pins		
/CPURES*	I	This pin is used to reset the CPU core. This pin should be connected to a switch for initiating a reset in the event that a software problem might hang the CPU core. The pin should also be pulled up to VSTANDBY* through an external pull-up resistor.
/PON*	I	This pin serves as the Power On Reset signal for PR31700. This signal must remain low when VSTANDBY is asserted until VSTANDBY† is stable. Once VSTANDBY is asserted, this signal should never go low unless all power is lost in the system.

†VSTANDBY—This signal provides power for the PR31700 and other components in the system that must never lose power. This signal should always be asserted if there is eithr a good Main Backup Battery, or if a Battery Charger is plugged in.

NAME	I/O	FUNCTIONS
Power Supply Pins		
ONBUTN	I	This pin is used as the On Button for the system. Asserting this signal will cause PWRCS to set to indicate to the System Power Supply to turn power on to the system. PWRCS will not assert if the PWROK signal is low.
PWRCS	O	This pin is used as the chip select for the System Power Supply. When the system is off, the assertion of this signal will cause the System Power Supply to turn VCCDRAM†† and VCC3 on to power up the system. The Power Supply will latch SPI commands on the falling edge of PWRCS.
PWROK	I	This pin provides a status from the System Power Supply that there is a good source of power in the system. This signal typically will be asserted if there is a Battery Charger supplying current or if the Main Battery is good and the Battery Door is closed. If PWROK is low when the system is powered off, PWRCS will not assert as a result of the user pressing the ONBUTN or an interrupt attempting to wake up the system. If the device is on when the PWROK signal goes low, the software will immediately shut down the system since power is about to be lost. When PWROK goes low, there must be ample warning so that the software can shut down the system before power is actually lost.
PWRINT	I	This pin is used by the System Power Supply to alert the software that some status has changed in the System Power Supply and the software should read the status from the System Power Supply to find out what has changed. These will be low priority events, unlike the PWROK status, which is a high priority emergency case.
VCC3	I	This pin provides the status of the power supply for the ROM, UCB1200, system buffers, and other transient components in the system. This signal will be asserted by the System Power Supply when PWRCS is asserted, and will always be turned off when the system is powered down.

††V_{CC}DRAM: This signal provides power for the DRAM and/or SDRAM. The supply must be off when VSTANDBY is first asserted, andremain off until the system is powered up by the assertion of PWRCS. When the software subsequently powers down the system it may choose to keep this supply on to preserve the contents of memory.

NAME	I/O	FUNCTIONS
SIB Pins		
SIBDIN	I	This pin contains the input data shifted from UCB1200 and/or external codec device.
SIBDOUT	O	This pin contains the output data shifted to UCB1200 and/or external codec device.
SIBSCLK	O	This pin is the serial clock sent to UCB1200 and/or external codec device. The programmable SIBSCLK rate is derived by dividing down from SIBMCLK.
SIBSYNC	O	This pin is the frame synchronization signal sent to UCB1200 and/or external codec device. This frame sync is asserted for one clock cycle immediately before each frame starts and all devices connected to the SIB monitor SIBSYNC to determine when they should transmit or receive data.
SIBIRQ	I	This pin is a general purpose input port used for the SIB interrupt source from UCB1200. This interrupt source can be configured to generate an interrupt on either a positive and/or negative edge.
SIBMCLK	I/O	This pin is the master clock source for the SIB logic. This pin is available for use in one of two modes. First, SIBMCLK can be configured as a high-rate output master clock source required by certain external codec devices. In this mode all SIB clocks are synchronously slaved to the main PR31700 system clock CLK2X. Conversely, SIBMCLK can be configured as an input slave clock source. In this mode, all SIB clocks are derived from an external SIBMCLK oscillator source, which is asynchronous with respect to CLK2X. Also, for this mode, SIBMCLK can still be optionally used as a high-rate master clock source required by certain external codec devices.

NAME	I/O	FUNCTIONS
SPI Pins		
SPICLK	O	This pin is used to clock data in and out of the SPI slave device.
SPIOUT	O	This pin contains the data that is shifted into the SPI slave device.
SPIIN	I	This pin contains the data that is shifted out of the SPI slave device.

NAME	I/O	FUNCTIONS
UART and IR Pins		
TXD	O	This pin is the UART transmit signal from the UART A module.
RXD	I	This pin is the UART receive signal to the UART A module.

NAME	I/O	FUNCTIONS
IROUT	O	This pin is the UART transmit signal from the UART B module or the Consumer IR output signal if Consumer IR mode is enabled.
IRIN	I	This pin is the UART receive signal to the UART B module.
RXPWR	O	This pin is the receiver power output control signal to the external communication IR analog circuitry.
CARDET	I	This pin is the carrier detect input signal from the external communication IR analog circuitry.

NAME	I/O	FUNCTIONS
Video Pins		
FRAME	O	This pin is the frame synchronization pulse signal between the Video Module and the LCD, and is used by the LCD to return it's pointers to the top of the display. The Video Module asserts FRAME after all the lines of the LCD have been shifted and transferred, producing a full frame of display.
DF	O	This pin is the AC signal for the LCD. Since LCD plasma tends to deteriorate whenever subjected to a DC voltage, the DF signal is used by the LCD to alternate the polarity of the row and column voltages used to turn the pixels on and off. The DF signal can be configured to toggle on every frame or can be configured to toggle every programmable number of LOAD signals.
LOAD	O	This pin is the line synchronization pulse signal between the Video Module and the LCD, and is used by the LCD to transfer the contents of it's horizontal line shift register to the LCD panel for display. The Video Module asserts LOAD after an entire horizontal line of data has been shifted into the LCD.
CP	O	This pin is the clock signal for the LCD. Data is pushed by the Video Module on the rising edge of CP and sampled by the LCD on the falling edge of CP.
VDAT(3:0)	O	These pins are the data for the LCD. These signals are directly connected to the LCD for 4-bit non-split displays. For 4-bit split and 8-bit non-split displays, an external register is required to demultiplex the 4-bit data into the desired 8 parallel data lines needed for the LCD.
DISPON	O	This pin is the display-on enable signal for the LCD.
VIDDONE	O	This pin is used to externally synchronize events to periods whenthe vido is not shifting.

NAME	I/O	FUNCTIONS
Endian Pin		
ENDIAN	I	This pin is used to select the endianess of the PR31700. The "1" level input sets the endianess to the big endian, while the "0" level input tot he little endian.

NAME	I/O	FUNCTIONS
Test Pins		
TESTSIU	I	This pin allows external logic to initiate read or write transactions to PR31700 registers. The TESTSIU mode is enabled by toggling this signal after the device has powered up. Once the function is enabled, if the TESTSIU pin is high when the bus is arbitrated (using /DREQ and /DGRNT), then external logic can initiate read and write transactions to PR31700 registers. This pin is used for debugging purposes only.
TESTCPU	I	This pin allows numerous internal CPU core signals to be brought to external PR31700 pins, in place of the normal signals assigned to these pins. The CPU core signals assigned to their respective pins during TESTCPU mode are vendor-dependent. The TESTCPU mode is enabled by asserting this TESTCPU signal, and this function is provided for generating test vectors for the CPU core. This pin is used for debugging purposes only.
TESTIN	I	This pin is reserved for vendor-dependent use. This pin is used for debugging purposes only.
VIDDONE	O	This signal is used to synchronize UCB1200 to read touchscreen input, when there is no video data shifted into LCD panel.

NAME	I/O	FUNCTIONS
Spare Pins		
NC5–1	No Connect	These pins are reserved for future use and should be left unconnected.
RSRV1	I	These pins are reserved for future use and should be connected to ground.

NAME	I/O	FUNCTIONS
Power Supply Pins		
V_{DD} (33 each)	V	These pins are the power pins for PR31700 and should be connected to the digital +3.3V power supply VSTANDBY.
V_{SS} (33 each)	G	These pins are the ground pins for PR31700 and should be connected to digital ground. **NOTE:** For some vendor-dependent implementations of PR31700, pin 131 may be used for a filter capacitor for the SYSCLK oscillator (capacitor connected between pin 131 and digital ground).
V_{dd} (for PLL)	V	This pin is the analog power pin for the PR31700. Keep away from other V_{DD}.
V_{SS} (for PLL)	G	This pin is the analog ground pin for the PR31700. Keep away from other V_{SS}.

PIN USAGE INFORMATION

This section contains tables summarizing various aspects of the pin usage for the PR31700. Table 1 lists the standard versus multi-function usage for each PR31700 pin, if applicable. Those signal names shown in parentheses are test signals for debugging purposes only. The column showing the multi-function select signal and reset state indicates the internal control signal used to select the multi-function mode, as well as the default configuration of each multi-function pin during reset. The "Bus Arb State" column shows which pins are tri-stated whenever the DGRNT* signal is asserted in response to a DREQ*(external bus arbitration request).

Table 1. PR31700 Standard and Multi-Function Pin Usage

PR31700 pin	Standard Function (I = input, O = output)	Multi-function	Multi-function select (Reset State: 1 = multi-function mode selected; 0 = standard function & mode selected)	Bus Arb State
D[31:0]	D[31:0] (I/O)			Hi-Z
A[12:0]	A[12:0] (I/O)			
ALE	ALE (O)			Hi-Z
RD*	RD* (O)			Hi-Z
WE*	WE* (O)			Hi-Z
CAS0* (WE0*)	CAS0* (O)			Hi-Z
CAS1* (WE1*)	CAS1* (O)			Hi-Z
CAS2* (WE2*)	CAS2* (O)			Hi-Z
CAS3* (WE3*)	CAS3* (O)			Hi-Z
RAS0*	RAS0* (O)			Hi-Z
RAS1* (DCS1*)	RAS1* (O)			Hi-Z
DCS0*	DCS0* (O)			Hi-Z
DCKE	DCKE (O)			Hi-Z
DCLKIN	DCLKIN (I)			
DCLKOUT	DCLKOUT (O)			Hi-Z
DQMH	DQMH (O)			Hi-Z
DQML	DQML (O)			Hi-Z
DREQ*	DREQ* (I)	MIO[27]	MIOSEL[27] (0)	
DGRNT*	DGRNT* (O)	MIO[26]	MIOSEL[26] (0)	
SYSCLKIN	SYSCLKIN (I)			
SYSCLKOUT	SYSCLKOUT (O)			
C32KIN	C32KIN (I)			
C32KOUT	C32KOUT (O)			
BC32K	BC32K(O)	MIO[25]	MIOSEL[25] (1)	
VDAT[3]	VDAT[3] (O)	(BERR)	IRQTEST (0)	
VDAT[2]	VDAT[2] (O)			
VDAT[1]	VDAT[1] (O)	(IRQHIGH)	IRQTEST (0)	
VDAT[0]	VDAT[0] (O)	(IRQLow)	IRQTEST (0)	
CP	CP (O)			
LOAD	LOAD (O)			
DF	DF (O)			
FRAME	FRAME (O)			

Table 1. PR31700 Standard and Multi-Function Pin Usage (Continued)

PR31700 pin	Standard Function (I = input, O = output)	Multi-function	Multi-function select (Reset State: 1 = multi-function mode selected; 0 = standard function & mode selected)	Bus Arb State
DISPON	DISPON (O)			
PWRCS	PWRCS (O)			
PWRINT	PWRINT (I)			
PWROK	PWROK (I)			
ONBUTN	ONBUTN (I)			
CPURES*	CPURES* (I)			
PON*	PON* (I)			
TXD	TXD (O)	MIO[24]	MIOSEL[24] (0)	
RXD	RXD (I)	MIO[23]	MIOSEL[23] (0)	
CS0*	CS0* (O)			Hi-Z
CS1*	CS1* (O)	MIO[22]	MIOSEL[22] (0)	
CS2*	CS2* (O)	MIO[21]	MIOSEL[21] (0)	
CS3*	CS3* (O)	MIO[20]	MIOSEL[20] (0)	
MCS0*	MCS0* (O)	MIO[19]	MIOSEL[19] (1)	
MCS1*	MCS1* (O)	MIO[18]	MIOSEL[18] (1)	
MCS2*	MCS2* (O)	MIO[17]	MIOSEL[17] (1)	
MCS3*	MCS3* (O)	MIO[16]	MIOSEL[16] (1)	
CHIFS	CHIFS (I/O)	MIO[31]	MIOSEL[31] (1)	
CHICLK	CHICLK (I/O)	MIO[30]	MIOSEL[30] (1)	
CHIDOUT	CHIDOUT (O)	MIO[29]	MIOSEL[29] (1)	
CHIDIN	CHIDIN (I)	MIO[28]	MIOSEL[28] (1)	
VCC3	VCC3 (I)			
IO6	IO6 (I/O)			
IO5	IO5 (I/O)			
IO4	IO4 (I/O)			
IO3	IO3 (I/O)			
IO2	IO2 (I/O)			
IO1	IO1 (I/O)			
IO0	IO0 (I/O)			
SPICLK	SPICLK (O)	MIO[15]	MIOSEL[15] (0)	
SPIOUT	SPIOUT (O)	MIO[14]	MIOSEL[14] (0)	
SPIIN	SPIIN (I)	MIO[13]	MIOSEL[13] (0)	
SIBSYNC	SIBSYNC (O)			
SIBDOUT	SIBDOUT (O)			
SIBDIN	SIBDIN (I)			
SIBMCLK	SIBMCLK (I/O)	MIO[12]	MIOSEL[12] (0)	

Table 1. PR31700 Standard and Multi-Function Pin Usage (Continued)

PR31700 pin	Standard Function (I = input, O = output)	Multi-function	Multi-function select (Reset State: 1 = multi-function mode selected; 0 = standard function & mode selected)	Bus Arb State
SIBSCLK	SIBSCLK (O)			
SIBIRQ	SIBIRQ (I)			
RXPWR	RXPWR (O)			
CARDET	CARDET (I)			
IROUT	IROUT (O)			
IRIN	IRIN (I)			
TESTAIU	TESTAIU (I)			
TESTCPU	TESTCPU (I)			
TESTIN	TESTIN (I)			
VIDDONE	VIDDONE (O)			
CARDREG*	CARDREG*(O) (SHOWDINO / CS*)	MIO[11]	MIOSEL[11] (1)	
CARDIOWR*	CARDIOWR* (O)	MIO[10]	MIOSEL[10] (1)	
CARDIORD*	CARDIORD* (O)	MIO[9]	MIOSEL[9] (1)	
CARD1CSL*	CARD1CSL* (O)	MIO[8]	MIOSEL[8] (1)	
CARD1SCH*	CARD1CSH* (O)	MIO[7]	MIOSEL[7] (1)	
CARD2CSL*	CARD2CSL* (O)	MIO[6]	MIOSEL[6] (1)	
CARD2CSH*	CARD2CSH* (O)	MIO[5]	MIOSEL[5] (1)	
CARD1WAIT*	CARD1WAIT* (I)	MIO[4]	MIOSEL[4] (1)	
CARD2WAIT*	CARD2WAIT* (I)	MIO[3]	MIOSEL[3] (1)	
CARDDIR*	CARDDIR* (O)	MIOX[2]	MIOSEL[2] (1)	
MIOX[1]	(MASTER)	MIOX[1]	MIOSEL[1] (1)	
MIOX[0]	(INSFETCH*)	MIOX[0]	MIOSEL[0] (1)	
ENDIAN	ENDIAN (I)			
NC[5:1]	SPARE			
RSRV1	SPARE (I)			
VDD–34 pins	+ 3.3 V			
VSS–34 pins	GND			

Table 2 lists various power-down states and conditions for each PR31700 pin. The ”Power-Down Control” column shows the conditions which trigger a power-down for each respective pin. This column also shows the reset state for each of these conditions.

The ”PON* state” column defines the state of each pin at power-on reset (PON*). This condition is defined as initial power up of the PR31700, whereby the PR31700 is initialized and the PR31700 pins are reset to the state shown in the table. This state is entered after power is applied for the very first time (VSTANDBY is turned on but VCC3 is still turned off).

The ”1st-time power-up state” column defines the state of each pin after power-up mode (RUNNING STATE) is executed for the first time. This mode is defined as VCC3 applied to the entire system and is initiated by the user pressing the ONBUTN while in the power-on reset (PON*) state. Note that the defined state of various pins for 1st-time power-up may depend on the configuration of external devices attached to these pins. After 1st-time power-up, the software could change the state of various pins to be different from those shown in the table. Thereafter, subsequent transitions from SLEEP STATE to RUNNING STATE might result in different states for these pins.

The ”power-down state” column defines the state of each pin during power-down mode (SLEEP STATE). This mode is defined as VCC3 turned off to the entire system, except for the PR31700 (RTC and interrupts alive) and any persistent memory.

Table 2. PR31700 Power-Down Pin Usage

PR31700 pin	Power-Down Control powerdown = (vccon & vcc3)* (reset state)	PON* state	1st time power-up state	power-down state
D[31:0]	MEMPOWERDOWN	Low	Low	Low
A[12:0]	MEMPOWERDOWN	Low	Low	Low
ALE		Low	Low	Low
RD*	POWERDOWN	Low	Hi	Low
WE*	MEMPOWERDOWN	Low	Low	Low
CAS0* (WE0*)	MEMPOWERDOWN	Low	Low	Low
CAS1* (WE1*)	MEMPOWERDOWN	Low	Low	Low
CAS2* (WE2*)	MEMPOWERDOWN	Low	Low	Low
CAS3* (WE3*)	MEMPOWERDOWN	Low	Low	Low
RAS0*	MEMPOWERDOWN	Low	Low	Low
RAS1* (DCS1*)	MEMPOWERDOWN	Low	Low	Low
DCS0*	MEMPOWERDOWN	Low	Low	Low
DCKE	MEMPOWERDOWN	Low	Low	Low
DCLKIN				
DCLKOUT	MEMPOWERDOWN	Low	Low	Low
DQMH	MEMPOWERDOWN	Low	Low	Low
DQML	MEMPOWERDOWN	Low	Low	Low
DREQ*	POWERDOWN & MIOPD[27] (1)	Pull-Down	In	Selectable
DGRNT*	POWERDOWN & MIOPD[26] (0)	Low	Hi	Selectable
SYSCLKIN	POWERDOWN	OSC off	OSC on	OSC off
SYSCLKOUT	POWERDOWN	OSC off	OSC on	OSC off
C32KIN		OSC on	OSC on	OSC on
C32KOUT		OSC on	OSC on	OSC on
BC32K	POWERDOWN & MIOPD[25] (1)	Pull-Down	In	Selectable
VDAT[3]	MODULE DISABLE	Low	Low	Low
VDAT[2]	MODULE DISABLE	Low	Low	Low
VDAT[1]	MODULE DISABLE	Low	Low	Low
VDAT[0]	MODULE DISABLE	Low	Low	Low
CP	MODULE DISABLE	Low	Low	Low
LOAD	MODULE DISABLE	Low	Low	Low
DF	MODULE DISABLE	Low	Low	Low
FRAME	MODULE DISABLE	Low	Low	Low
DISPON	MODULE DISABLE	Low	Low	Low
PWRCS		Low	Hi	Low
PWRINT				
PWROK				
ONBUTN				
CPURES*				
PON*				
MBUSCLK	MODULE DISABLE	Out Low	Out Low	Out Low

Table 2. PR31700 Power-Down Pin Usage (Continued)

PR31700 pin	Power-Down Control powerdown = (vccon & vcc3)* (reset state)	PON* state	1st time power-up state	power-down state
MBUSDATA	MODULE DISABLE	Out Low	Out Low	Out Low
MBUSINT				
TXD	POWERDOWN & MIOPD[24] (0)	Low	Low	Selectable
RXD	POWERDOWN & MIOPD[23] (1)	Pull-Down	In	Selectable
CS0*	POWERDOWN	Pull-Down	Hi	Pull-Down
CS1*	POWERDOWN & MIOPD[22] (1)	Pull-Down	Hi	Selectable
CS2*	POWERDOWN & MIOPD[21] (1)	Pull-Down	Hi	Selectable
CS3*	POWERDOWN & MIOPD[20] (1)	Pull-Down	Hi	Selectable
MCS0*	POWERDOWN & MIOPD[19] (0)	In	IN	Selectable
MCS1*	POWERDOWN & MIOPD[18] (0)	In	IN	Selectable
MCS2*	POWERDOWN & MIOPD[17] (0)	In	IN	Selectable
MCS3*	POWERDOWN & MIOPD[16] (0)	In	IN	Selectable
CHIFS	POWERDOWN & MIOPD[31] (1)	Pull-Down	IN	Selectable
CHICLK	POWERDOWN & MIOPD[30] (1)	Pull-Down	IN	Selectable
CHIDOUT	POWERDOWN & MIOPD[29] (1)	Pull-Down	IN	Selectable
CHIDIN	POWERDOWN & MIOPD[28] (1)	Pull-Down	IN	Selectable
VCC3	POWERDOWN	Pull-Down		Pull-Down
IO6	POWERDOWN & IOPD[6] (1)	Pull-Down	IN	Selectable
IO5	POWERDOWN & IOPD[5] (1)	Pull-Down	IN	Selectable
IO4	POWERDOWN & IOPD[4] (1)	Pull-Down	IN	Selectable
IO3	POWERDOWN & IOPD[3] (1)	Pull-Down	IN	Selectable
IO2	POWERDOWN & IOPD[2] (1)	Pull-Down	IN	Selectable
IO1	POWERDOWN & IOPD[1] (1)	Pull-Down	IN	Selectable
IO0	POWERDOWN & IOPD[0] (1)	Pull-Down	IN	Selectable
SPICLK	POWERDOWN & MIOPD[15] (0)	Low	Low	Selectable
SPIOUT	POWERDOWN & MIOPD[14] (0)	Low	Low	Selectable
SPIIN	POWERDOWN & MIOPD[13] (1)	Pull-Down		Selectable
SIBSYNC	POWERDOWN	Low	Low	Low
SIBDOUT	POWERDOWN	Low	Low	Low
SIBDIN	POWERDOWN	Pull-Down		Pull-Down
SIBMCLK	POWERDOWN & MIOPD[12] (1)	Pull-Down	IN	Selectable
SIBSCLK	POWERDOWN	Low	Low	Low
SIBIRQ	POWERDOWN	Pull-Down		Pull-Down
RXPWR	POWERDOWN	Low	Low	Low
CARDET	POWERDOWN	Pull-Down		Pull-Down
IROUT	POWERDOWN	Low	Low	Low
IRIN	POWERDOWN	Pull-Down		Pull-Down
TESTAIU				
TESTCPU				
TESTIN				
VIDDONE	MODULE DISABLE	Low	Low	Low

Table 2. PR31700 Power-Down Pin Usage (Continued)

PR31700 pin	Power-Down Control powerdown = (vccon & vcc3)* (reset state)	PON* state	1st time power-up state	power-down state
CARDREG*	POWERDOWN & MIOPD[11] (1)	Pull-Down	IN	Selectable
CARDIOWR*	POWERDOWN & MIOPD[10] (1)	Pull-Down	IN	Selectable
CARDIORD*	POWERDOWN & MIOPD[9] (1)	Pull-Down	IN	Selectable
CARD1CSL*	POWERDOWN & MIOPD[8] (1)	Pull-Down	IN	Selectable
CARD1CSH*	POWERDOWN & MIOPD[7] (1)	Pull-Down	IN	Selectable
CARD2CSL*	POWERDOWN & MIOPD[6] (1)	Pull-Down	IN	Selectable
CARD2CSH*	POWERDOWN & MIOPD[5] (1)	Pull-Down	IN	Selectable
CARD1WAIT*	POWERDOWN & MIOPD[4] (1)	Pull-Down	IN	Selectable
CARD2WAIT*	POWERDOWN & MIOPD[3] (1)	Pull-Down	IN	Selectable
CARDDIR*	POWERDOWN & MIOPD[2] (1)	Pull-Down	IN	Selectable
MIOX[1]	POWERDOWN & MIOPD[1] (0)	IN	IN	Selectable
MIOX[0]	POWERDOWN & MIOPD[0] (0)	IN	IN	Selectable
ENDIAN				
NC[5:1]				
RSRV1				
VDD–34 EACH				
VSS–34 EACH				

FUNCTION SPECIFICATIONS

OUTLINE

The PR31700 consists of system support logic, integrated with the PR3901 Processor Core designed by Philips. For details of the system support logic and the PR3901 Processor Core, refer to the PR31700 User's Manual.

PR3901 PROCESSOR CORE

The PR3901 is a Philips-developed microprocessor core based on the R3000A RISC architecture developed by MIPS Technologies, Inc.

INSTRUCTIONS

All PR3901 Processor Core instructions are 32-bit instructions. Apart from some coprocessor instructions, the instructions are upwardly compatible with the R3000A. The PR3901 Processor Core instructions can be classified into six types.

- Load and store instructions
  - Transfer data between memory and general-purpose registers.
- Computational instructions
  - These include arithmetic, logical, shift, multiply, divide, and multiply-add instructions. The multiply-add instructions are extensions to the R3000A. The multiply instructions can also be used as three-operand instructions.
- Special instructions
  - Used for system call or break point.
- Jump and branch instructions
  - Change the control flow of a program. The Branch-Likely instruction is provided as an extension to the R3000A.
- Coprocessor instructions
  - Perform operations for coprocessors. The R3000A LWCz and SWCz instructions are reserved instructions in the PR3901 Processor Core. Attempting execution generates a reserved instruction exception. Note that the COPz, CTCz and MTCz instructions are no-operation instructions, the CFCz and MFCz instructions load undefined data to general purpose registers (rt) in the PR31700.
- System control coprocessor instructions
  - Perform operations on the CP0 registers to manipulate the memory management and exception handling functions of the processor.

REGISTERS

The PR3901 Processor Core has following registers.

- 32 general purpose registers (32-bit)
- HI/LO registers
  - Hold the result of multiply and divide operation
- PC (Program Counter)
- Cause register
  - Indicates the nature of the most recent exception
- EPC (Exception Program Counter) register
  - Holds the program counter at the time the exception occurred, indicating the address where processing is to resume after the exception processing is completed.
- Status register
  - Holds the operating mode status (user mode or kernel mode), interrupt masking status, diagnosis status and other such information.
- BadVAddr (Bad Virtual Address) register
  - Holds the most recent virtual address for which a virtual address translation error occurred.
- PRId register
  - Shows the revision number of the PR3901 Processor Core.
  - Cache register
  - Controls the instruction cache (reserved) and the data cache auto-lock bits.
- Debug register
  - Control software debug exception.
- DEPC
  - Program counter for software debug exception.

MEMORY MANAGEMENT

The PR3901 Processor Core has a 4G-byte memory address space. The 4G-byte memory space consists of a 2G-byte user area and a 2G-byte kernel area. The kernel area contains a cache area and an uncache area.The PR3901 Processor Core provides a full-featured memory management unit (MMU) utilizing an on-chip Translation Lookaside Buffer (TLB). The on-chip TLB majur characteristics are :

- 32 x 64-bit wide entries
- fully associative
- 2 entry micro TLB for instruction address translation
- instruction address translation accesses full TL after micro-TLB miss
- data address translation accesses full TLB

PIPELINE

The PR3901 Processor Core pipeline consists of five stages. The pipeline configuration enables the PR3901 Processor Core to execute nearly all instructions in one clock.

CACHE

The PR31700 incorporates a 4K-byte instruction cache and a 1K-byte data cache. The instruction cache is direct-mapped with a block size of 16 bytes. The data cache uses two-way set-associative mapping with a block size of four bytes. The data cache has a lock function that locks data in one direction. The write-through method is used to write data back to memory.

DSP FUNCTION

The PR3901 Processor Core has a high-speed multiplier/accumulator and supports 32-bit multiplier operations, with 64-bit accumulator in one cycle.

PERIPHERAL FUNCTIONS

CLOCK GENERATOR

The PR31700 uses an internal PLL and an external crystal oscillator to generate a clock with eight times the input clock frequency. The PLL oscillation can be halted externally to reduce power dissipation.

WRITE BUFFER

The PR31700 incorporates a four-stage write buffer.

BUS INTERFACE UNIT (BIU) MODULE

The PR31700 has a Bus Interface Unit with the following features.

- supports 2 Banks of SDRAM and/or DRAM / HDRAM
  - 8-bit or 16-bit SDRAM configuration
  - 16-bit or 32-bit DRAM configuration
  - 16-bit or 32-bit HDRAM configuration
  - 4 Mbit, 16 Mbit and 64 Mbit parts supported
  - page mode reads and writes supported
  - independent refresh counters for each bank
  - self refreshing parts supported to retain memory when system is powered down
- 4 general purpose chip selects (CS3*–CS0*)
  - 16-bit or 32-bit ports
  - programmable wait states
  - read page mode
- 4 general purpose chip selects (MCS3*–MCS0*)
  - 16-bit ports
  - programmable wait states
  - read page mode
- 2 full PCMCIA slots
  - 16-bit ports
  - IORD and IOWR provided to support I/O cards
  - WAIT signal supported

SYSTEM INTERFACE UNIT (SIU) MODULE

The PR31700 has a System Interface Unit with the following features.

- multi-channel 32-bit DMA controller
- independent DMA controller for video, SIB to/from BETTY audio/telecom codecs, high-speed serial port, IR, UART, and general purpose UART
- address decoding for the internal registers

CLOCK MODULE

The PR31700 has a Clock Module with the following features.

- The PR31700 supports system-wide single crystal configuration, besides the 32 kHz RTC XTAL (reduces cost, power, and board space)
- common crystal rate divided to generate clock for CPU, video, sound, telecom, UARTs, etc.
- independent enabling or disabling of individual clocks under software control, for power management

CONCENTRATION HIGHWAY INTERFACE (CHI) MODULE

The PR31700 has a CHI Module with the following features.

- high-speed serial Concentration Highway Interface (CHI) contains logic for interfacing to external full-duplex serial time-division-multiplexed (TDM) communication peripherals
- supports ISDN line interface chips and other PCM/TDM serial devices
- CHI interface is programmable (number of channels, frame rate, bit rate, etc.) to provide support for a variety of formats
- supports data rates up to 4.096 Mbps
- independent DMA support for CHI receive and transmit

INTERRUPT MODULE

The PR31700 has an Interrupt Module with the following features.

- contains logic for individually enabling, reading, and clearing all PR31700 interrupt sources
- interrupts generated from internal PR31700 modules or from edge transitions on external signal pins

IO MODULE

The PR31700 has an IO Module with the following features.

- contains support for reading and writing the 7 bi-directional general purpose IO pins and the 32 bi-directional multi-function IO pins
- each IO port can generate a separate positive and negative edge interrupt
- independently configurable IO ports allow the PR31700 to support a flexible and wide range of system applications and configurations

IR MODULE

The PR31700 has an IR Module with the following features.

- IR consumer mode
  - allows control of consumer electronic devices such as stereos, TVs, VCRs, etc.
  - programmable pulse parameters
  - external analog LED circuitry
- IRDA communication mode
  - not compatible with General Magic Cap Devices
  - allows communication with other IRDA devices such as FAX machines, copiers, printers, etc.
  - supported by the UART module within the PR31700
  - external analog receiver preamp and LED circuitry
  - data rate = up to 115 kbps at 1 meter
- IR FSK communication mode
  - compatible with General Magic Cap Devices
  - supported by the UART module within the PR31700
  - external analog IR chip(s) perform frequency modulation to generate the desired IR communication mode protocol
  - data rate = up to 36000 bps at 3 meters
- carrier detect state machine
  - periodically enables IR receiver to check if a valid carrier is present

POWER MODULE
The PR31700 has a Power Module with the following features.

- power-down modes for individual internal peripheral modules
- serial (SPI port) power supply control interface supported
- power management state machine has 3 states: RUNNING, DOZING and SLEEP

SERIAL INTERCONNECT BUS (SIB) MODULE
The PR31700 has a SIB Module with the following features.

- The PR31700 contains holding and shift registers to support the serial interface to the UCB1200 ASIC and/or other optional codec devices
- synchronous, frame-based protocol
- The PR31700 always master source of clock and frame frequency and phase; programmable clock frequency
- each SIB frame consists of 128 clock cycles, further divided into 2 subframes or words of 64 bits each (supports up to 2 devices simultaneously)
- independent DMA support for audio receive and transmit, telecom receive and transmit
- supports 8-bit or 16-bit mono telecom formats
- supports 8-bit or 16-bit mono or stereo audio formats
- independently programmable audio and telecom sample rates
- CPU read/write registers for subframe control and status

SERIAL PERIPHERAL INTERFACE (SPI) MODULE
The PR31700 has an SPI Module with the following features.

- provides interface to SPI peripherals and devices
- full-duplex, synchronous serial data transfers (data in, data out, and clock signals)
- The PR31700 supplies dedicated chip select and interrupt for an SPI interface serial power supply
- 8-bit or 16-bit data word lengths for the SPI interface
- programmable SPI baud rate

TIMER MODULE
The PR31700 has a Timer Module with the following features.

- Real Time Clock (RTC) and Timer
- 40-bit counter (30.517 s granularity); maximum uninterrupted time = 388.36 days
- 40-bit alarm register (30.517 s granularity)
- 16-bit periodic timer (0.868 s granularity); maximum timeout = 56.8 ms
- interrupts on alarm, timer, and prior to RTC roll-over

UART MODULE
The PR31700 has a UART Module with the following features.

- 2 independent full-duplex UARTs
- programmable baud rate generator
- UART A port used for serial control interface to external IR module
- UART B port used for general purpose serial control interface
- UART A and UART B DMA support for receive and transmit

VIDEO MODULE
The PR31700 has a Video Module with the following features.

- bit-mapped graphics
- supports monochrome, grey scale, or color modes
- time-based dithering algorithm for gray scale and color modes
- supports multiple screen sizes
- supports split and non-split displays
- variable size and relocatable video buffer
- DMA support for fetching image data from video buffer

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0 V (GND)

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	Power supply voltage	V_{SS} – 0.5 to 4.5	V
V_{IN}	Input voltage	V_{SS} – 0.5 to V_{DD} + 0.5	V
T_{stg}	Storage temperature range	–55 to +125	°C
Pd	Maximum dissipation (T_{amb} = 70°C)	1	W

NOTE:

1. Using an LSI at specifications higher than the maximum ratings can cause permanent damage to the LSI. For normal operation, use under the recommended operating conditions. Exceeding the recommended operating conditions may affect the reliability of the LSI.

RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0 V (GND)

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
V_{DD}	Power supply voltage	3.0	3.3	3.6	V
T_{opr}	Operating temperature range	0	–	70	°C

DC CHARACTERISTICS

(T_{amb} = 0°C to 70°C, V_{DD} = 3.3V ± 0.3V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{DD}	Operating current	$V_{IN} = V_{DD}$ or V_{SS}; V_{DD} = MAX $I_{OH} = I_{OL} = 0$	–	110	130	mA
$I_{DDS,}P$	Static current	$V_{IN} = V_{DD}$ or V_{SS}; V_{DD} = MAX $I_{OH} = I_{OL}$ = 0 mA SLEEP mode & RTC stop mode	–	10	100	µA
$I_{DDS,}Q$		$V_{IN} = V_{DD}$ or V_{SS}; V_{DD} = MAX $I_{OH} = I_{OL}$ = 0 mA SLEEP mode & RTC running mode	–	20	120	µA
I_{IN}	Input leakage current	$V_{IN} = V_{DD}$ or V_{SS}	–10	–	10	µA
V_{IH1}	Input voltage[1]	V_{DD} = 3.6V	$V_{DD} \times 0.8$	–	V_{DD} + 0.3	V
V_{IL1}	Input voltage[1]	V_{DD} = 3.0V	–0.3	–	$V_{DD} \times 0.2$	V
V_{IH2}	Input voltage[2]	V_{DD} = 3.6V	2.4	–	V_{DD} + 0.3	V
V_{IL2}	Input voltage[2]	V_{DD} = 3.0V	–0.3	–	0.6	V
V_{OH1}	Output voltage[3]	V_{DD} = 3.0V; I_{OH} = –4mA	V_{DD} – 0.6	–	–	V
V_{OL1}	Output voltage[3]	V_{DD} = 3.0V; I_{OL} = 4mA	–	–	V_{DD} + 0.4	V
V_{OH2}	Output voltage[4]	V_{DD} = 3.0; I_{OH} = –8mA	V_{DD} – 0.6	–	–	V
V_{OL2}	Output voltage[4]	V_{DD} = 3.0; I_{OL} = 8mA	–	–	V_{DD} + 0.4	V
V_{OH3}	Output voltage[5]	V_{DD} = 3.0; I_{OH} = –16mA	V_{DD} – 0.6	–	–	V
V_{OL3}	Output voltage[5]	V_{DD} = 3.0; I_{OL} = 16mA	–	–	V_{DD} + 0.4	V
V_{OH4}	Output voltage[6]	V_{DD} = 3.0; I_{OH} = –24mA	V_{DD} – 0.6	–	–	V
V_{OL4}	Output voltage[6]	V_{DD} = 3.0; I_{OL} = 24mA	–	–	V_{DD} + 0.4	V
I_{IHP}	Input current (Pull–down resister)	V_{DD} = MAX; VIN = V_{DD}	20	–	120	µA

NOTES:
1. SYSVLKIN
2. Other inputs
3. D[31:0], RAS0*, RAS1*, DCS0*, DCKE*, DQMH, DQML, DREQ*, DGRNT*, BC32K, VDAT[3:0], CP, LOAD, DF, FRAME, DISPON, VIDDONE, PWRCS, TXD, RXD, CS3~O*,CHIFS, CHICLK, CHIDOUT, CHIDIN, IO[6;0], SPICLK, SPIOUT, SPIIN, SIBSYNC, SIBDOUT, SIBMCLK, SIBCLK, RWPWR, IROUT, CARD1WAIT*, CARD2WAIT*, MIOX[2;0]
4. A[12:], ALE, RD*, WE* CAS3~O*, CARDREG*, CARDIOWR*, CARD1CSL*, CARD1CSH*, CARD2CSL*, CARD2CSH*
5. DCLKOUT
6. MBUSCLK, MBUSDATA

CRYSTAL OSCILLATOR CHARACTERISTICS

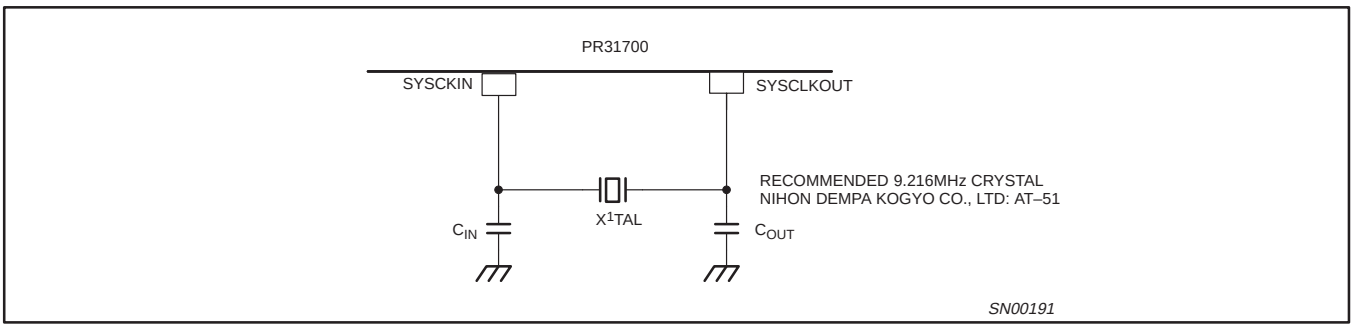


Figure 4. 10MHz Crystal

SYMBOL	PARAMETER	RECOMMENDED VALUE		UNIT
		MIN.	MAX.	
f_{IN}	Crystal Oscillator frequency	8.25	10	MHz
C_{IN}, C_{OUT}	External capacitors	10	33	pF

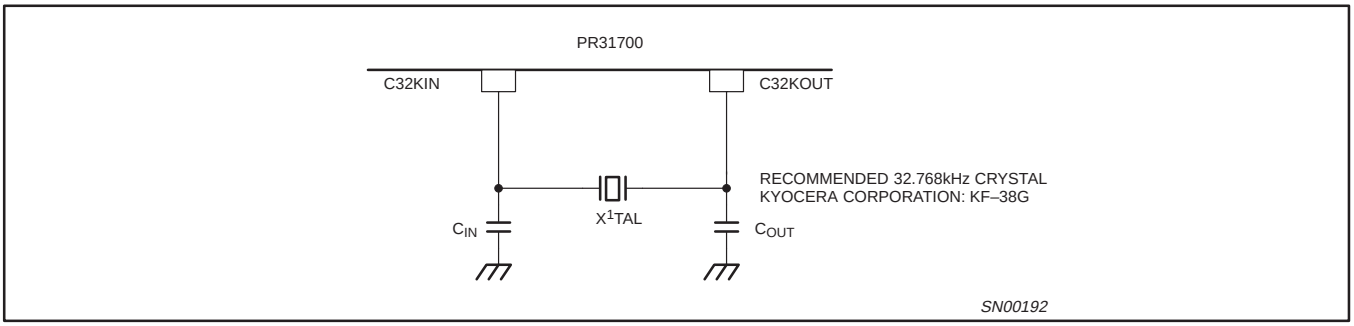


Figure 5. 32 kHz Crystal

SYMBOL	PARAMETER	RECOMMENDED VALUE		UNIT
		MIN.	MAX.	
C_{IN}, C_{OUT}	External capacitors	10	33	pF

ELECTRICAL SPECIFICATIONS
(V_{SS} = 0V, V_{DD} = 3.3V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Crystal stabilization time 9.216MHz	$T_{STA–10M}$	f = 8.25MHz10MHz X'tal : AT–51 Cin = Cout = 10pF–33pF	-	-	10	ms
Crystal stabilization time 32.768kHz	$T_{STA–32k}$	f = 32kHz X'tal : KF–38G Cin = Cout = 10pF–33pF	-	-	2	s

PR31700 TIMING

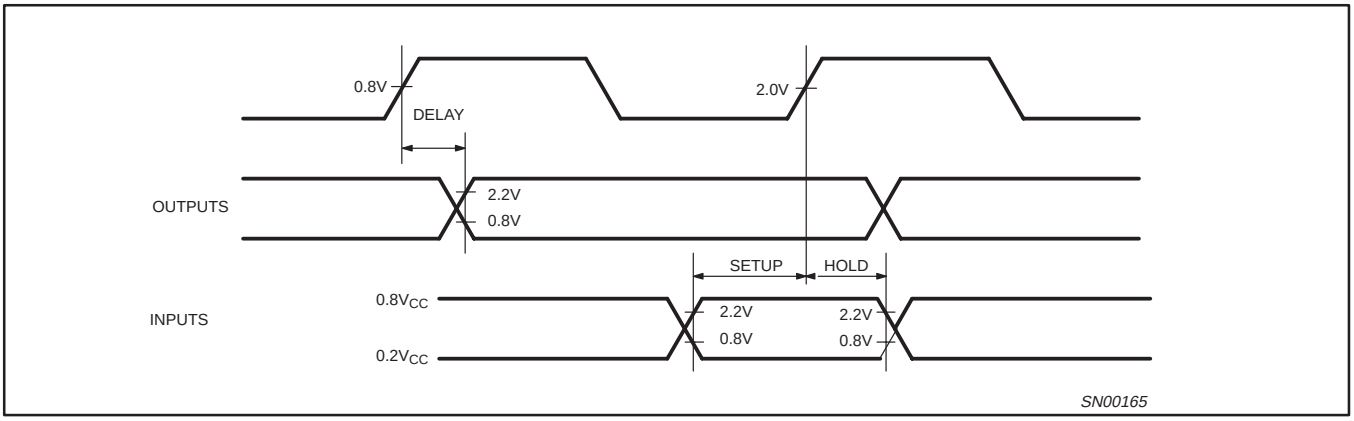


Figure 6. Definition of AC Specification

AC CHARACTERISTICS

The following operating conditions apply to all values specified in this section.
T_{amb} = 0°C to 70°C, V_{DD} = 3.3 ±0.3V, External Capacitance = 40pF

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	DCLKOUT high time	-	5.4	-	ns
2	DCLKOUT low time	-	5.4	-	ns
3	DCLKOUT period	-	13.5	-	ns
4	Delay DCLKOUT to ALE	Rising	-	4	ns
4	Delay DCLKOUT to ALE	Falling	-	3	ns
Memory Interface					
4	Delay DCLKOUT to A[12:0]	-	-	8	ns
4	Delay DCLKOUT to D[31:16]	-	-	8	ns
4	Delay DCLKOUT to D[15:0]	-	1.5	8	ns
4	Delay DCLKOUT to CS3–0*	Rising	-	10	ns
4	Delay DCLKOUT to CS3–0*	Falling	-	10	ns
4	Delay DCLKOUT to RD*	Rising	-	8	ns
4	Delay DCLKOUT to RD*	Falling	-	7	ns
4	Delay DCLKOUT to WE*	Rising	-	5	ns
4	Delay DCLKOUT to WE*	Falling	-	4	ns
4	Delay DCLKOUT to CAS3–0*	Rising	-	2.5	ns
4	Delay DCLKOUT to CAS3–0*	Falling	-	2.5	ns
4	Delay DCLKOUT to CARDxCSx*	Rising	-	9	ns
4	Delay DCLKOUT to CARDxCSx*	Falling	-	8	ns
4	Delay DCLKOUT to CARDDIR*	Rising	-	12	ns
4	Delay DCLKOUT to CARDDIR*	Fallmng	-	11	ns
4	Delay DCLKOUT to CARDREG*	Rising	-	9	ns
4	Delay DCLKOUT to CARDREG*	Fatting	-	10	ns
4	Delay DCLKOUT to CARDIORD*	Rising	-	10	ns
4	Delay DCLKOUT to CARDIORD*	Falling	-	9	ns
4	Delay DCLKOUT to CARDIOWR*	Rising	-	9	ns
4	Delay DCLKOUT to CARDIOWR*	Falljng	-	9	ns
4	Delay DCLKOUT to RAS0*	Rising	-	6	ns
4	Delay DCLKOUT to RAS0*	Falling	-	6	ns
4	Delay DCLKOUT to RAS1*	Rising	1.5	8	ns
4	Delay DCLKOUT to RAS1*	Falling	1.5	9	ns
4	Delay DCLKOUT to DQMH/L	Rising	1.5	8	ns
4	Delay DCLKOUT to DQMH/L	Falling	1.5	9	ns
4	Delay DCLKOUT to DCS0*	Rising	1.5	7	ns
4	Delay DCLKOUT to DCS0*	Falling	1.5	6	ns
4	Delay DCLKOUT to DCKE	Rising	1.5	8	ns
4	Delay DCLKOUT to DCKE	Falling	1.5	8	ns
4	Delay DCLKOUT to MCS3–0*	Rising	-	10	ns
4	Delay DCLKOUT to MCS3–0*	Falling	-	10	ns
5	D[31 : 16] to DCLKIN Setup time	-	1	-	ns

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
6	D[31 : 16] to DCLKIN Hold time	-	2	-	ns
5	D[15:0] to DCLKIN Setup time	-	0	-	ns
6	D[15:0] to DCLKIN Hold time	-	2.5	-	ns
7	DCLKOUT to DCLKIN Board Delay time	-	0	3	ns

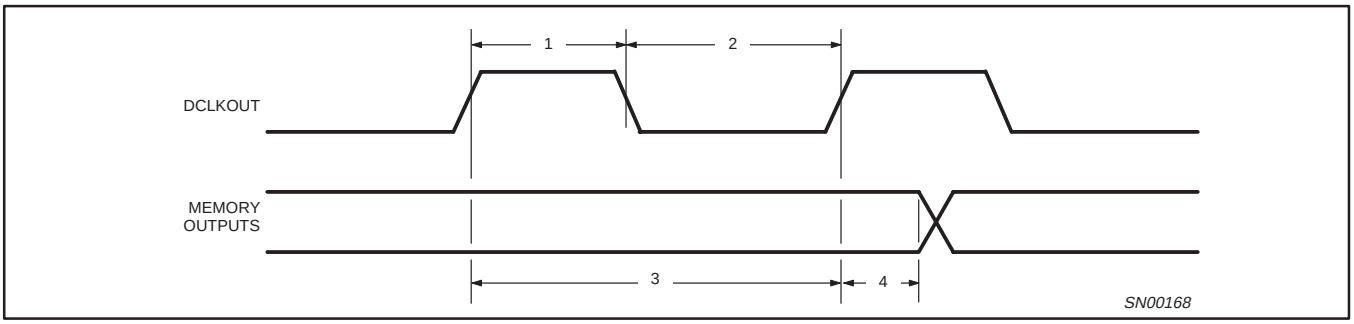


Figure 7. Memory Output and Clock Timing

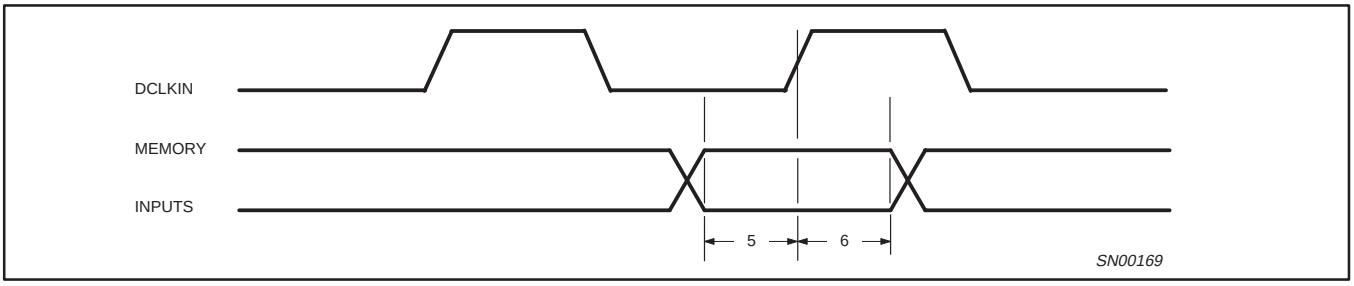


Figure 8. Memory Input Timing

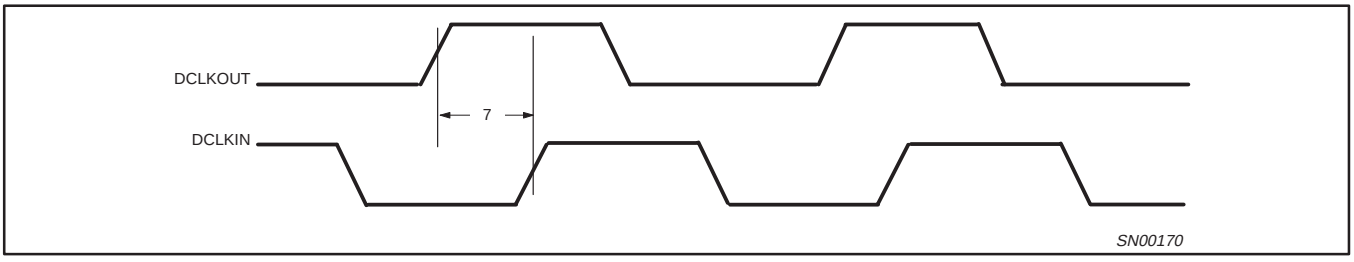


Figure 9. DCLKOUT to DCLKIN

CHI CHARACTERISTICS

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	CHICLK high time	-	100	-	ns
2	CHICLK low time	-	100	-	ns
3	CHICLK period	-	225	-	ns
4	Delay CHICLK Rising to CHIDOUT(Master)	Rising	-	5	ns
4	Delay CHICLK Rising to CHIDOUT(Master)	Falling	-	5	ns
7	Delay CHICLK Falling to CHIDOUT(Master)	Rising	-	5	ns
7	Delay CHICLK Falling to CHIDOUT(Master)	Falling	-	5	ns
4	Delay CHICLK Rising to CHIFS(Master)	Rising	-	5	ns
4	Delay CHICLK Rising to CHIFS(Master)	Falling	-	5	ns
7	Delay CHICLK Falling to CHIFS(Master)	Rising	-	5	ns
7	Delay CHICLK Falling to CHIFS(Master)	Falling	-	5	ns
4	Delay CHICLK Rising to CHIDOUT(Slave)	Rising	-	15	ns
4	Delay CHICLK Rising to CHIDOUT(Slave)	Falling	-	15	ns
7	Delay CHICLK Falling to CHIDOUT(Slave)	Rising	-	15	ns
7	Delay CHICLK Falling to CHIDOUT(Slave)	Falling	-	15	ns
4	Delay CHICLK Rising to CHIFS(Slave)	Rising	-	15	ns
4	Delay CHICLK Rising to CHIFS(Slave)	Falling	-	15	ns
7	Delay CHICLK Falling to CHIFS(Slave)	Rising	-	15	ns
7	Delay CHICLK Falling to CHIFS(Slave)	Falling	-	15	ns
5	CHIDIN to CHICLK Rising Setup time(Master)	-	20	-	ns
6	CHIDIN to CHICLK Rising Hold time(Master)	-	20	-	ns
8	CHIDIN to CHICLK Falling Setup time(Master)	-	20	-	ns
9	CHIDIN to CHICLK Falling Hold time(Master)	-	20	-	ns
5	CHIFS to CHICLK Rising Setup time(Slave)	-	20	-	ns
6	CHIFS to CHICLK Rising Hold time(Slave)	-	20	-	ns
8	CHIFS to CHICLK Falling Setup time(Slave)	-	20	-	ns
9	CHIFS to CHICLK Falling Hold time(Slave)	-	20	-	ns
5	CHIDIN to CHICLK Rising Setup time(Slave)	-	20	-	ns
6	CHIDIN to CHICLK Rising Hold time(Slave)	-	20	-	ns
8	CHIDIN to CHICLK Falling Setup time(Slave)	-	20	-	ns
9	CHIDIN to CHICLK Falling Hold time(Slave)	-	20	-	ns

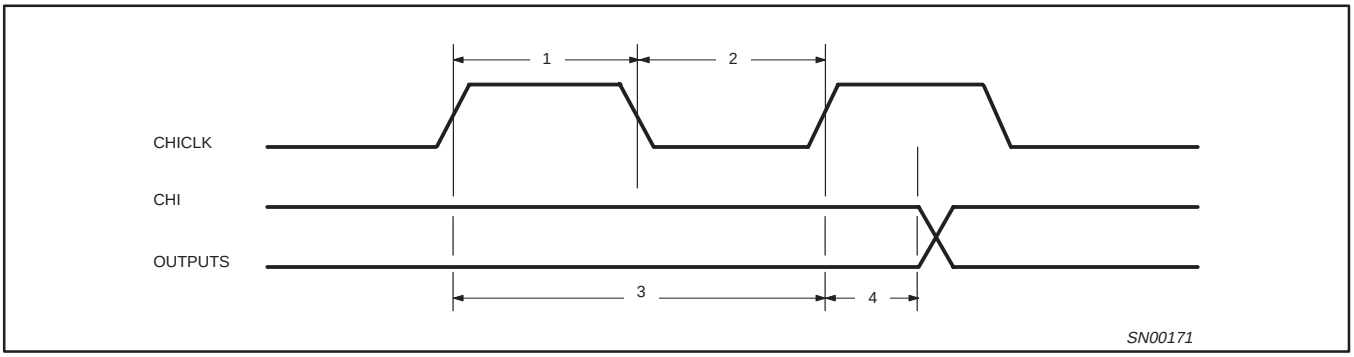


Figure 10. CHI Output and Clock Timing (CHITXEDGE=1)

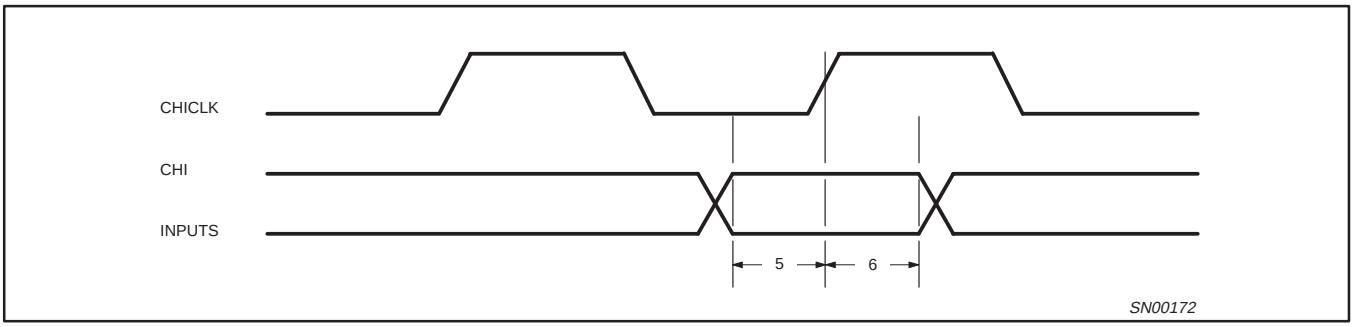


Figure 11. CHI Input Timing (CHIRXEDGE=1)

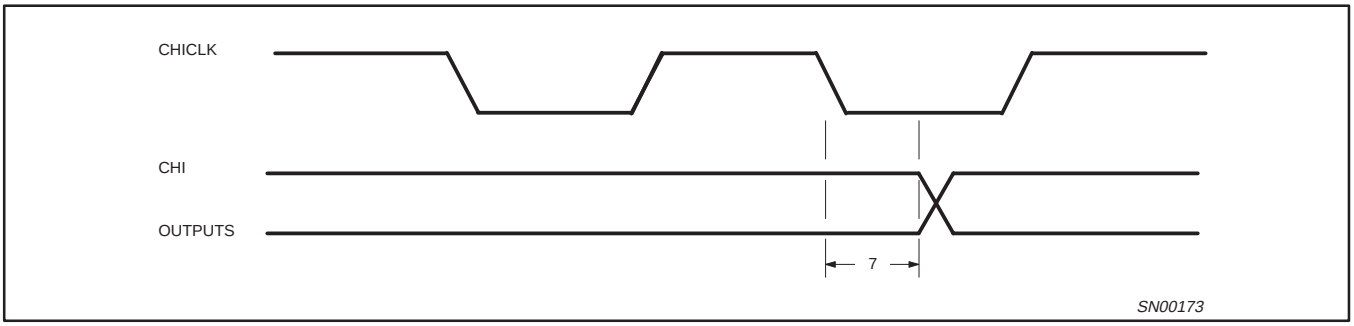


Figure 12. CHI Output and Clock Timing (CHITXEDGE=0)

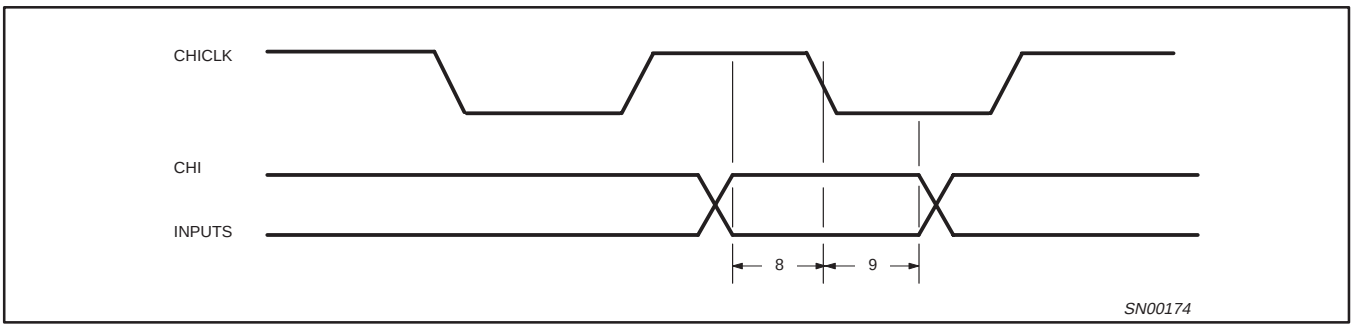


Figure 13. CHI Input Timing (CHIRXEDGE=0)

SIB CHARACTERISTICS

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	SIBMCLK high time	-	20	-	ns
2	SIBMCLK low time	-	20	-	ns
3	SIBMCLK period	-	50	-	ns
4	Delay SIBMCLK (Master) to SIBSCLK	Rising	-	5	ns
5	Delay SIBMCLK (Master) to SIBSCLK	Falling	-	5	ns
6	Delay SIBSCLK Rising to SIBSYNC	Rising	-	2	ns
6	Delay SIBSCLK Rising to SIBSYNC	Falling	-	2	ns
6	Delay SIBSCLK Rising to SIBDOUT	Rising	-	2	ns
6	Delay SIBSCLK Rising to SIBDOUT	Falling	-	2	ns
7	SIBDIN to SIBSCLK Rising Setup time	-	20	-	ns
8	SIBDIN to SIBSCLK Rising Hold time	-	0	-	ns

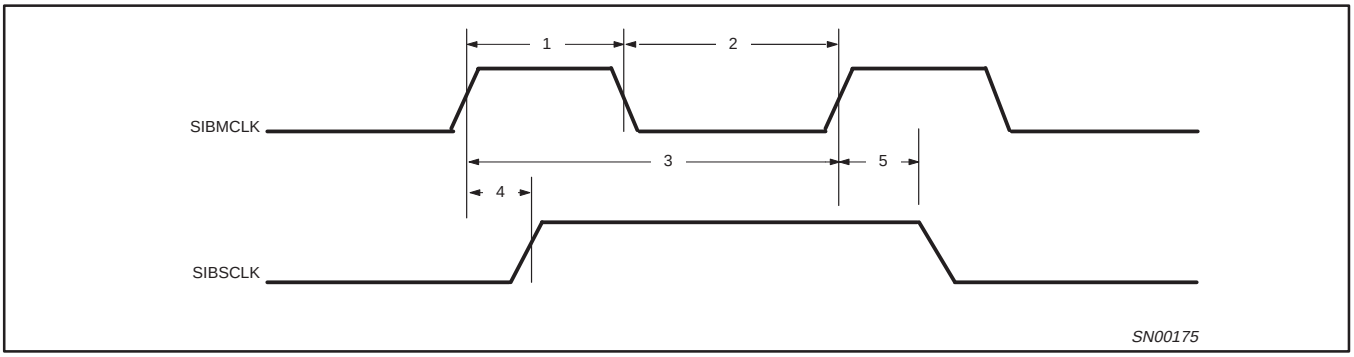


Figure 14. SIB CLK Timing

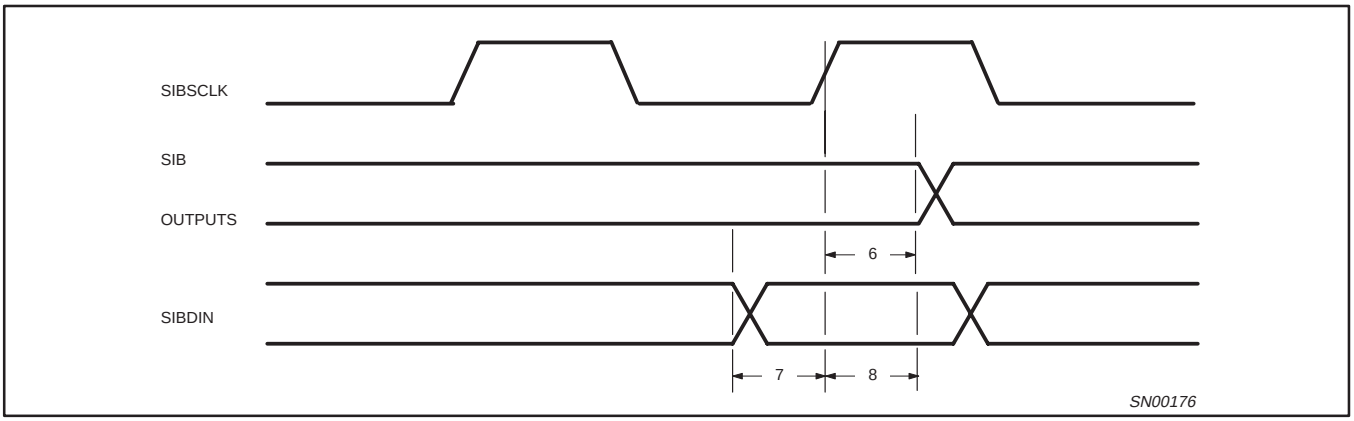


Figure 15. SIB Timing

SPI CHARACTERISTICS

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	SPICLK high time	-	120	-	ns
2	SPICLK low time	-	120	-	ns
3	SPICLK period	-	250	-	ns
4	Delay SPICLK Rising to SPIOUT	Rising	-	5	ns
4	Delay SPICLK Rising to SPIOUT	Falling	-	5	ns
7	Delay SPICLK Falling to SPIOUT	Rising	-	5	ns
7	Delay SPICLK Falling to SPIOUT	Falling	-	5	ns
8	SPIIN to SPICLK Rising Setup time	-	15	-	ns
9	SPIIN to SPICLK Rising Hold time	-	15	-	ns
5	SPIIN to SPICLK Falling Setup time	-	15	-	ns
6	SPIIN to SPICLK Falling Hold time	-	15	-	ns

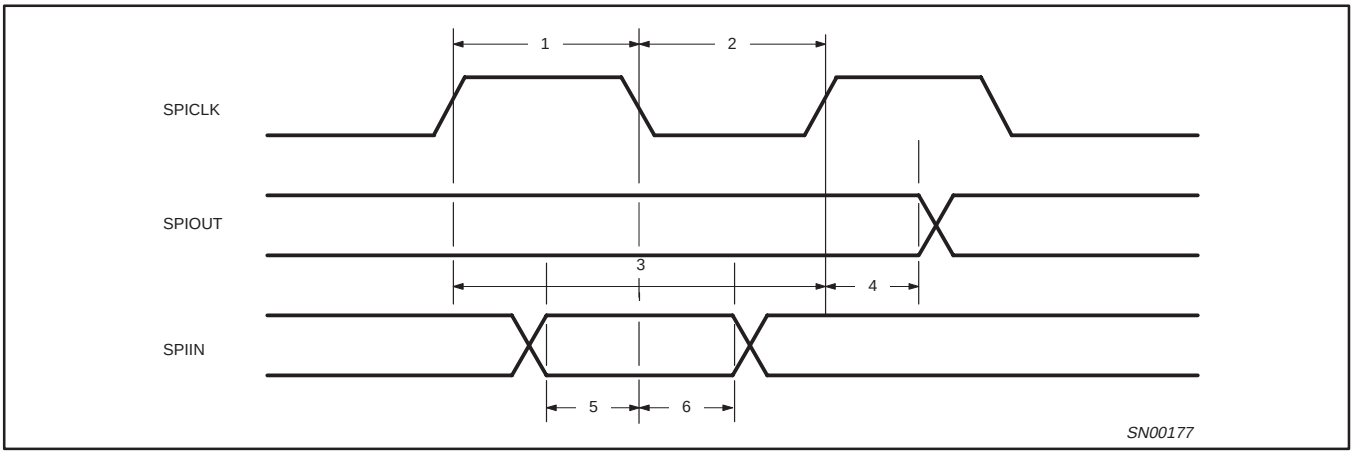


Figure 16. SPI Timing (PHAPOL = 1)

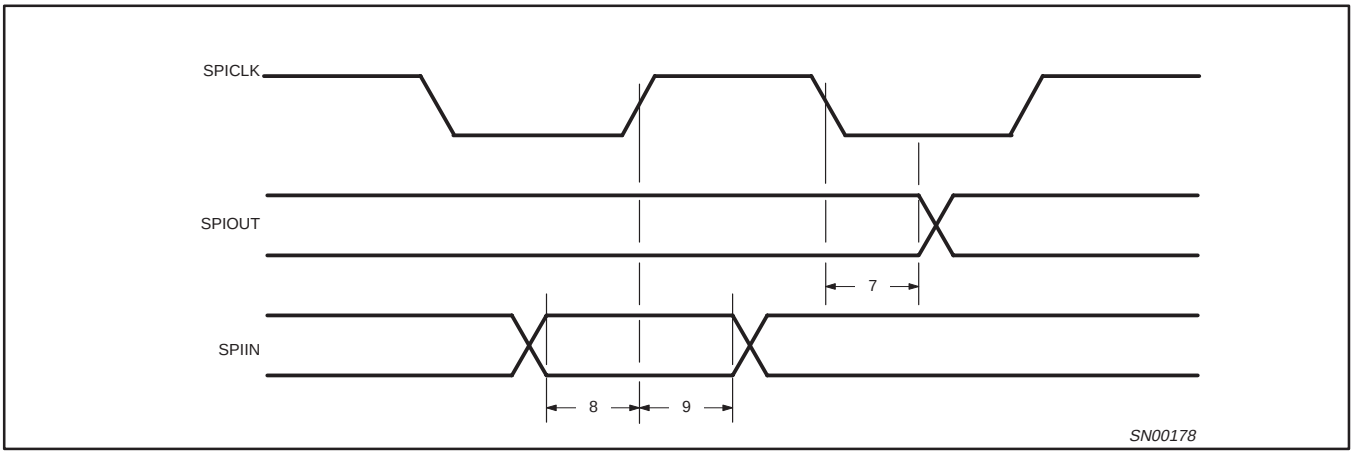


Figure 17. SPI Timing (PHAPOL = 0)

VIDEO CHARACTERISTICS

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	LOAD Pule width	-	100	1600	ns
2	Delay LOAD Falling to FRAME	-	100	3200	ns
3	Delay LOAD Falling to DF	-	100	3200	ns
4	Delay LOAD Falling to CP	-	100	3200	ns
5	Delay CP Rising to VDAT[3:0]	-	-	5	ns
6	VDAT to CP Rising Setup	-	15	25	ns
7	VDAT to CP Rising Hold	-	15	25	ns

NOTE:
1. Values shown assume a 75MHz clock for the CPU. Min and Max values are programmable using Video Control Registers.

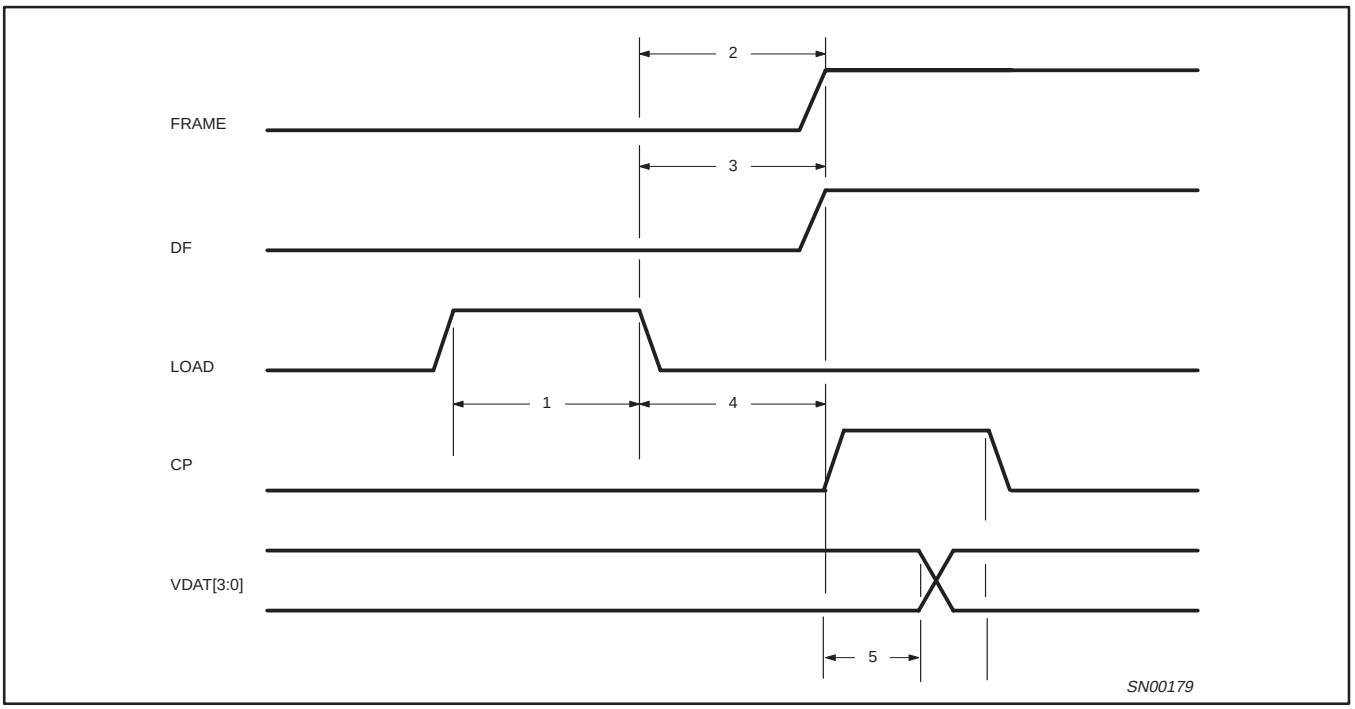


Figure 18. Video Timing, 4-Bit Non-Split LCD

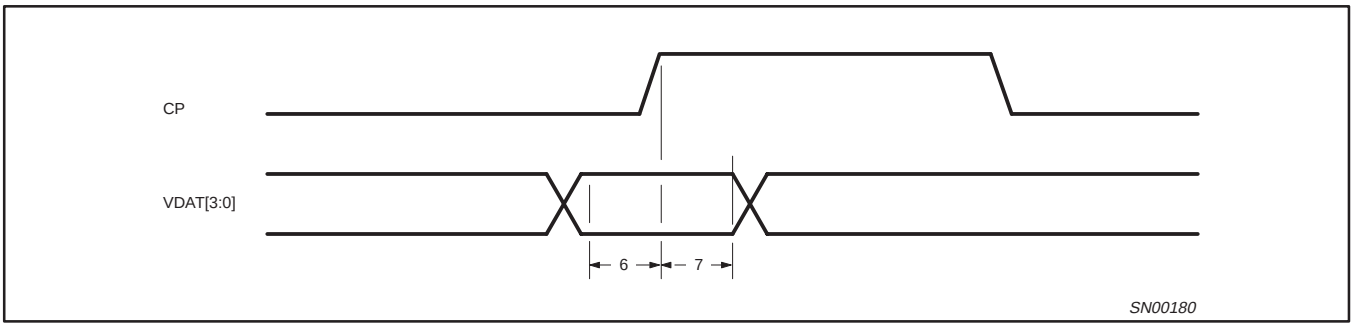


Figure 19. Video Data Timing, 4-Bit Split LCD and 8-Bit Non-Split LCD

POWER CHARACTERISTICS

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	VSTANDBY to PON* Rising	-	50	-	ms
2	VSTANDBY to ONBUTN delay time	-	2	-	s

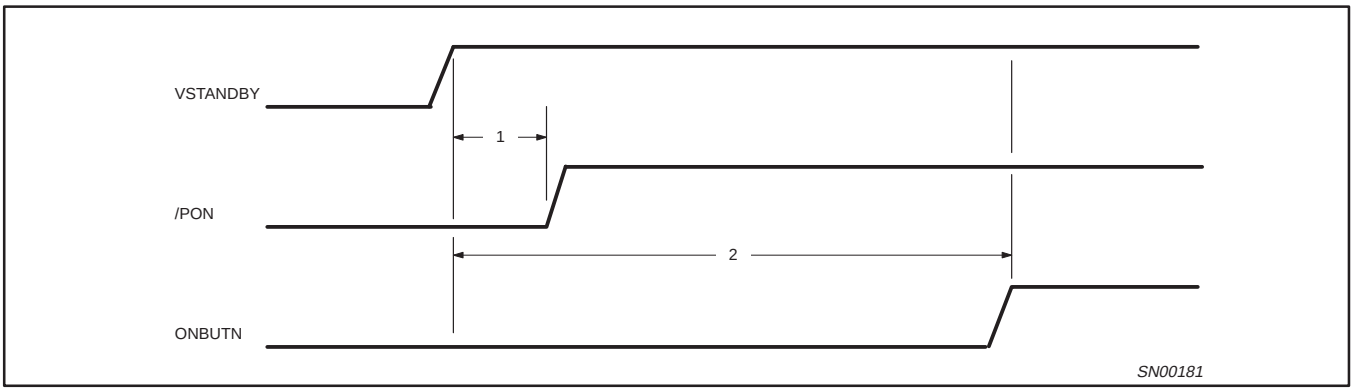


Figure 20. Power On Timing Diagram

CPU RESET CHARACTERISTIC

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	CPURES* low time	-	10	-	ns

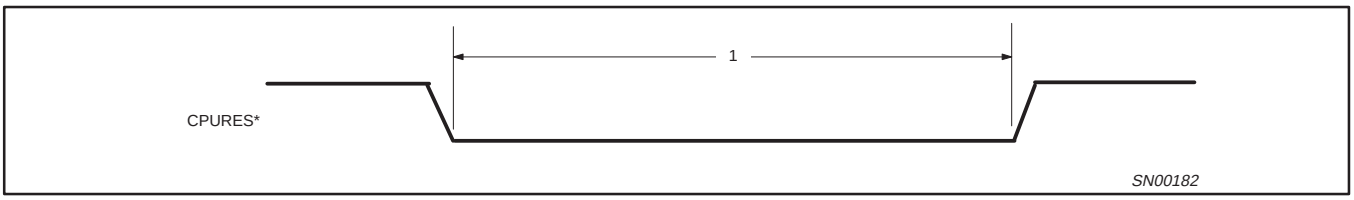
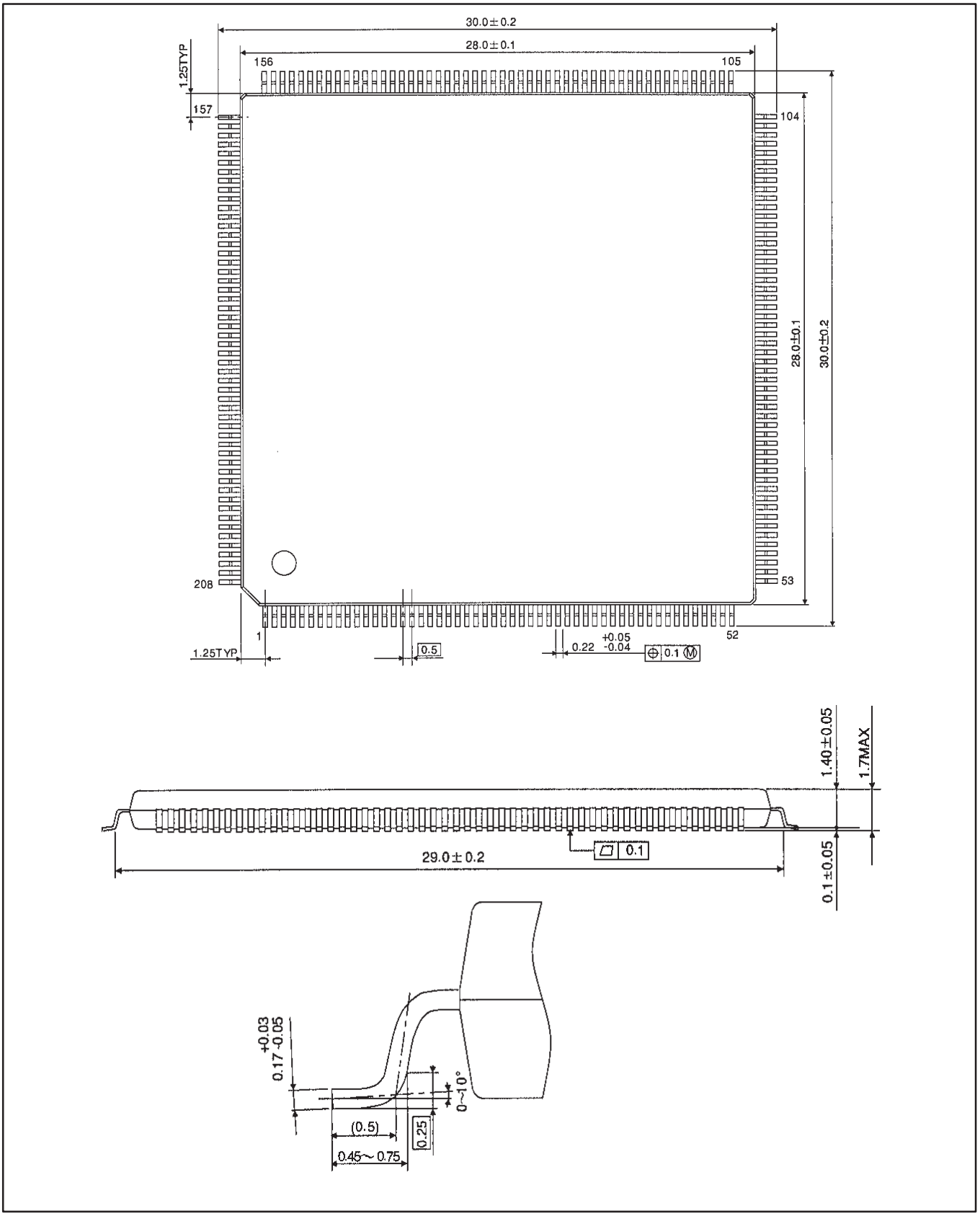


Figure 21. CPU Reset Timing Diagram

LQFP208: 208-PIN PLASTIC LOW PROFILE QUAD FLAT PACKAGE



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Data sheet status	Product status	Definition [1]
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