APPLICATION NOTE

BLV859 UHF linear push-pull power transistor

AN98013

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CONTENTS

1 ABSTRACT

A broadband linear amplifier design is presented, suitable for application in TV transposers operating in band IV and V (470 to 860 MHz). The design is based on two BLV859 bipolar transistorscombined with quadrature hybrids. Typical results at the recommended class-A bias point (25.5 V/9.1 A) for the total module include 40 W peak sync output power at –54 dB three tone IMD level (fvision = –8 dB, fsound = –10 dB, fsideband = –16 dB) and an average gain of 10.5 dB in the (470 to 860) MHz range.

2 INTRODUCTION

The BLV859 is a bipolar linear push-pull power transistor designed to operate in the 460 to 860 MHz range. With a specified output power of 20 W peak-sync in class-A it is the largest device in the new generation of transposer transistors. The intermodulation distortion level is < –54 dB (fvision = –8 dB, fsound = –10 dB, fsideband = –16 dB) and power gain >10 dB at 860 MHz.

For application in TV transposers for Band IV/V (470 to 860 MHz) a wideband linear power amplifier has been designed with two BLV859 transistors in class-A.

2.1 Amplifier Electrical design objectives

The amplifier operates at a supply voltage of 25.5 V and a total current Ic = 9.1 A (2 × 4.55 A).

Electrical characteristics (Ths = 25 °C, 25.5 V, 9.1 A, 470 to 860 MHz bandwidth)

	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power gain (small signal)	Gp	9.5	–	–	dB
Gain ripple (small signal)	Griple	–	–	±1	dB
Output Power @ 1 dB compression	Pout	60	–	–	W
Intermodulation: (–8 dB/–7 dB/–16 dB, Pref = 40 W)	IMD1	–	–	–50	dB
Intermodulation: (–8 dB/–10 dB/–16 dB, Pref = 40 W)	IMD2	–	–	–53	dB
Input return loss/Output return loss	IRL/ORL	–	–	–15	dB

3 DESIGN OF THE AMPLIFIER

The amplifier consists of 2 balanced circuits, both equipped with a BLV859 and coupled in parallel by means of a wideband 3 dB –90 degree sagewireline coupler at the input and output.

3.1 Mounting the transistors

For good thermal contact, heatsink compound should used when mounting the transistors on a heatsink.

3.2 Balun

Both input and output matching circuits of each BLV859 are connected to a coax BALUN which splits a 50 Ω unbalanced port in two 12.5 Ω ports. The BALUN has a transformation factor of 2.

The construction of the BALUN is described in Fig.4.

Essential for the BALUN is the shortcircuit between the inner and outerlead as can be seen in Figs 1 and 2.

3.3 Bias circuit

Each transistor has its own bias unit to obtain a stable DC setting. With the potentiometers P1 and P2 it’s possible to adjust the collector current of both BLV859 transistors. The nominal collector current should be 4.55 A.

The sense resistor in the collector branch is implemented as a folded printed line (L17). In this way we obtain a small sense resistor (approximately 80 m/Ω) that can handle the dissipated power.

3.4 Positioning of the matching capacitors

Figure 2 gives the component layout of the BLV859 amplifier.

Input:
The capacitors (C30, C35, C32 and C39) are situated on a distance of approximately 1 mm from the transistor.
The capacitors (C26, C34, C28 and C38) are situated on a distance of approximately 0.5 mm from the balun.
The position of these capacitors influences the tuning for flat gain.
Output:
The capacitors (C27, C37, C28 and C41) are situated as close as possible to the Balun.
The position of capacitors (C31, C36, C33 and C40) is critical to obtain the S22 contours as described in the amplifier tuning procedure.

Figure 3 gives the dimensions of the BLV859 amplifier printed-circuit board and Fig.5 gives the printed-circuit board layout of the frontside and backside.

3.5 Amplifier tuning procedure

Both amplifiers are separately tuned under small signal conditions by means of a networkanalyzer. The amplifiers are tuned for flat gain over the complete bandwidth (470 to 860 MHz). To obtain a flat gain the input is gradually mismatch. The input returnloss S11 is the main parameter for setting the gain level and flatness.

Tuning of the output will mainly influence IMD and to a lesser extent the gain flatness. To obtain a good IMD performance over the band it’s recommended to follow the S22 tuning contours as plotted in Figs 6 to 9. A minimal S22 is required between 700 and 800 MHz (better then –25 dB). (The markers are positioned at 470 MHz (marker 1), 636 MHz (marker 2), 860 MHz (marker 3)). An S22 of –15 to –20 dB is required at the highest frequency (860 MHz) and at midfrequency (636 MHz). An S22 of –12 to –15 dB is required at the lowest frequency (470 MHz).

After individual tuning, both amplifiers can be coupled and the load resistors can be attached. The module is now ready for use and the complete characterization can be started. Figures 10 to 13 show the small signal characterization of the complete module.

4 AMPLIFIER PERFORMANCE

Broadband measurement data are presented in graphs of Figs 14 to 18, IMD and powergain are given at two 3-tone systems, (fv = –8 dB/fsb = –16 dB/fs = –10 dB) and (fv = –8 dB/fsb = –16 dB/fs = –7 dB), over the complete frequency range (470 MHz to 860 MHz).

IMD and powergain are given at two 3-tone systems, (fv = –8 dB/fsb = –16 dB/fs = –10 dB) and (fv = –8 dB/fsb = –16 dB/fs = –7 dB), versus P0_sync at the highest channel (Ch69).

At the nominal Po_sync level of 40 W for which the module is dimensioned the full band performance is as follow:

3 tones (–8/–16/–7) dB: IMD ≤ –50 dB/powergain ≥9.5 dB

3 tones (–8/–16/–10) dB: IMD ≤ –54 dB/powergain ≥9.5 dB

When coupling the amplifiers a degradation in powergain and IMD can be expected. Reasons for this are the amplitude and phase imbalances in the couplers and transistors. Also detuning of the loads of both transistors due to non-perfect 50 Ω coupler parts. At the highest frequency (ch69) only a slight degration in gain and IMD has been noted, in the order of some tents of a dB in Gain and 0.5 dB in IMD. At lower frequencies the degradation can be more or less pronounced. In all cases the IMD and gain will fullfill the minimal requirements (IMD ≤ –53 dB (–8/–16/–10 dB) and a small signal gain ≥9.5 dB) over the band.

5 CONCLUSION

A complete transposer module is presented base on 2 × BLV859, capable of operating in full band IV/V with flat gain and good linearity. Design and tuning procedures described result in a good broadband behavior. High gain ≥9.5 dB and good linearity (Po_sync ≥40 W @ –53 dB (–8/–16/–10) dB has been obtained at the class-A bias point (25 V/9.1 A).

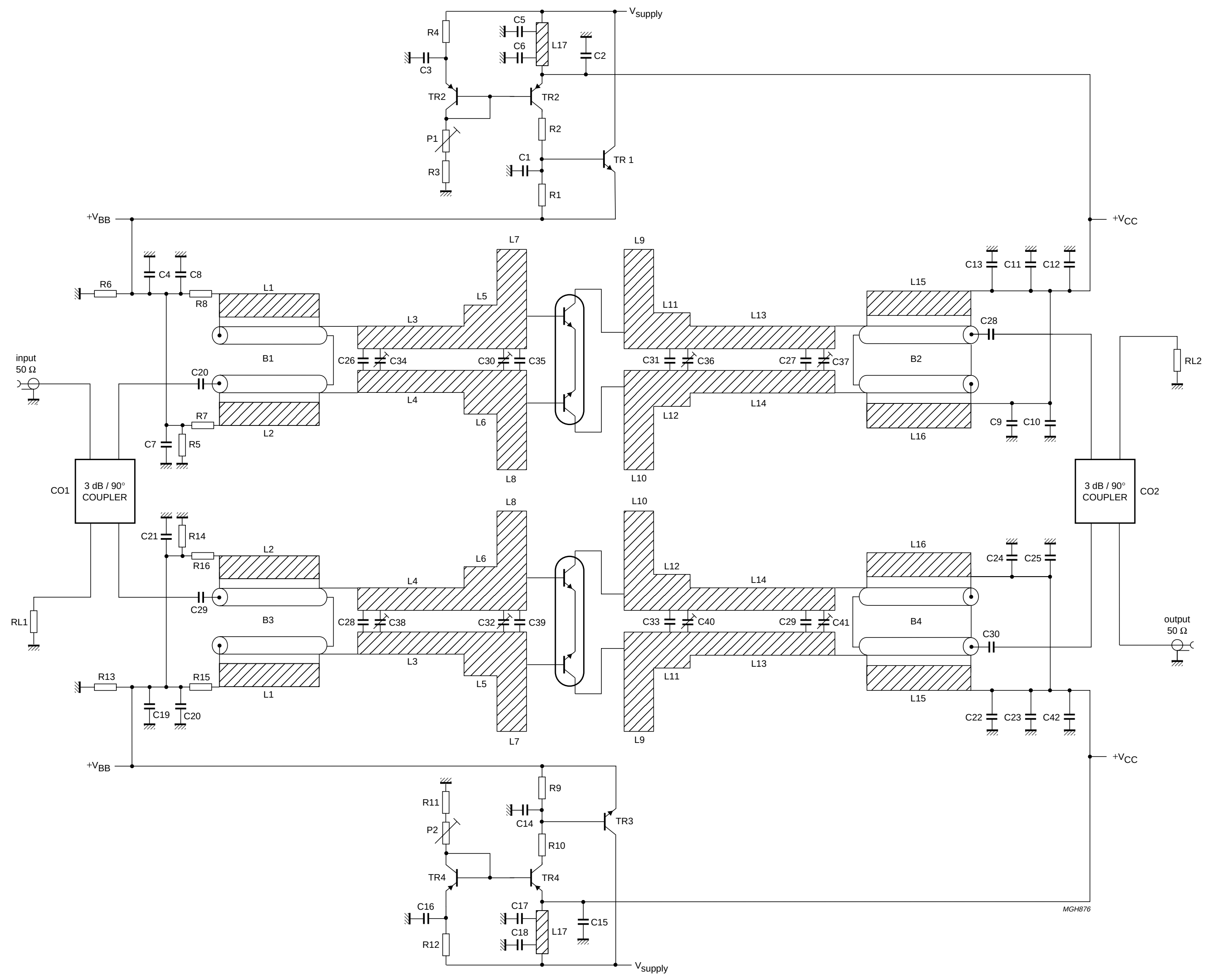
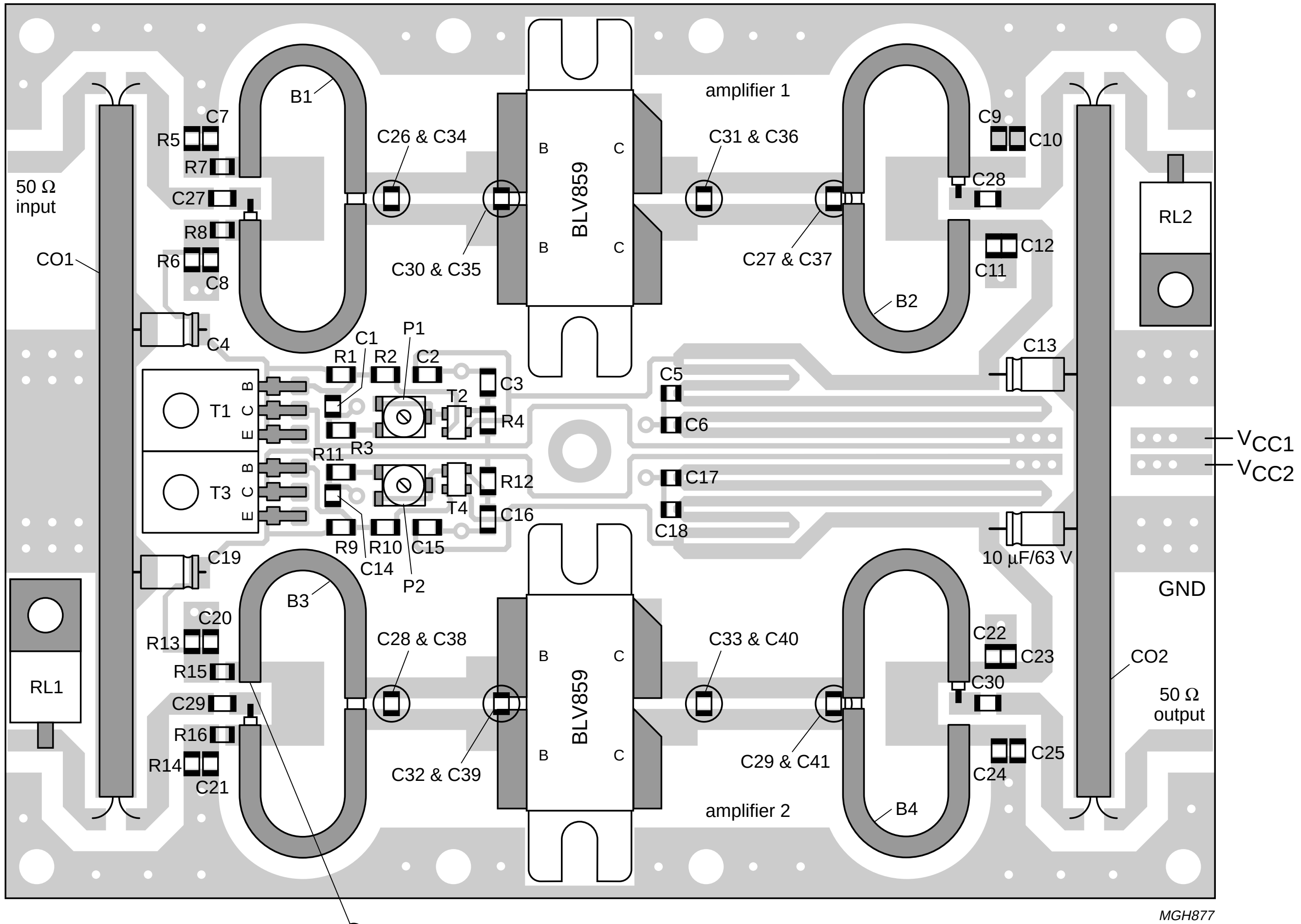


Fig.1 Schematic diagram of the BLV859 amplifier.



inner lead and outer lead are shorted (repeat for each balun)

See Section 6.

Fig.2 Component layout of the BLV859 amplifier.

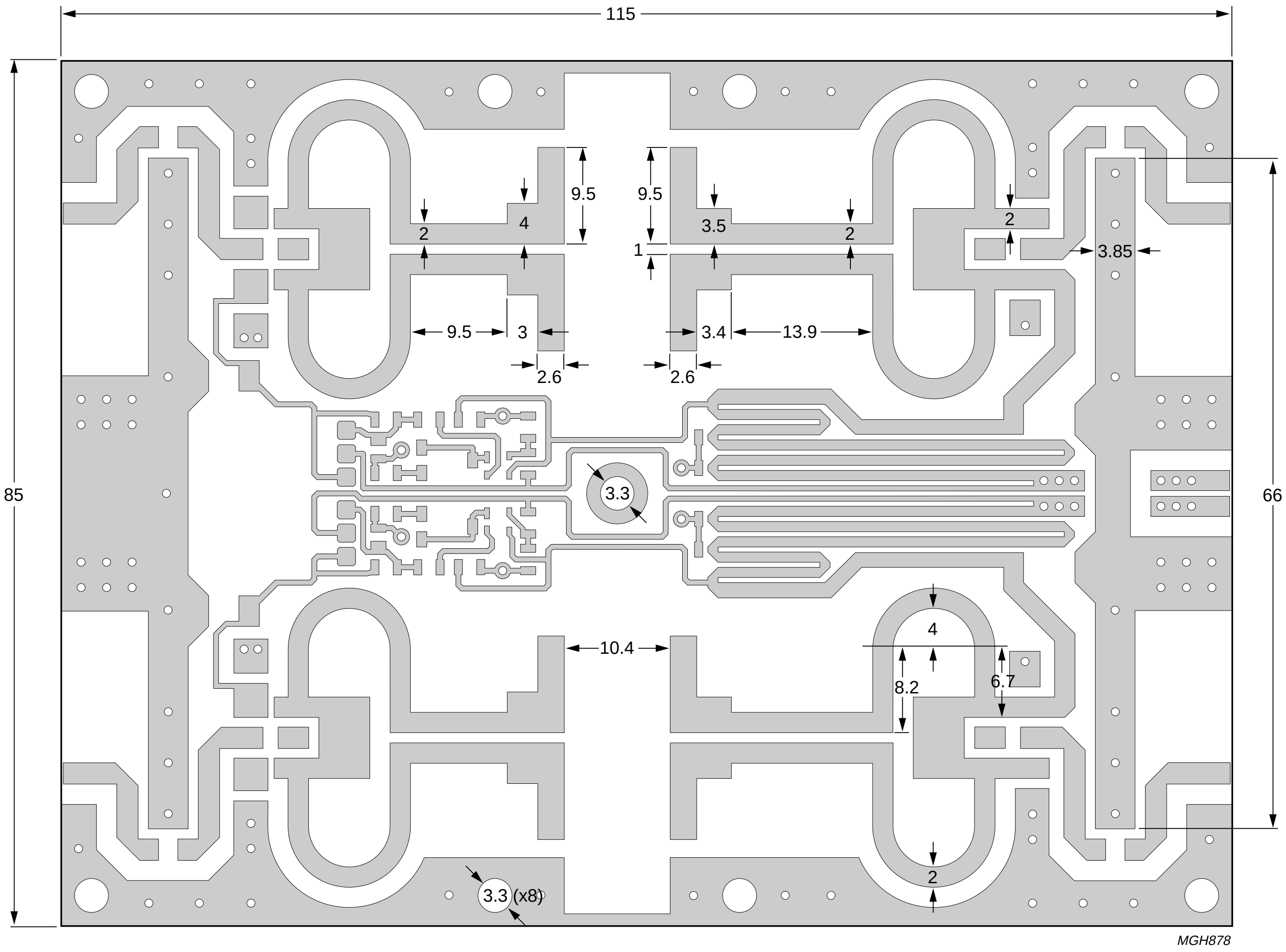


Fig.3 Printed-circuit board Dimension of the BLV859 amplifier.

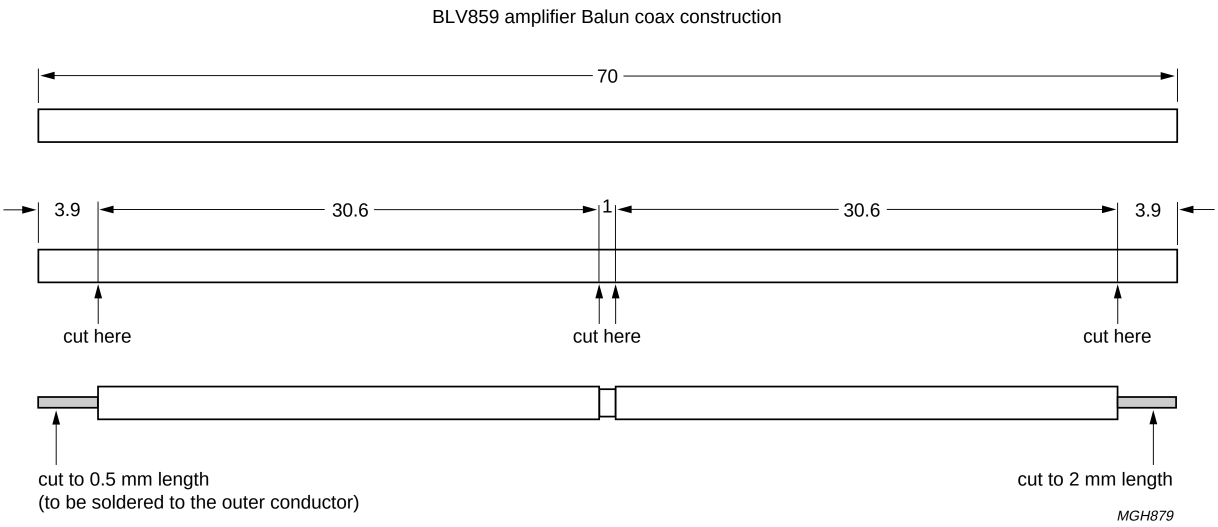
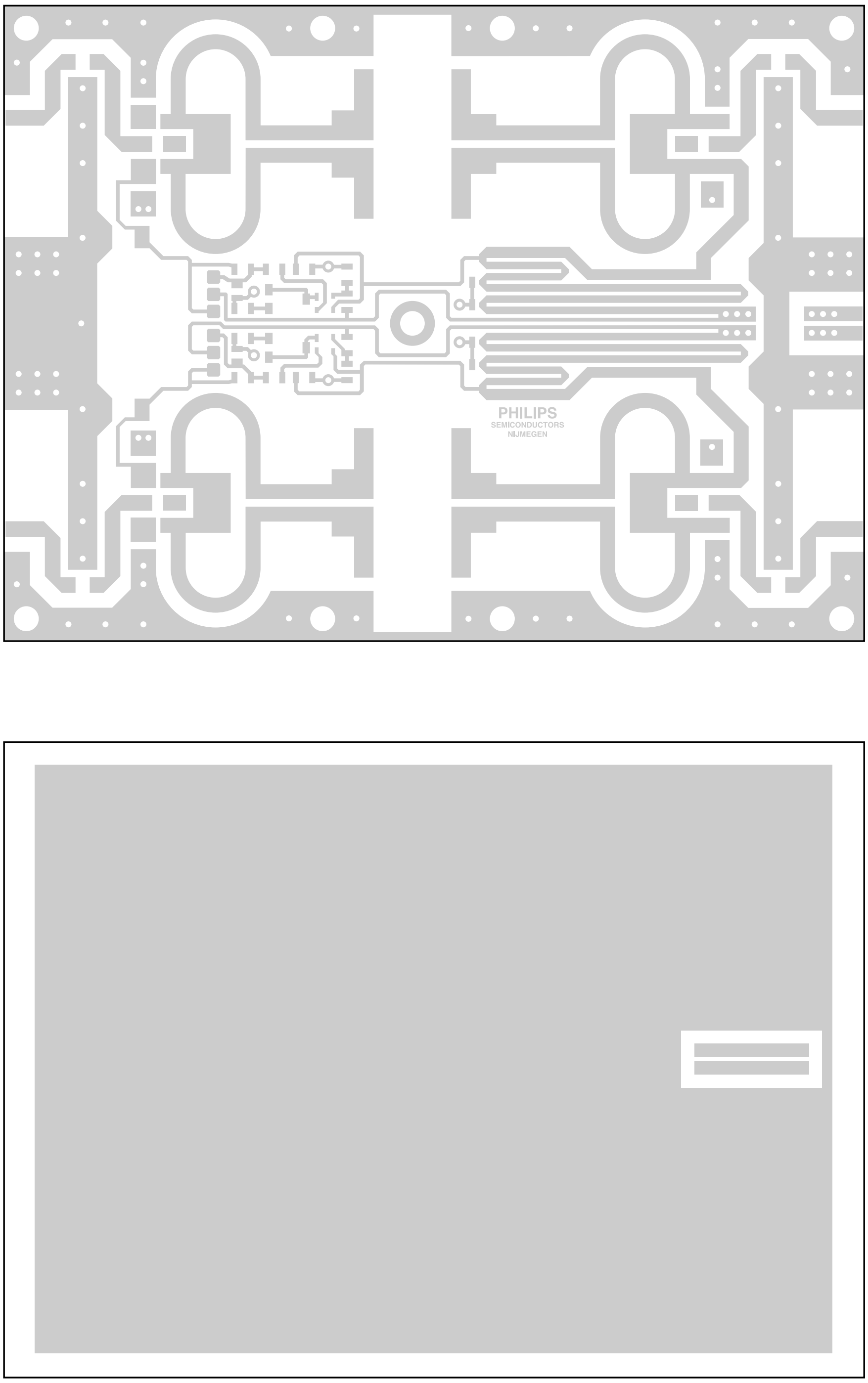
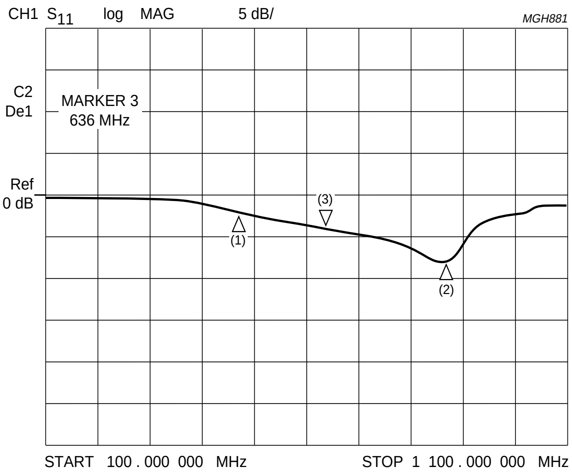


Fig.4 BALUN construction.



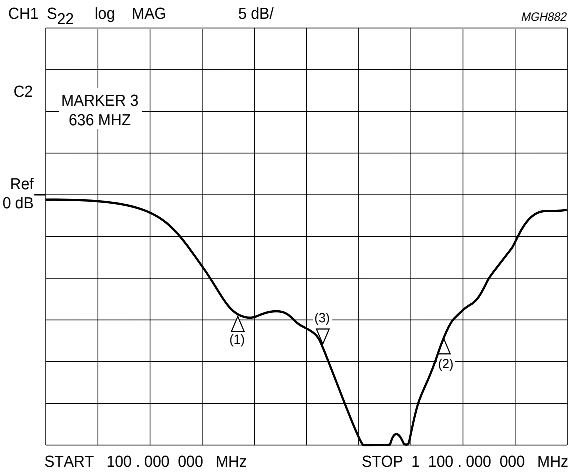
MGH880

Fig.5 Printed-circuit board layout of the frontside and backside (not to scale).



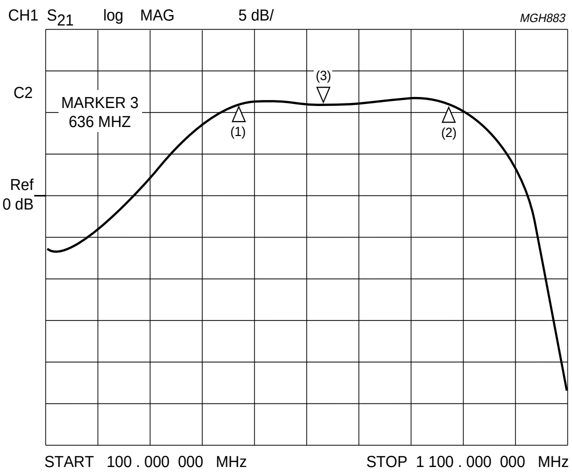
(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; –4 dB.

Fig.6 Small signal results of a separated amplifier; a.



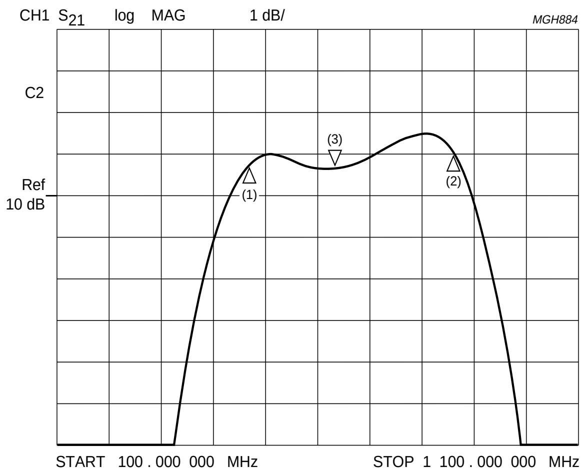
(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; –17.8 dB.

Fig.7 Small signal results of a separated amplifier; b.



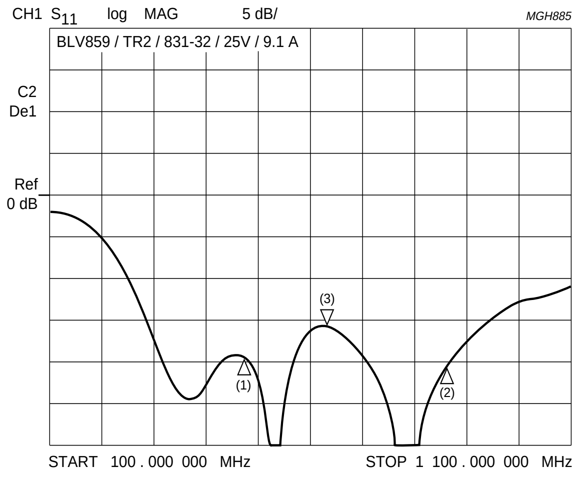
(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; –10.55 dB.

Fig.8 Small signal results of a separated amplifier; c.



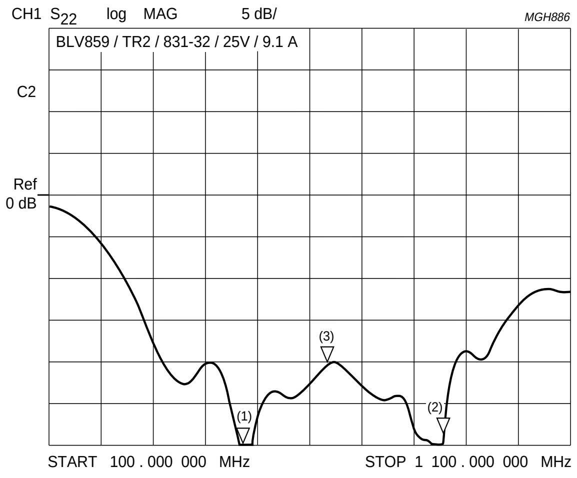
(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; –10.65 dB.

Fig.9 Small signal results of a separated amplifier; d.



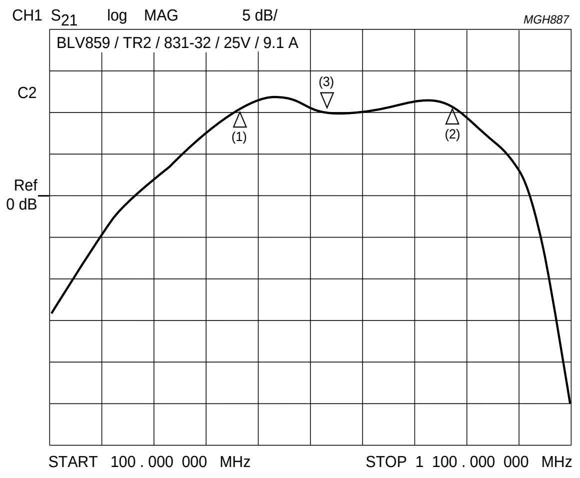
(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; –15.8 dB.

Fig.10 Small signal results of the total model; a.



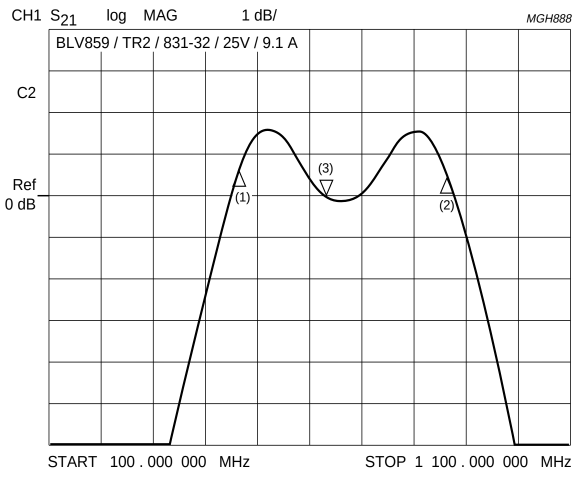
(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; –20.3 dB.

Fig.11 Small signal results of the total model; b.



(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; –9.6 dB.

Fig.12 Small signal results of the total model; c.



(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; –9.7 dB.

Fig.13 Small signal results of the total model; d.

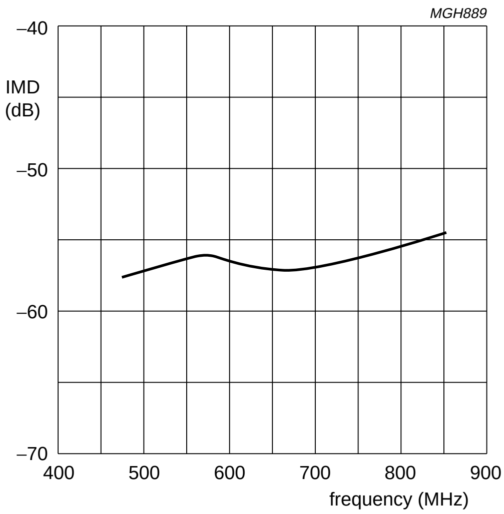


Fig.14 IMD versus frequency for the complete module (Po_sync = 40 W, 3 tones fv = –8 dB, fs = –16 dB, fsb = –10 dB).

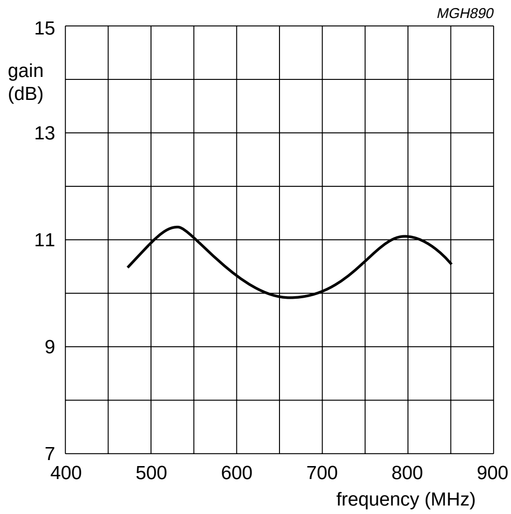


Fig.15 Gain versus frequency for the complete module (Po_sync = 40 W, 3 tones fv = –8 dB, fs = –16 dB, fsb = –10 dB).

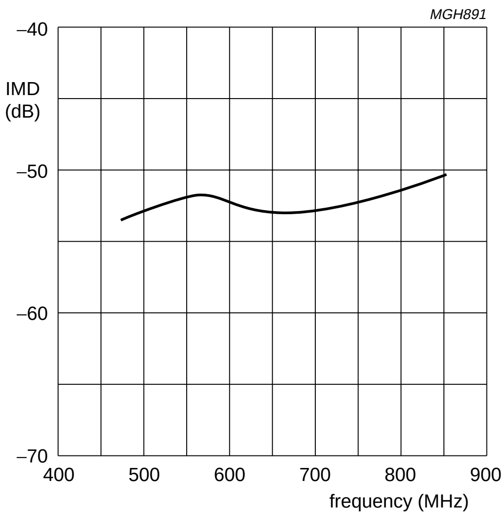


Fig.16 IMD versus frequency for the complete module (Po_sync = 40 W, 3 tones fv = –8 dB, fs = –16 dB, fsb = –7 dB).

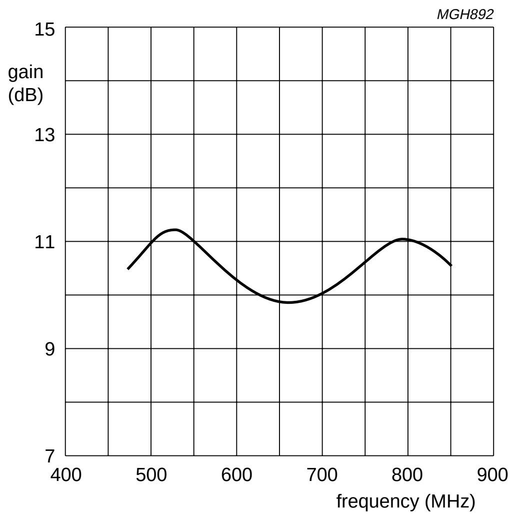


Fig.17 Gain versus frequency for the complete module (Po_sync = 40 W, 3 tones fv = –8 dB, fs = –16 dB, fsb = –7 dB).

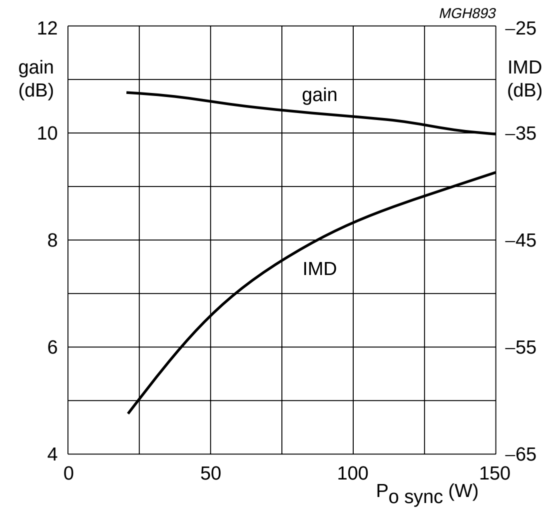


Fig.18 Gain & IMD versus Po_sync for the complete module (3 tones fv = –8 dB, fs = –16 dB, fsb = –10 dB).

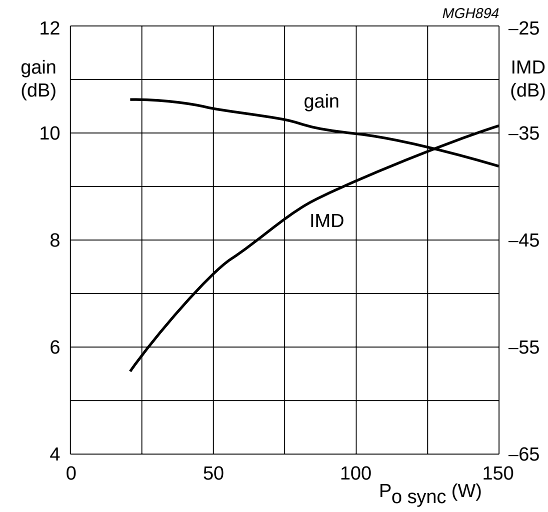


Fig.19 Gain & IMD versus Po_sync for the complete module (3 tones fv = –8 dB, fs = –16 dB, fsb = –7 dB).

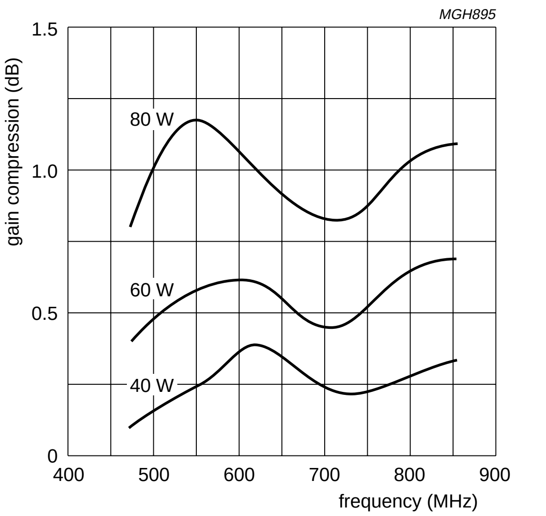


Fig.20 Gain compression for the complete module/Single tone measurement.

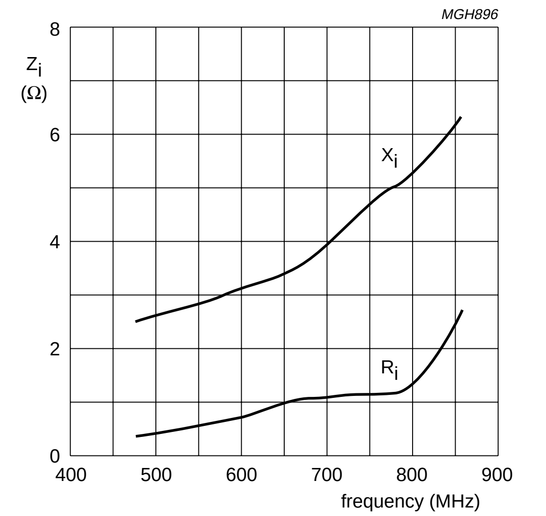


Fig.21 Input impedance (per section).

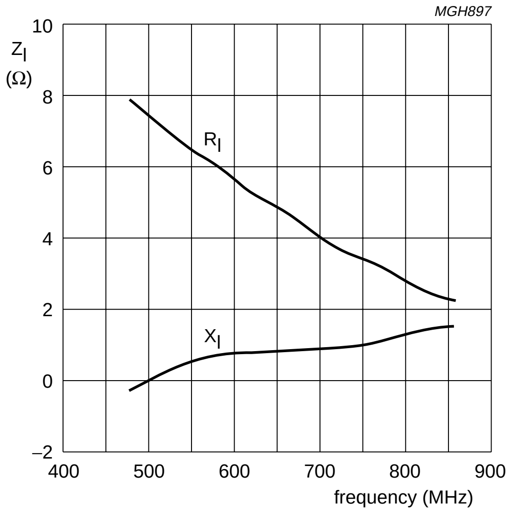


Fig.22 Output impedance (per section).

6 APPENDIX 1

Component list BLV589 module

COMPONENT	DESCRIPTION	VALUE	DIMENSION	12 NC
C1, C2, C3, C5, C6, C14, C15, C16, C17, C18	multilayer ceramic chip capacitor	15 nF	0805	2222 590 16629
C4, C19	solid aluminium capacitor	25 V/47 µF		2222 030 36479
C13, C22	solid aluminium capacitor	63 V/10 µF		2222 030 38109
C7, C8, C20, C21	multilayer ceramic chip capacitor	10 nF	0805	2222 590 16627
C9, C10, C11, C12, C23, C24, C25, C42	multilayer ceramic chip capacitor	100 nF	1206	2222 591 16641
C31, C33, C35, C39	multilayer ceramic chip capacitor (note 1)	12 pF		
C26, C37, C28, C41	multilayer ceramic chip capacitor (note 1)	9.1 pF		
C27, C29, C30, C32, C34, C36, C38, C40	capacitance trimmer REF: 9402 1 Firm: Tekelec	1 to 5 pF		
C27, C28, C29, C30	multilayer ceramic chip capacitor (note 1)	47 pF		
R1, R9	SMD resistor	220 Ω	0805	2322 734 22201
R2, R10	SMD resistor	1.8 Ω	0805	2322 734 21808
R3, R11	SMD resistor	2.7 kΩ	0805	2322 734 22702
R4, R12	SMD resistor	33 Ω	0805	2322 734 23309
R7, R8	SMD resistor	3.3 Ω	0805	2322 734 23308
P1, P2	RG4M08-102VM-TG Firm: muRata Potentiometer	1kΩ		
T1, T3	NPN transistor	BD139		9330 912 20112
T2, T4	double PNP transistor	BVC62		5322 130 60505
B1, B2, B3, B4	semi rigid coax balun UT70-25	ZO = 25 Ω ±1.5 Ω	70 mm	
L1, L2, L15, L16	Striline (note 2)	50 Ω	width 2 mm/length 30.6 mm	
L3, L4	Striline (note 2)	50 Ω	width 2 mm/length 9.5 mm	
L5, L6	Striline (note 2)	32.4 Ω	width 4 mm/length 3 mm	
L7, L8, L9, L10	Striline (note 2)	16.2 Ω	width 9.5 mm/length 2.6 mm	
L11, L12	Striline (note 2)	35.7 Ω	width 3.5 mm/length 3.4 mm	
L13, L14	Striline (note 2)	50 Ω	width 2 mm/length 13.9 mm	
L17	Striline (note 2)		width 1 mm/length 120 mm	

Notes

1. ATC capacitor type 100 A or capacitor of same quality.
2. Printed-circuit board Firm: Rogers ULTRALAM 200 (B0300M1046QB) (ε_r = 2.55) thickness = 0.76 mm.

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