APPLICATION NOTE

50 W base station power amplifier for DCS1800 and PCS1900

AN98024

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CONTENTS

1 ABSTRACT

In the fast emerging market of wireless communications, ease of design, high performance and low production costs are important design key parameters. This paper describes a 50 W modular base station power amplifier design for DCS1800 and PCS1900. The low cost reliable concept, that allows for very fast design cycles, consists of a 50 W power transistor driven by a power module and a low cost wide band transistor. The design is realised on a low cost substrate material and, at 26 V supply voltage, an overall gain larger than 47 dB has been reached at 50 W continuous wave output power.

2 INTRODUCTION

This paper will discuss the realisation of a 3 stage silicon bipolar 50 W RF line up solution for DCS1800 (1805 to 1880 MHz) and PCS1900 (1930 to 1990 MHz) (GMSK modulation). As a target, the minimum overall gain was set to 47 dB, corresponding with 1 mW input to achieve 50 W (+47 dBm) RF output power into a 50 Ω load. 26 V supply voltage and a bias/switching voltage of 5 V are assumed to be available in base station power supplies. The low loss and low cost printed-circuit board used, is a Rogers RT4000 series epoxy based board (32 mils) with enhanced RF performance compared to FR4.

The design maintains the possibility to test each stage separately as well as the overall performance.

The gain criteria for the line up is defined as follows: pre-driver gain larger than 15 dB, driver gain larger than 24 dB and final stage gain larger than 8 dB. These requirements can be obtained using the following Philips components (see Fig.1): stage 1: BFG425W wide band transistor, stage 2: BGY1816 or BGY1916 power module (depending on the frequency band) and stage 3: BLV2046 Si power transistor. In the following paragraphs these devices will be discussed in detail, the final paragraph will discuss the full line up with measurement results.

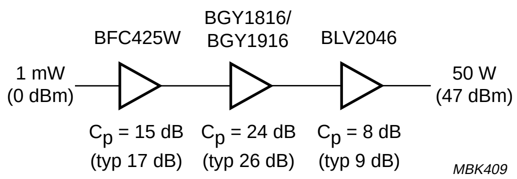

Fig.1 The 50 W line-up.

The pre-driver is biased in class A and matched for wide band operation over 1800 to 2000 MHz (no tune design). The 5 V supply powers the BFG425W and can switch the bias circuit of the module and final amplifier on/off e.g. for trouble shouting of the base station. The module is factory optimised for gain, efficiency and output power for the DCS (BGY1816) and PCS (BGY1916) band with internal biasing circuitry (no tune design). With only design time necessary for the final amplifier (minimum tuning), a quick and cheap base station power amplifier can be designed.

Nominal operating collector efficiency for the module is 35% at 16 W. Bearing this in mind and a 45% typical efficiency of the BLV2046, the overall line-up efficiency is 35% at 50 W.

3 PRE-DRIVER (BFG425W)

The BFG400W series wide band silicon transistors are using Double Poly Silicon technology. With a Ft over 20 GHz, high gain and low noise properties, the BFG400W series can be used for many applications.

To drive the module it is calculated that 20 mW output power is required. The BFG425W is the best choice in the BFG400W series to accomplish this target. With it's small footprint (typ. 2.0 × 1.25 mm, SOT343R, see Fig.2) and SMD components, a compact pre driver can be build for the module to keep valuable board space to a minimum and take advantage of pick and place machines during production.

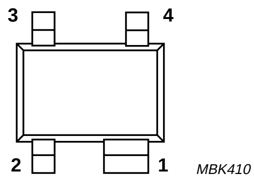

Fig.2 The SOT343R package.

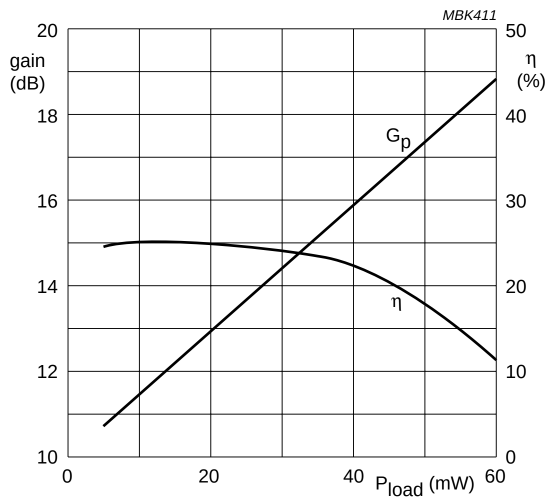

Fig.3 Gain and efficiency of BFG425W.

Biased in class A, the BFG425W is set to 30 mA and V_{CE} = 4 V, S parameters were measured and analysed for stability, matching and gain flatness. Computer simulations (HP-MDS) calculated the necessary matching component values and topology, optimized for 1800 to 2000 MHz band. Calculations/measurements proved sufficient bandwidth, which allows a design without tuning in production.

Summary of results:

Table 1 The results of the BFG425W

BFG425W	RESULTS	CONDITIONS
Gain	15.0 dB	Pload = 20 mW
P1 dB	45 mW	
Efficiency	33%	Pload = 45 mW
ΔGain vs. Frequency	<1 dB	
ΔGain vs. Pload	<1 dB	
Return loss in	<–15 dB	
Return loss out	<–15 dB	

Analysis has proven the BFG425W to deliver sufficient output power and gain to drive the module and final amplifier without running into compression, see Fig.3.

4 DRIVER (BGY1816/BGY1916)

As driver, a power module is used to boost the pre-driver signal sufficiently to drive the final amplifier. Running from a 26 V rail (and 5 V bias) the module can easily generate 16 W of RF power into a 50 Ω load with a gain of 26 dB.

Advantages for using a module are the 50 Ω input and output impedance, the small size and the fact that no tuning is required in production (thus saving production time), all of these reducing Time to Market in both design and production phase of the complete amplifier. In addition the very competitive price of the module is an advantage.

Two modules are available, an 1800 MHz (BGY1816) and a 1900 MHz (BGY1916) version, each factory optimised for output power, gain flatness and efficiency for their particular frequency bands.

AIN is used as substrate carrier for all modules, to eliminate the hazardous BeO for power devices and to keep our environment safe. Al_2O_3 is not preferred in these modules as the temperature handling is roughly 10 times worse than AIN and inserts are necessary for heat sinking for the power related transistors. All traces are thin film, gold metallized, on the AIN substrate, thus guaranteeing a consistent product during production.

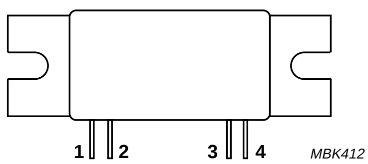

Fig.4 The SOT365 package.

The module consists of 3 stages silicon bipolar transistors. The package used is a SOT365 (16.5 × 48.0 mm, see Fig.4). The first stage is biased in class A to obtain high gain, linearity and a constant 50 Ω input impedance. The second and final stages are biased in class AB to increase the efficiency.

Each transistor is internally biased with a temperature compensated network. With these networks it is possible to adjust each individual transistor during production (if necessary) to assure specified gain expansion over power sweep and temperature range up to 85 °C.

An equaliser matching network between first and second stage is placed to control the gain slope over frequency. All RF-related dies are pre-matched with MOS capacitors to minimise component losses and guarantee (constant Q) gain performance during production. The matching networks consists of 0603 capacitors and distributed inductors. The final stage uses a collector matching network to improve broadband performance and efficiency. The final stage consists of 4 dies in parallel, each die capable to produce 6 W of RF power, thus producing 24 W of RF power in saturation. IR scans proved during RF operation (16 W) and under load mismatch condition (VSWR 1 : 5, all phases) that the junction temperature of any die remains well under 170 °C with a Tmb equal to 85 °C, necessary to guarantee module reliability and MTBF. Figure 5 shows the typical gain and efficiency performance of the BGY1816 module.

Summary of results:

Table 2 The results of the BGY1816

BGY1816	**RESULTS**
Gain	26 dB (typical, min spec 24 dB)
Efficiency	>30% @ 16 W
Psaturation	>22 W
Gain expansion	<1 dB
Gain ripple	<2 dB
DIMD	<–55 dBc (16 W, –40 dBc) @ 100 kHz
RIMD	<–55 dBc (16 W, –35 dBc) @ 100 kHz
IMD	<–23 dBc @ 16 W PEP @ 100 kHz
Ruggedness	1 : 5 all phases
Return loss input	<–15 dB
2nd Harmonic	<–40 dBc @ 16 W

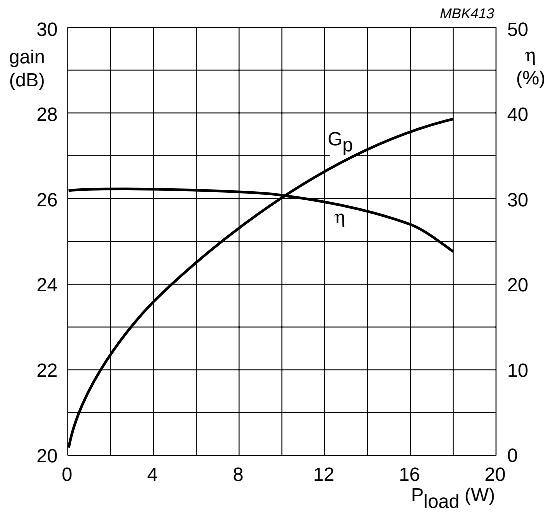

Fig.5 Gain and efficiency of BGY1816.

Due to it's compact size and high degree of integration, one saves valuable board space and keeps component costs and count down. Using an external pre-driver with this module a cheap and small line up can be designed for a micro cell or used as driver for a final amplifier.

5 FINAL STAGE (BLV2046)

As final stage the BLV2046 is used. The BLV2046 is a silicon NPN planar epitaxial transistor used in a class-AB common emitter configuration, capable of 50 W RF power with more than 8 dB gain and an efficiency larger than 40% in the 1805 to 1990 MHz band.

The transistor dies use a sub-micron interdigitated bipolar technology. To improve thermal stability and ruggedness, emitter ballasting resistors are used in combination with high breakdown voltages (typ. 80 V with open emitter).

The BLV2046 has internal input and output matching networks using MOS capacitors which allow an easier matching design for wide band circuits, and guarantee constant Q, gain performance and impedance behaviour during production. The TiPtAu top metallization ensures an excellent MTBF.

The encapsulation is a SOT460A package (22.9 × 6.3 mm) with a ceramic cap. The SOT460A (see Fig.6) is a non hermetic low cost package with very good thermal characteristics and low emitter inductance by means of metallized via holes.

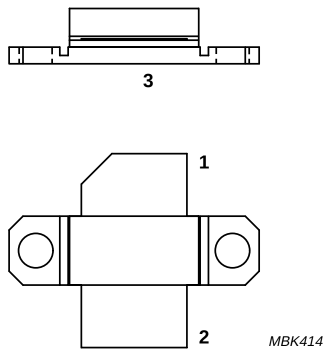

Fig.6 The SOT460A package.

To achieve the best compromise between gain expansion/linearity and efficiency, the BLV2046 is biased at 26 V with a quiescent current of 600 mA.

Summary of results:

Table 3 The results of the BLV2046

BLV2046	TYPICAL	CONDITIONS
Gain (dB)	8.5	at 50 W output power
Efficiency (%)	45	at 50 W output power
Gain expansion (dB)	<1	1805 to 1880 MHz
Gain ripple (dB)	<1	1805 to 1880 MHz
IMD (dBc)	–35	Pload = 50 W (PEP) @ Icq = 200 mA

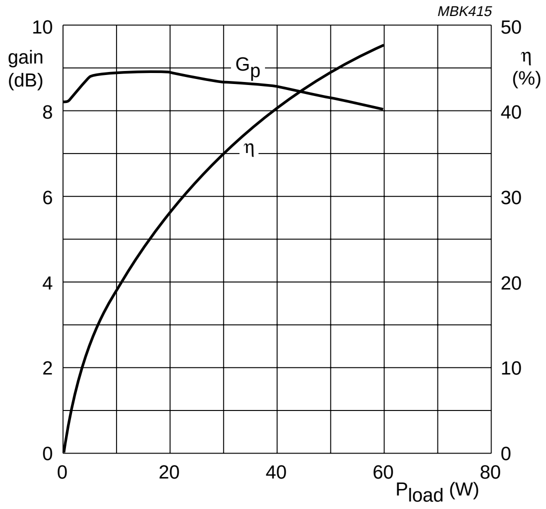

Fig.7 Gain and efficiency of the BLV2046.

The BLV2046 has proven to be a powerful single ended 50 W NPN silicon bipolar transistor as final stage to achieve a low cost, easy design, high efficiency and high gain amplifier. Although specified a 50 W transistor at 26 V supply, the transistor can easily generate 60 W of RF power with a (typical) gain of 8 dB and a (typical) efficiency of 45% into a 50 Ω load, see Fig.7.

6 FULL LINE-UP RESULTS

The full line up has been build on Rogers RT4000 series (32 mils), an epoxy based circuit board, closely resembling printed-circuit board used in the field. The line up exists of two boards one containing the pre-driver and driver, the second accommodates the final amplifier.

The two circuit boards are mounted on a brass base plate, which is mounted on a heat sink using forced air cooling.

As all inputs and outputs of the 3 stages are 50 Ω, the individual stages can easily be checked for performance or trouble shooting.

On the (pre)driver board a provision is made for a 5 V stabilising IC, powerful enough to feed the BGF425W, BGY1816 and the bias of the BLV2046.

During the tests the mounting base plate temperature was measured between 55 and 60 °C, T_{amb} = 24 °C.

As mentioned earlier, the line-up is a practically no tune design. To obtain maximum performance from the loading circuit of the BLV2046 one tuning capacitor has been used. Measurements of the output returnloss proved better then –10 dB.

Summary of results:

Table 4 The results of the total line-up

FULL LINE UP	RESULTS	CONDITIONS
Gain	>50 dB	Pload = 50 W
Efficiency	>36%	Pload = 50 W
∆Gain vs. frequency	<2 dB	1805 – 1880 MHz
∆Gain vs. Pload	<1 dB	Pload 1 – 50 W
Tmb	57 °C	T_{amb} = 25 °C
Return loss in	<–15 dB	Pload = 50 W
Return loss output	<–10 dB	
2nd Harmonic	<–35 dBc	

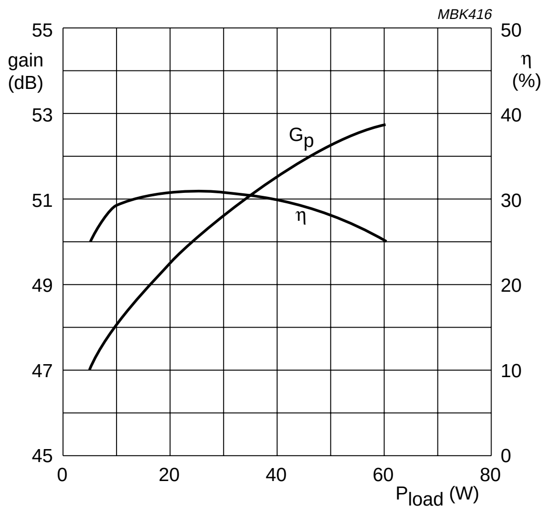

Fig.8 Gain and efficiency of the line-up.

7 CONCLUSION

A 50 W full line up base station amplifier has been presented for the PCS/DCS band. It has been proven that the line up can generate 50 W of RF output power with an overall gain larger than 47 dB with an overall efficiency of 36%. No instabilities were noticed in spite of the large gain. Gain flatness and gain expansion are smaller than 2 dB over the band and power range.

Using the combination BFG425W, BGY1816/BGY1916 and BLV2046 one can design a low cost PCS/DCS amplifier in a very short design cycle time. It is easy to manufacture, requires minimum tuning and small circuit board surface area.

8 LINE UP LAYOUT

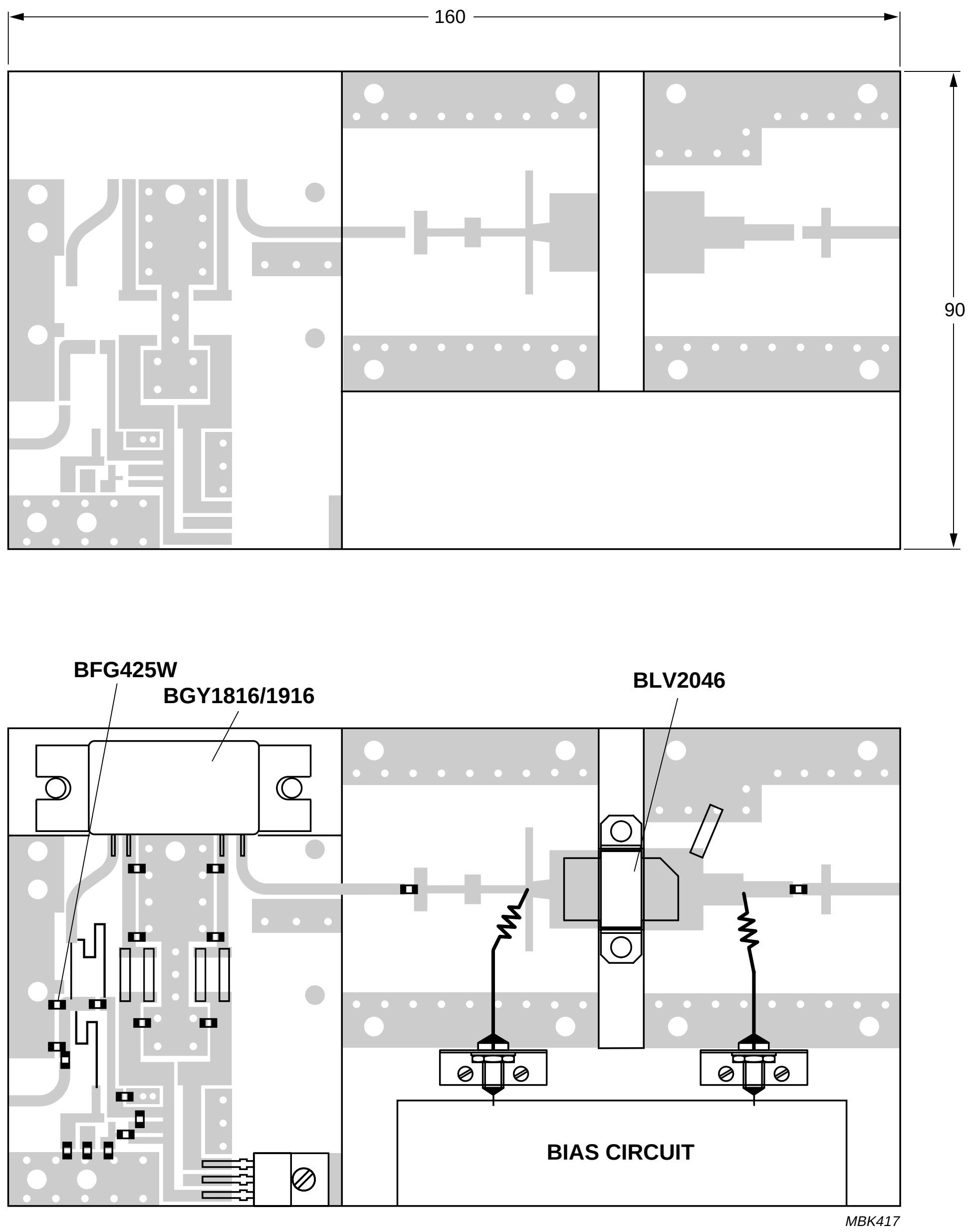

Fig.9 Layout of the line-up.

Remark: Fig.9 shows the layout of the 50 W line-up used to test the overall performance. It is meant as a demo-board, giving maximum flexibility for evaluation. For production the size of this board (160 × 90 mm) can easily be reduced by 50%.

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