APPLICATION NOTE

A linear broadband 12 W amplifier for band IV/V TV transposers based on the BLV58

AN98028

Philips
Semiconductors

CONTENTS

1 ABSTRACT
2 INTRODUCTION
3 GENERAL CONSIDERATIONS
4 AMPLIFIER DESCRIPTION
5 LOAD NETWORK DESIGN
6 INPUT NETWORK DESIGN
7 BIASING
8 AMPLIFIER TUNING
9 AMPLIFIER PERFORMANCE
10 CONCLUSION
11 LIST OF COMPONENTS BLV58 BROADBAND AMPLIFIER

1 ABSTRACT

A broadband linear amplifier design is presented, suitable for application in TV transposers operating in bands IV and V (470 – 860 MHz). The design is based on a single BLV58 bipolar transistor in push pull configuration. Results at the published class A bias point (25 V/3.2 A) for the BLV58 include 12 W peak sync output power at –52 dB three tone IMD level and 11 dB gain in the (470 – 860) MHz range. Po-sync level improved by 4 W at 26 V/3.8 A.

2 INTRODUCTION

For solid state TV transposers Philips introduced the BLV58, a bipolar linear push-pull power transistor designed to operate in the 470 – 860 MHz range. Narrowband intermodulation distortion level is < –45 dB and powergain >10 dB at 860 MHz.

In this application note an amplifier design is to be discussed which demonstrates the broadband capabilities of a BLV58 in push-pull configuration. Special attention is paid to the broadband tuning procedure for good and reproducible linearity. Fullband performance data are presented measured with two different 3-tone systems at two bias levels.

3 GENERAL CONSIDERATIONS

UHF solid state TV transposers for service in band 4 and 5 are commonly realized using broadband amplifiers which are capable to handle both bands. The typical frequency range is 470 – 860 MHz or channel 21 to 69. Some transposers also service additional channel at the high end of band V. But these are quite rare. High powers are obtained by combining power from several lower power modules. The basic low power module consists of two push-pull amplifier combined using 3 dB quadrature hybrids. The push-pull amplifier is designed for flat gain response by allowing input mismatch which gradually improves with frequency. To have good input return loss throughout the band two of these push-pull amplifiers are combined using 3 dB quadrature hybrids.

Low and flat intermodulation distortion (IMD) is required throughout the band. As linearity performance is strongly determined by the collector loading, special attention must be paid to the tuning procedure for obtaining minimum and reproducible IMD response.

The class-A bias point used for this design is that published in the datasheet. However broadband performance has been evaluated at elevated bias levels within the DC safe operating area. Some means of bias temperature compensation is applied to achieve thermal stability.

4 AMPLIFIER DESCRIPTION

Figure 1 shows the schematic of the total push pull amplifier without the biasing circuitry. It utilizes mixed lumped and distributed low pass/high pass impedance matching sections for maximum bandwidth. The low pass sections consists of shunt capacitors and series transmission lines. The high pass sections consist of series capacitors and short circuited stubs. The stubs also form a part of the balance to unbalance(balun) transformers. The length of the stubs is less than 1/8 wavelength at 470 MHz. Balance is maintained by loading both the outer and inner conductors with identical stubs. The series capacitors also act as DC blocking.

The board material used for this amplifier is ULTRALAM 2000 from ROGERS Corp. which has a good price/performance ratio and good mechanical stability. It is a PTFE based substrate with ε_r = 2.55 and 30 mils (0.76 mm) thickness.

The printed-circuit board layout is shown in Figs 2 and 3 shows the component layout diagram. The list of components is given on page 7.

5 LOAD NETWORK DESIGN

The theoretical design was based on load impedance data from the datasheet. The conjugate of the broadband load impedance for one section was modelled as shown in Fig.4. R represents the load resistance to obtain good linearity, C the effective output capacitance of the transistor and L the bonding wires and package lead inductance.

With the component values given in Fig.4 a good broadband fit is obtained with the published load impedance. Minimum distortion is obtained when the effective load impedance presented to the chip is real or nearly real as possible.

A semi-low pass Chebychev matching network with three sections combined with a single high pass section is used to match R to 25 Ω. C and L of the model are absorbed in the matching network forming one section of the low pass. The initial component values were optimized for good full band match using CAD techniques.

6 INPUT NETWORK DESIGN

For achieving gain versus frequency levelling a lossless impedance matching network is applied which provide variation of reflected input power as a function of frequency. The BLV58 exhibit an approximate –4 dB per octave powergain roll off in the frequency range of interest. As solving the problem of impedance matching with drive compensation for gain levelling is difficult to solve analytical, CAD techniques were used to solve the problem. The initial low pass/high pass matching network for the input was first designed to have perfect match at the highest frequency of band V. With the component values found a computer optimization run was done to find the right values which provide the appropriate mismatch versus frequency while maintaining the best match at the highest frequency.

In order to get rid of the mismatch seen by the driver, two stages combined using 3 dB quadrature hybrids can be used which will result in minimum mismatch versus frequency. For evaluation of the single stage amplifier design a 3-port circulator was used to isolate the drive from the reflective input.

7 BIASING

The bias network were designed for spurious free operation. For stability in the low MHz region, basebias to collectorbias coil inductance ratio was chosen high. The minimum ratio strongly depending on Hfe, Cob and Ce of the device is approximately 1.5 for the BLV58. A transmission line stub is used for the collectorbias and a microchoke for the basebias. RF decoupling capacitors are added to provide low impedance to ground for all frequency components. Linearity is affected slightly by this in a positive way.

A bias circuit which achieves thermal stability through feedback techniques is used. The circuit applied is shown in Fig.6. The PNP(Q1) acts as a current source for the base of the BLV58. R1 controls the collector current drawn by the BLV58 and R2 sets the minimum of it. R3 establishes the operating bias point of the PNP. R4 sets the collector current drawn by the BLV58. R5 reduces the power dissipation in the PNP by taking a large part of the voltage drop across it. R6 reduces the effects of leakage current on the bias of the RF device. The diode (D1) thermally compensates the PNP’s base-emitter voltage. A major part of the power consumption is concentrated in R4. The voltage drop across R4 should therefore be minimized (<1 V).

8 AMPLIFIER TUNING

Amplifiers with linearity requirements can be tuned in two ways. Although it will not always result in minimum distortion the first method optimizes for broadband gain using small signal techniques.

In the second method, loading for minimum distortion is emphasized. The tuning procedure adopted for this design consists of two phases. First the output network is tuned for the correct load impedance. Secondly the input network is tuned to obtain flat gain with the previously obtained load fixed. This off course will not necessarily results in the highest possible broadband gain obtainable from the device. The BLV58 requires a slightly different load impedance for minimum distortion than for maximum gain. The tuning procedure used is described below.

To obtain collector load tuning for minimum distortion a passive device(dummy) is used which represents the conjugate of the load as shown in Fig.4. Figure 5 shows the practical realization of the dummy device. An empty package of the BLV58 (SOT289) serves as carrier for the chip components R and C. Part of the printed line on the BeO die together with the collector leads form the required inductor L. The IMD performance of the BLV58 in a narrowband 860 MHz circuit, tuned with this dummy, was excellent. By inserting the dummy in place of the BLV58 without any voltages applied, the output network was tuned for minimum returnloss on small signal basis. After some practical optimization of the initial output network, the result obtained was as shown in Fig.4. Returnloss is better than –12 dB throughout the band and was considered the best obtainable with the applied matching technique. For the remaining part of the tuning procedure the output was not altered anymore. After replacing the dummy with a BLV58 biased into class-A, the complete amplifier was tuned for flat small signal gain by means of the input network only. Again some optimization of the input network was required too, to obtain the result as shown in Fig.9. The small signal gain is better than 11 dB throughout the band with a 0.6 dB ripple. Figure 10 contains the input response showing the mismatch versus frequency for gain levelling.

The output response is shown in Fig.7. A slightly increased bandwidth at the cost of inband returnloss is observed.

9 AMPLIFIER PERFORMANCE

The first class-A bias point for linearity evaluation was taken from the datasheet, i.e. V_{CE} = 25 V and I_{CQ} = 3.2 A. Based on the maximum published junction to case thermal resistance of 1.5 K/W, the maximum case temperature for zero RF drive is 80 °C. Improved linearity can be obtained at higher levels of collector voltage and current as long as the ratings (V_{CEmax} = 27 V and IC_{max} = 4 A) are not exceeded. As an example linearity has also been measured at V_{CE} = 26 V and I_{CQ} = 3.8 A. Maximum case temperature for zero drive at this bias point is 52 °C.

Linearity evaluation is done by comparing the intermodulation distortion products (IMD’s) generated by a multi-tone test signal to a given reference level. Three tones are used to simulate television signals according two specifications for tone levels and spacings. The first is according the old German Post Office (GPO) specification, given in Fig.11, and the second according the new specification, given in Fig.12. The latter results in a somewhat lower Po-sync at same IMD level.

The test setup used for linearity evaluation is shown in Fig.13. To obtain good accuracy, the test signal must have a superior IMD to the levels to be measured. This has been achieved by amplifying each tone separately before combining them. Good isolation between the individual tones is obtained by using circulators as depicted in Fig.13. An additional circulator is added to isolate the drive from the reflective input of the amplifier.

Broadband measurement data are presented in the graphs of Figs 14 to 21. IMD and powergain are given at several output power levels to accommodate performance assessment for specific power levels. At an IMD level of –52 dB commonly specified for transposers, output power levels are as listed below (interpolated values):

1. 3-tones: –8/–16/–7 dB
   a) Po-sync ≥ 12 W @ 25 V/3.2 A
   b) Po-sync ≥ 16 W @ 26 V/3.8 A
2. 3-tones: –3/–20/–10 dB
   a) Po-sync ≥ 11 W @ 25 V/3.2 A
   b) Po-sync ≥ 15 W @ 26 V/3.8 A

So, Po-sync increases by 4 W typically or the second bias point and decreases by 1 W for the new tone specification. The power gain is approximately 11 dB for both cases with a ripple of 0.5 dB. Less gain compression is observed for the second bias point.

10 CONCLUSION

An amplifier design has been presented based on a single BLV58, capable of operating in full band IV/V with flat gain and good linearity. Design and tuning procedure described result in good and reproducible broadband behaviour. High gain (11 dB) and good linearity (Po-sync ≥ 12 W @ –52 dB) has been obtained at the published class-A bias point (25 V/3.2 A). At a higher bias point (26 V/3.8 A). Po-sync improves by 4 W.

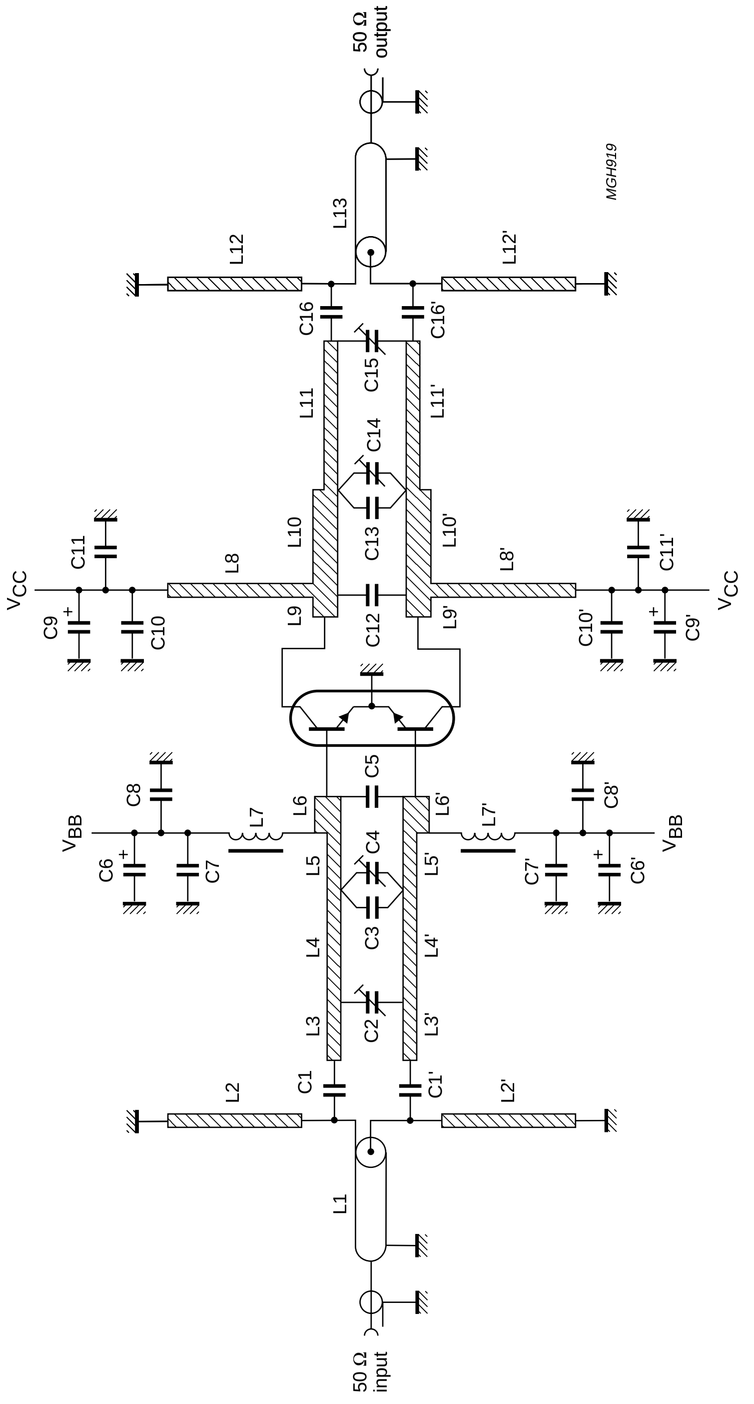


Fig.1 Circuit Diagram of Broadband Amplifier.

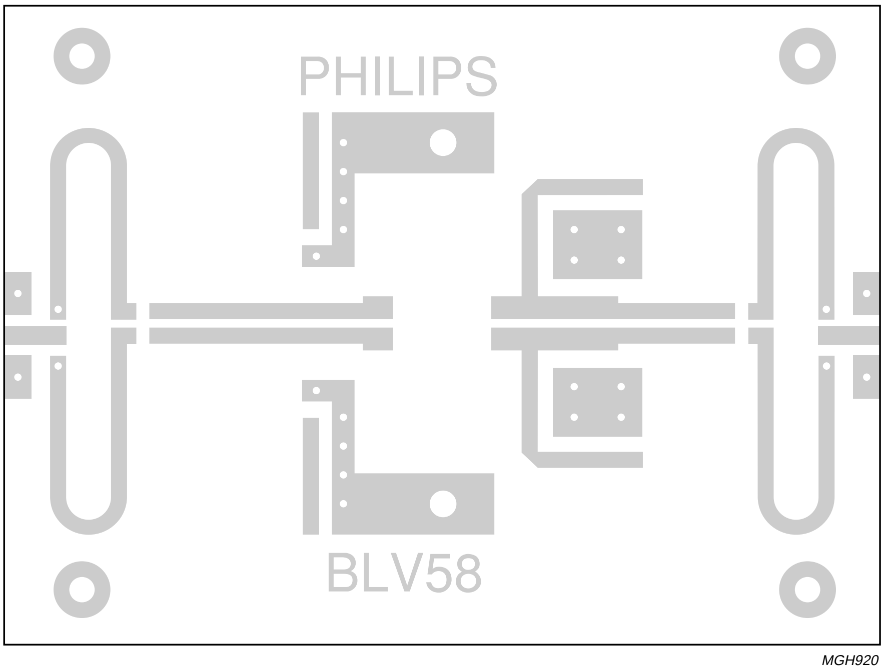


Fig.2 PC Board Layout (Not to Scale).

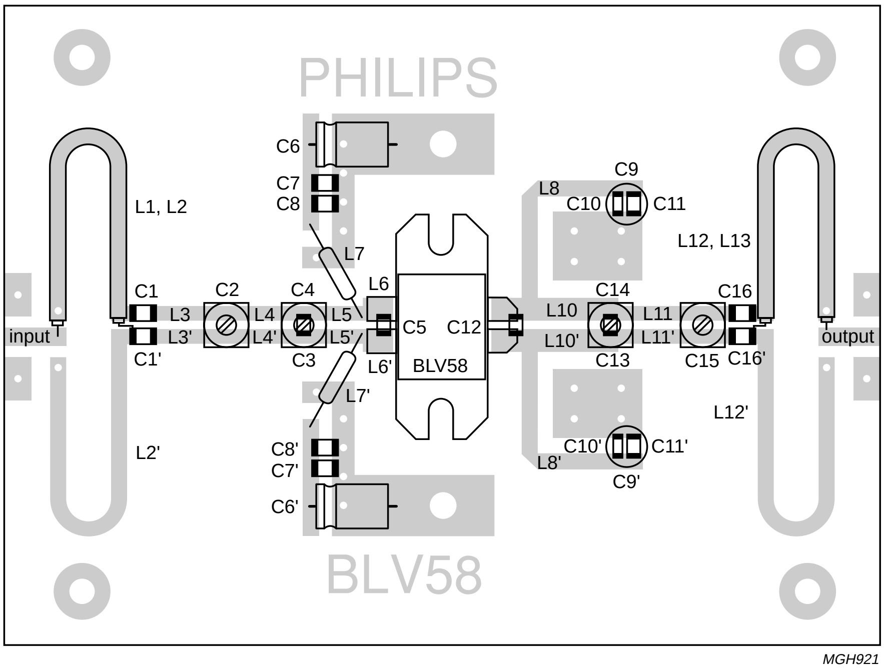


Fig.3 Component Layout Diagram.

11 LIST OF COMPONENTS BLV58 BROADBAND AMPLIFIER

Capacitors

C1 = C1’	11	pF	ATC 100B chip capacitor
C2 = C4 = C14 = C15	1.2 – 3.5	pF	Philips film dielectric trimmer
C3 = C13	6.8	pF	ATC 100A chip capacitor
C5	13	pF	ATC 100A chip capacitor
C6 = C6’	10	µF	63 V electrolytic capacitor
C7 = C7’ = C10 = C10’	100	nF	Philips chip capacitor
C8 = C8’ = C11 = C11’	100	pF	ATC 100B chip capacitor
C9 = C9’	2.2	µF	63 V electrolytic chip capacitor
C12	18	pF	ATC 100A chip capacitor
C16 = C16’	10	pF	ATC 100B chip capacitor

Transmission-lines/inductors

L1 = L13	50	Ω	Semi-Rigid Coax: L = 50 mm; OD = 2.2 m
L2 = L2’ = L12 = L12’	53	Ω	Stripline: L = 50 mm; W = 1.9 mm
L3 = L3’	61	Ω	Stripline: L = 11.2 mm; W = 1.5 mm
L4 = L4’	61	Ω	Stripline: L = 10.5 mm; W = 1.5 mm
L5 = L5’	61	Ω	Stripline: L = 6.3 mm; W = 1.5 mm
L6 = L6’	41	Ω	Stripline: L = 3.7 mm; W = 2.8 mm

L7 = L7’	470	nH	RF micro-choke
L8 = L8’	53	Ω	Stripline: L = 28 mm; W = 1.9 mm
L9 = L9’	41	Ω	Stripline: L = 3.5 mm; W = 2.8 mm
L10 = L10’	41	Ω	Stripline: L = 12 mm; W = 2.8 mm
L11 = L11’	61	Ω	Stripline: L = 12.5 mm; W = 1.5 mm

Coaxal Lines L1 and L13 are soldered on striplines L2 and L12 respectively. The same lengths of coaxial lines (centre conductor unused) are soldered on L2’ and L12’ respectively. It results in a lower characteristic impedance of the striplines, due to the increased effective thickness. The initial value of 53 Ω decreases the approximately 44 Ω.

PCB: ULTRALAM 2000, thickness = 30 mils, ε_r = 2.55.

The back side of the board is fully metallized and serves as ground plane. Plated through holes are used for grounding areas on the top side.

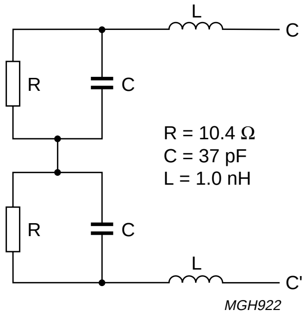


Fig.4 Equivalent Model for the Conjugate of the Load Impedance (Collector to Collector).

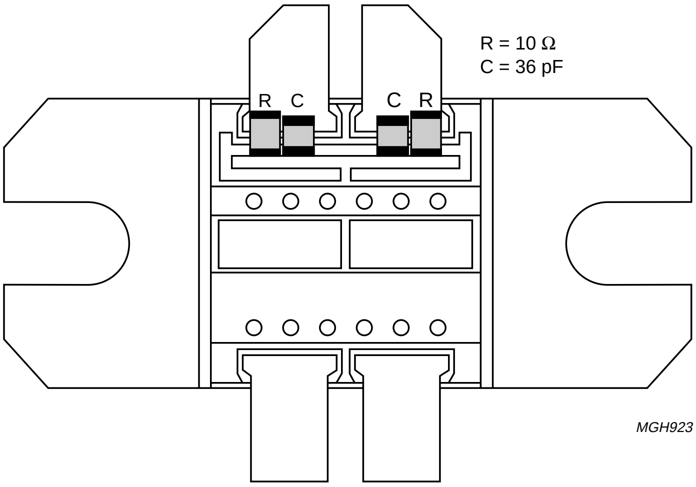


Fig.5 Passive Device (Dummy) for Load Tuning.

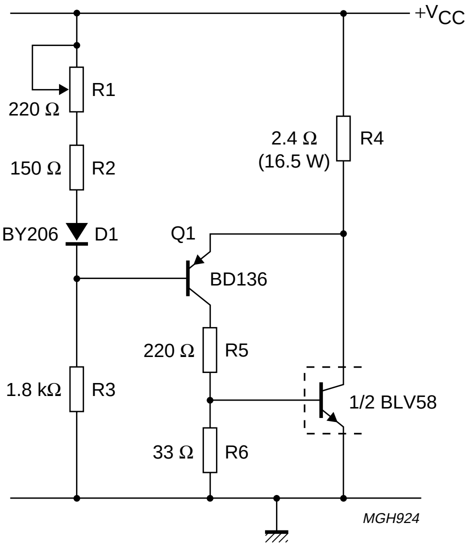
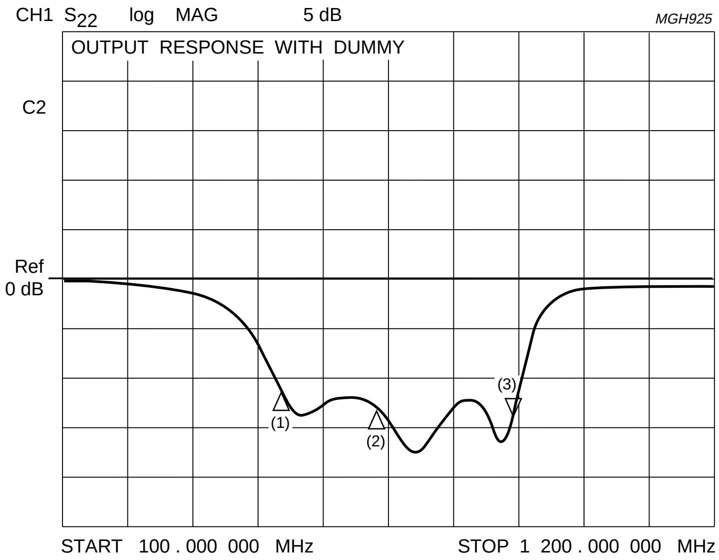
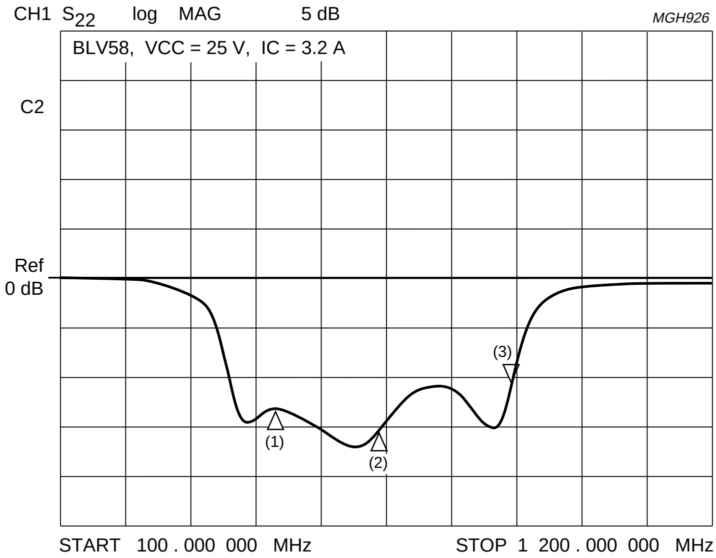


Fig.6 Class-A Bias Circuit for One Section.



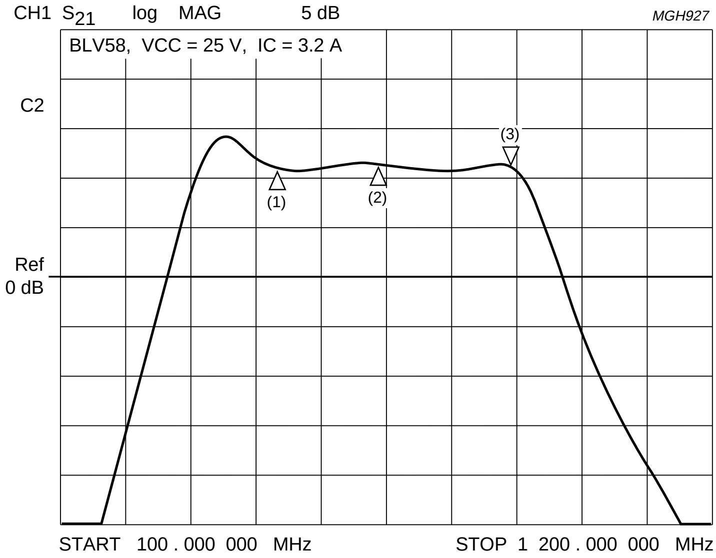
(1) −11.366 dB; 470 MHz.
(2) −13.365 dB; 636 MHz.
(3) −14.217 dB; 859 MHz.

Fig.7 Output Return Loss with Dummy Insert.



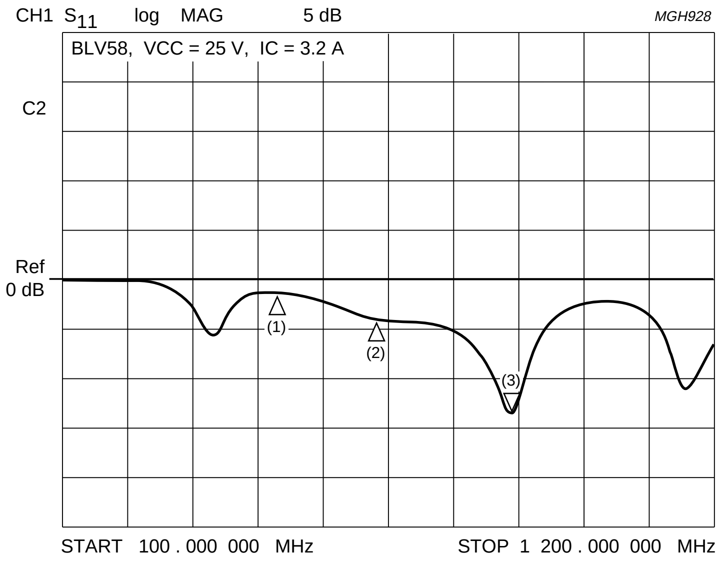
(1) −13.134 dB; 470 MHz.
(2) −15.409 dB; 636 MHz.
(3) −10.677 dB; 862 MHz.

Fig.8 Output Return Loss with BLV58.



(1) −10.959 dB; 470 MHz.
(2) −11.551 dB; 636 MHz.
(3) −10.979 dB; 862 MHz.

Fig.9 Small Signal Gain Response of Amplifier.



(1) –1.4169 dB; 470 MHz.

(2) –3.9376 dB; 636 MHz.

(3) –13.496 dB; 862 MHz.

Fig.10 Input Return Loss of Amplifier.

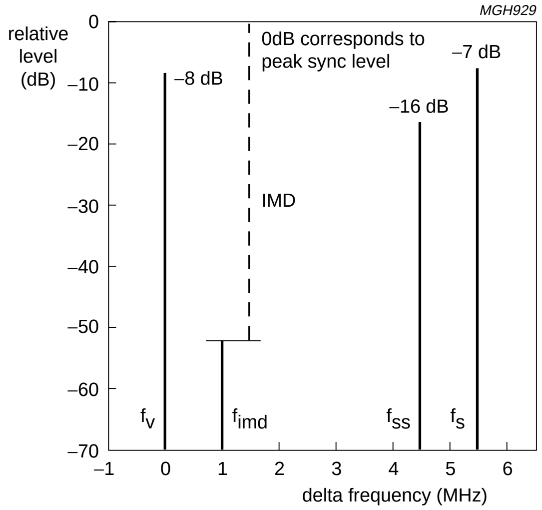


Fig.11 Three Tone Test used to Measure (IMD) According Old GPO Specification.

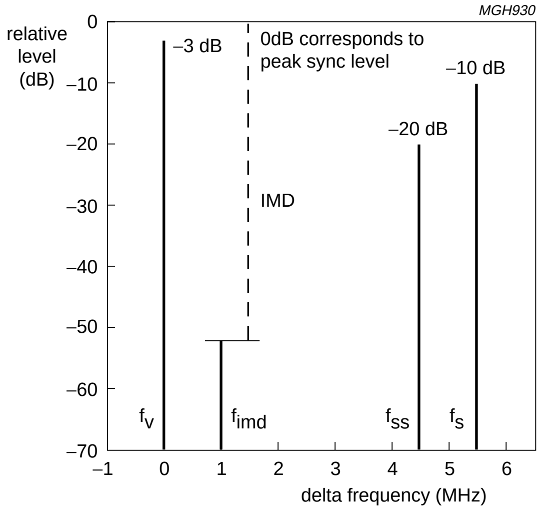


Fig.12 Three Tone Test used to Measure (IMD) According New GPO Specification.

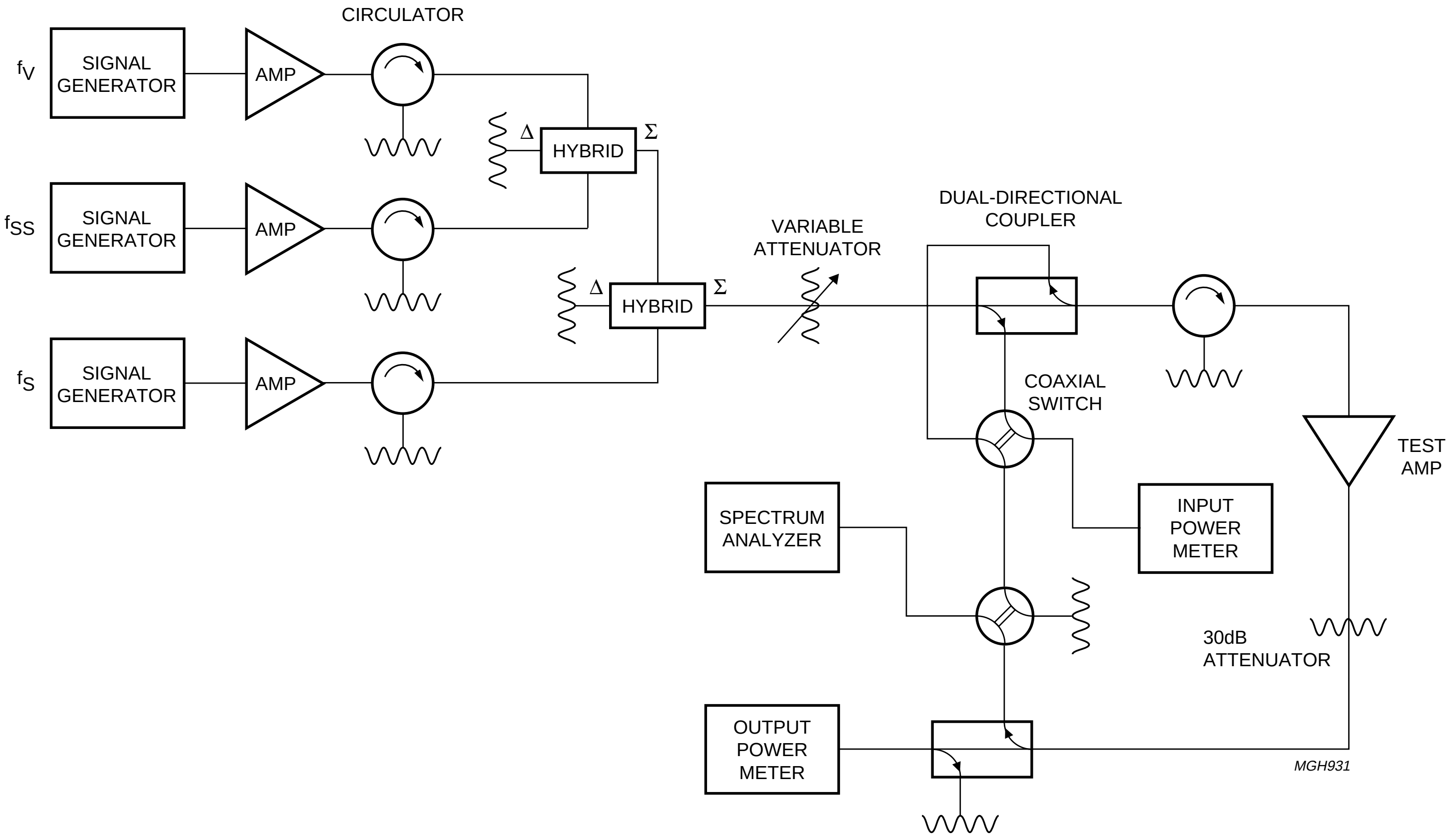
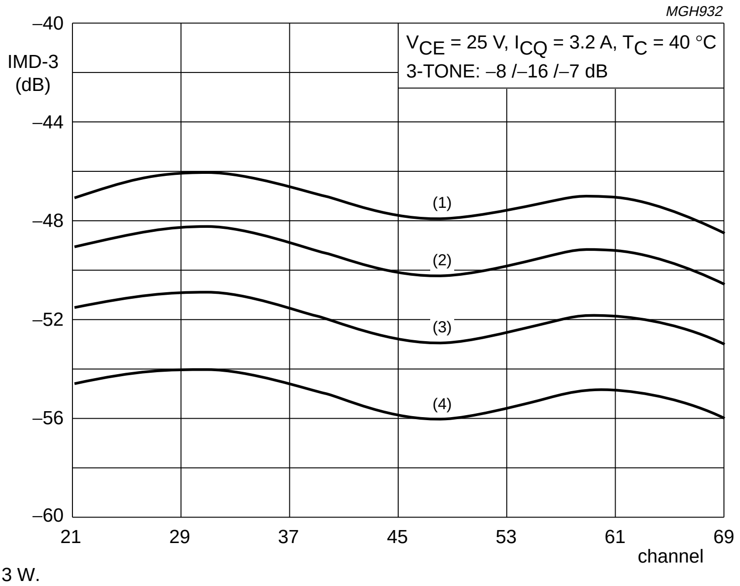
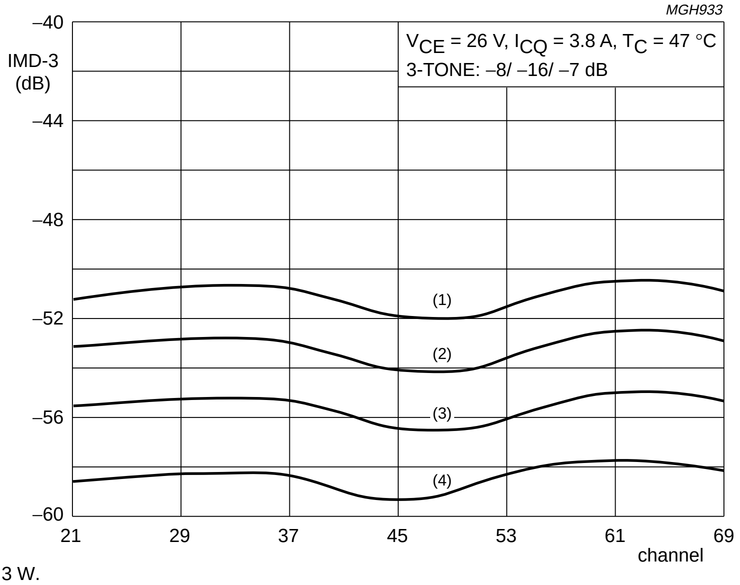


Fig.13 Three Tone Test Setup for Linearity Measurement.



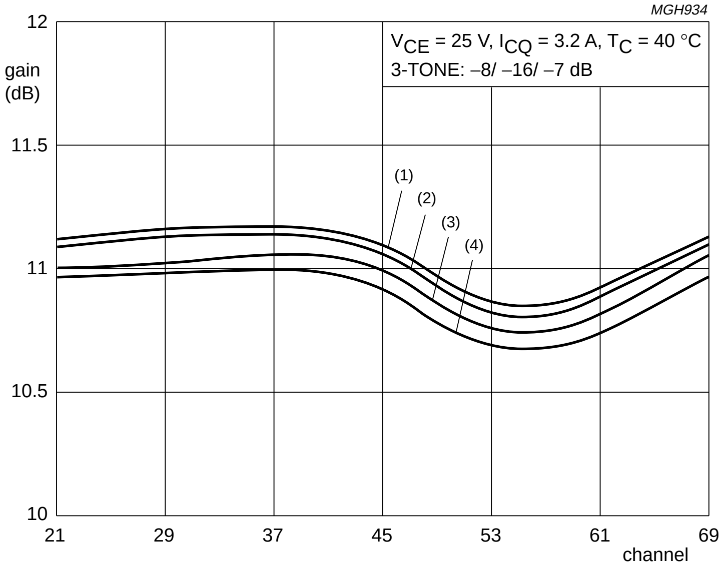
(1) Peak sync power = 18.3 W.
(2) Peak sync power = 15.7 W.
(3) Peak sync power = 13.1 W.
(4) Peak sync power = 10.4 W.

Fig.14 IMD versus Channel @ V_{CE} = 25 V and I_{CQ} = 3.2 A. According Old 3-Tone GPO Specification.



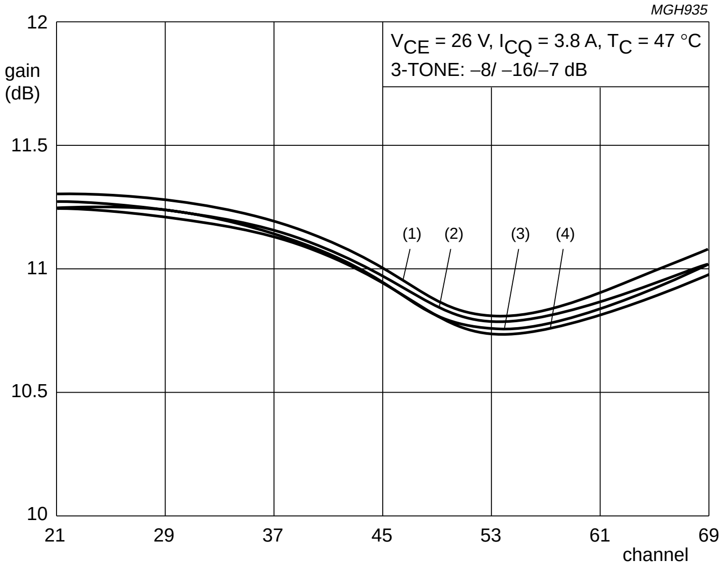
(1) Peak sync power = 18.3 W.
(2) Peak sync power = 15.7 W.
(3) Peak sync power = 13.1 W.
(4) Peak sync power = 10.4 W.

Fig.15 IMD versus Channel @ V_{CE} = 26 V and I_{CQ} = 3.8 A. According Old 3-Tone GPO Specification.



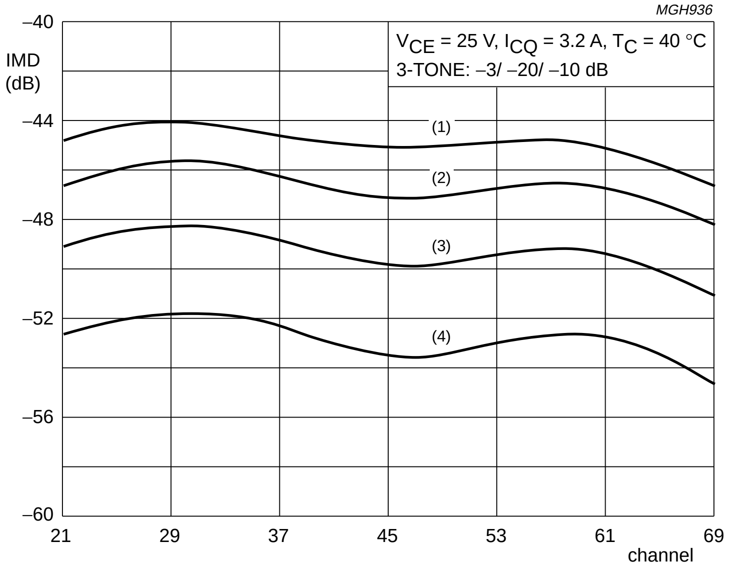
(1) Peak sync power = 10.4 W.
(2) Peak sync power = 13.1 W.
(3) Peak sync power = 15.7 W.
(4) Peak sync power = 18.3 W.

Fig.16 Gain versus Channel @ V_{CE} = 25 V and I_{CQ} = 3.2 A. According Old 3-Tone GPO Specification.



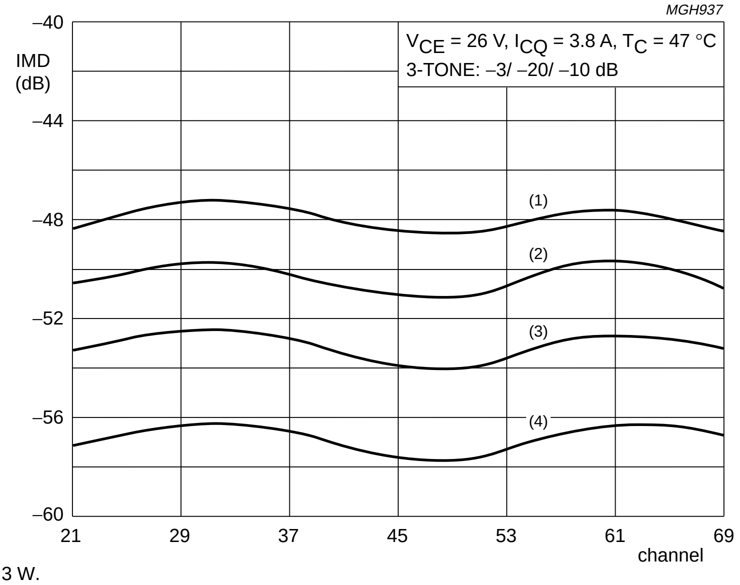
(1) Peak sync power = 10.4 W.
(2) Peak sync power = 13.1 W.
(3) Peak sync power = 15.7 W.
(4) Peak sync power = 18.3 W.

Fig.17 Gain versus Channel @ V_{CE} = 26 V and I_{CQ} = 3.8 A. According Old 3-Tone GPO Specification.



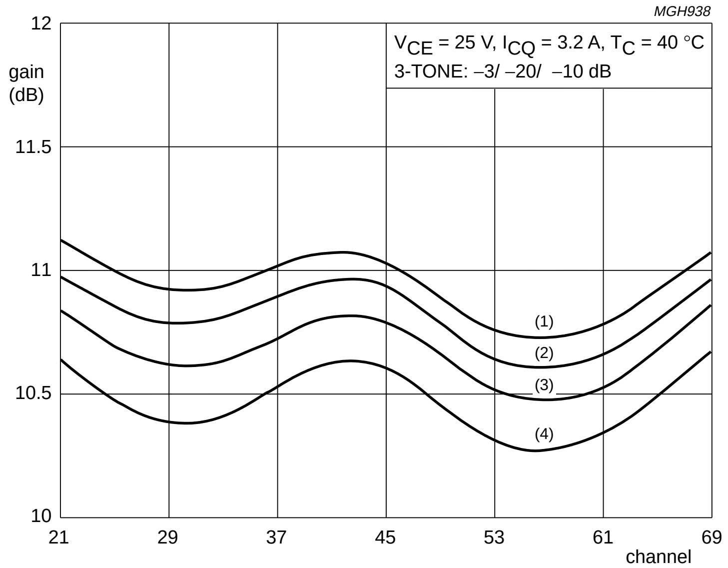
(1) Peak sync power = 21.3 W.
(2) Peak sync power = 18.0 W.
(3) Peak sync power = 14.7 W.
(4) Peak sync power = 11.5 W.

Fig.18 IMD versus Channel @ V_{CE} = 25 V and I_{CQ} = 3.2 A. According New 3-Tone GPO Specification.



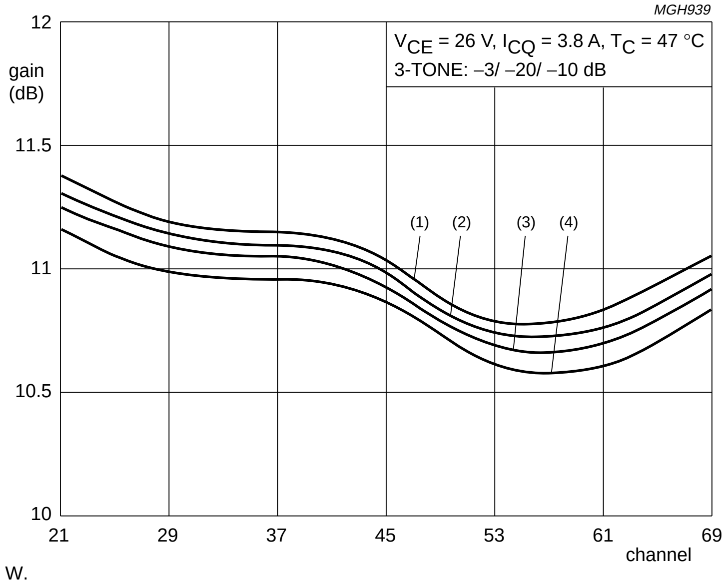
(1) Peak sync power = 21.3 W.
(2) Peak sync power = 18.0 W.
(3) Peak sync power = 14.7 W.
(4) Peak sync power = 11.5 W.

Fig.19 IMD versus Channel @ V_{CE} = 26 V and I_{CQ} = 3.8 A. According New 3-Tone GPO Specification.



(1) Peak sync power = 11.5 W.
(2) Peak sync power = 14.7 W.
(3) Peak sync power = 18.0 W.
(4) Peak sync power = 21.3 W.

Fig.20 Gain versus Channel @ V_{CE} = 25 V and I_{CQ} = 3.2 A. According New 3-Tone GPO Specification.



(1) Peak sync power = 11.5 W.
(2) Peak sync power = 14.7 W.
(3) Peak sync power = 18.0 W.
(4) Peak sync power = 21.3 W.

Fig.21 IMD versus Channel @ V_{CE} = 26 V and I_{CQ} = 3.8 A. According New 3-Tone GPO Specification.

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