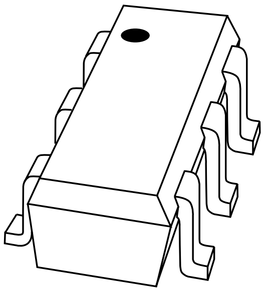
DATA SHEET



BF1102
Dual N-channel dual gate MOS-FET

Preliminary specification 1999 Jul 08

Philips
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FEATURES

- Two low noise gain controlled amplifiers in a single package
- Specially designed for 5 V applications
- Superior cross-modulation performance during AGC
- High forward transfer admittance
- High forward transfer admittance to input capacitance ratio.

APPLICATIONS

- Gain controlled low noise amplifier for VHF and UHF applications such as television tuners and professional communications equipment.

DESCRIPTION

The BF1102 is a combination of two equal dual gate MOS-FETs with shared source and gate 2 leads.
The source and substrate are interconnected. An internal bias circuit enables DC stabilization and a very good cross-modulation performance at 5 V supply voltage. Integrated diodes between the gates and source protect against excessive input voltage surges. The transistor has a SOT363 micro-miniature plastic package.

PINNING - SOT363

PIN	DESCRIPTION
1	gate 1 (1)
2	gate 2 (1,2)
3	drain (1)
4	drain (2)
5	source (1,2)
6	gate 1 (2)

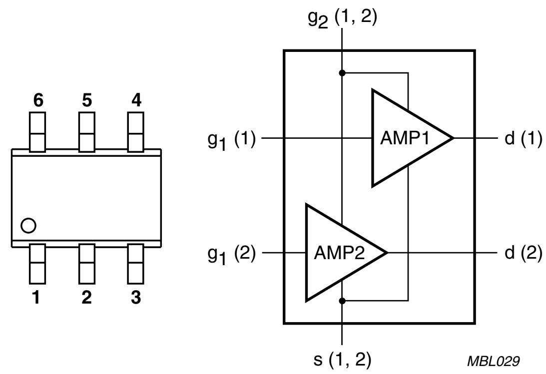


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per MOS-FET unless otherwise specified						
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current (DC)		–	–	40	mA
P_{tot}	total power dissipation	$T_s \leq 102$ °C; note 1	–	–	200	mW
$\lvert y_{fs} \rvert$	forward transfer admittance	$I_D = 15$ mA	–	43	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	$I_D = 15$ mA	–	2.8	–	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	30	–	fF
F	noise figure	f = 800 MHz	–	–	2.8	dB
X_{mod}	cross-modulation	input level for k = 1% at 40 dB AGC	100	–	–	dBμV
T_j	operating junction temperature		–	–	150	°C

Note

1. T_s is the temperature at the soldering point of the source lead.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per MOS-FET unless otherwise specified					
V_{DS}	drain-source voltage		–	7	V
I_D	drain current (DC)		–	40	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	$T_s \leq 102$ °C	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	240	K/W

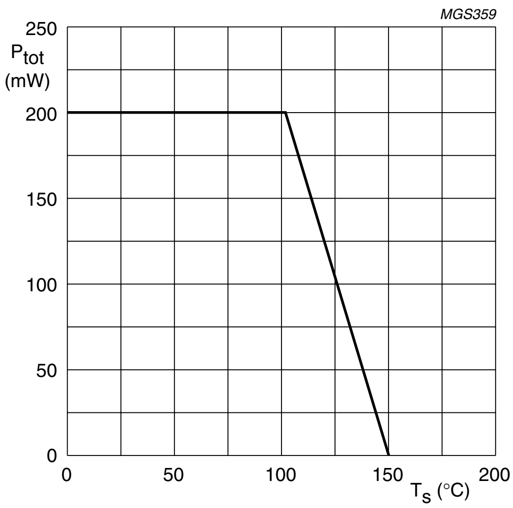


Fig.2 Power derating curve.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per MOS-FET unless otherwise specified					
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1\text{-}S} = V_{G2\text{-}S} = 0$; $I_D = 10\ \mu A$	7	–	V
$V_{(BR)G1\text{-}SS}$	gate-source breakdown voltage	$V_{GS} = V_{DS} = 0$; $I_{G1\text{-}S} = 10$ mA	6	15	V
$V_{(BR)G2\text{-}SS}$	gate-source breakdown voltage	$V_{GS} = V_{DS} = 0$; $I_{G2\text{-}S} = 5$ mA	6	15	V
$V_{(F)S\text{-}G1}$	forward source-gate voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{S\text{-}G1} = -10$ mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{S\text{-}G2} = -10$ mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate-source threshold voltage	$V_{DS} = 5$ V; $V_{G2\text{-}S} = 4$ V; $I_D = 20\ \mu A$	0.3	1	V
$V_{G2\text{-}S(th)}$	gate-source threshold voltage	$V_{DS} = 5$ V; $V_{G1\text{-}S} = 4$ V; $I_D = 20\ \mu A$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S} = 4$ V; $V_{DS} = 5$ V; $R_G = 120$ kΩ; note 1	12	20	mA
$I_{G1\text{-}S}$	gate cut-off current	$V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	–	50	nA
$I_{G2\text{-}S}$	gate cut-off current	$V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	–	20	nA

Notes

1. R_{G1} connects gate 1 to $V_{GG} = 5$ V.

DYNAMIC CHARACTERISTICS

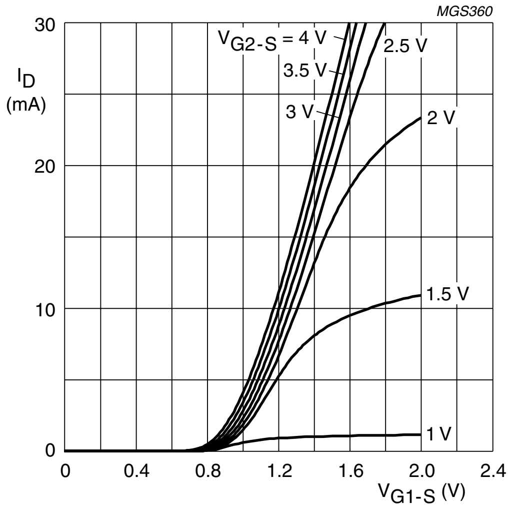
Common source; T_{amb} = 25 °C; $V_{G2\text{-}S} = 4$ V; $V_{DS} = 5$ V; $I_D = 15$ mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per MOS-FET unless otherwise specified (note 1)						
$\lvert y_{fs} \rvert$	forward transfer admittance	T_j = 25 °C	36	43	50	mS
$C_{ig1\text{-}ss}$	input capacitance at gate 1	f = 1 MHz	2	2.8	3.6	pF
$C_{ig2\text{-}ss}$	input capacitance at gate 2	f = 1 MHz	–	–	7	pF
C_{oss}	output capacitance	f = 1 MHz	–	1.6	2.5	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	30	50	fF
F	noise figure	f = 800 MHz; $Y_S = Y_{S\ opt}$	–	2	2.8	dB
X_{mod}	cross-modulation	input level for k = 1% at 0 dB AGC; f_w = 50 MHz; f_{unw} = 60 MHz; (note 2)	85	–	–	dBμV
		input level for k = 1% at 40 dB AGC; f_w = 50 MHz; f_{unw} = 60 MHz; (note 2)	100	–	–	dBμV

Notes

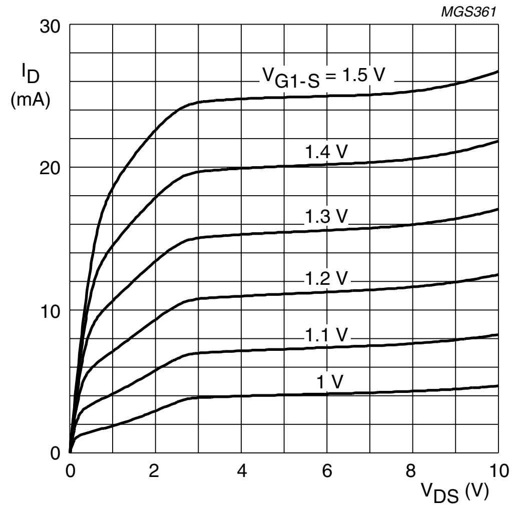
1. Not used MOS-FET: $V_{G1\text{-}S} = 0$; $V_{DS} = 0$.
2. Measured in test circuit of Fig.17.

ALL GRAPHS FOR ONE MOS-FET



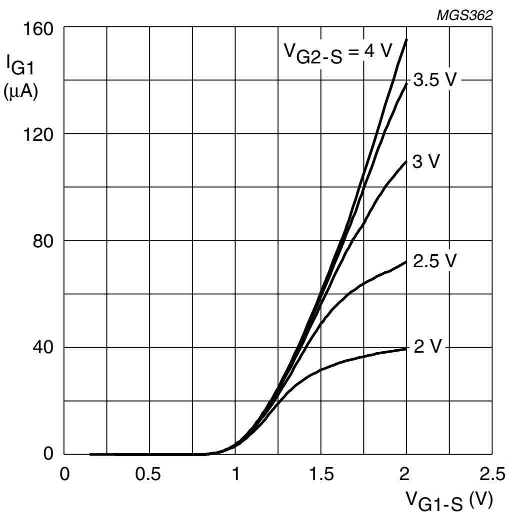
V_{DS} = 5 V.
T_j = 25 °C.

Fig.3 Transfer characteristics; typical values.



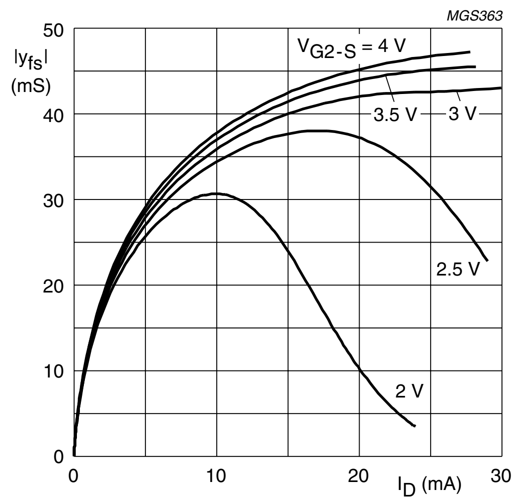
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.4 Output characteristics; typical values.



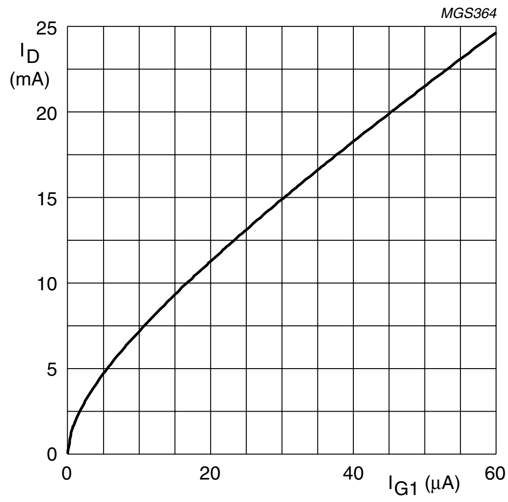
V_{DS} = 5 V.
T_j = 25 °C.

Fig.5 Gate 1 current as a function of gate 1 voltage; typical values.



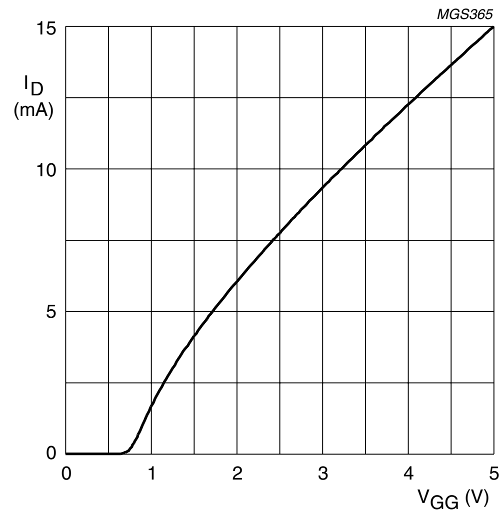
V_{DS} = 5 V.
T_j = 25 °C.

Fig.6 Forward transfer admittance as a function of drain current; typical values.



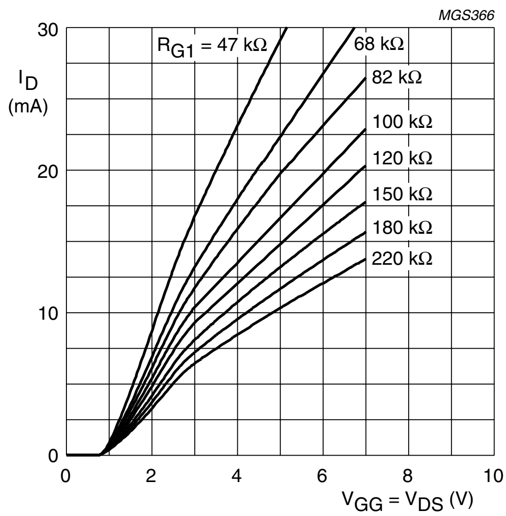
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; T_j = 25 °C.

Fig.7 Drain current as a function of gate 1 current; typical values.



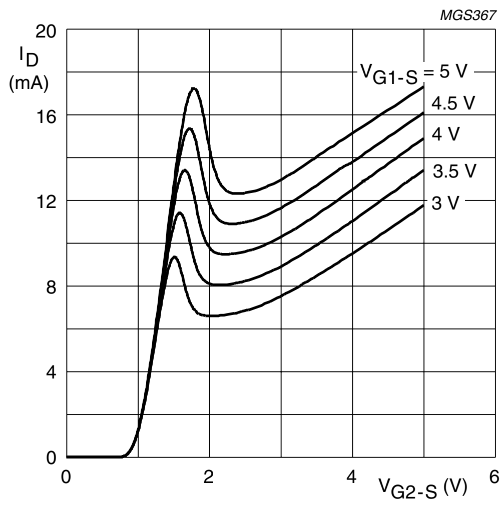
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}); see Fig.17.

Fig.8 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values.



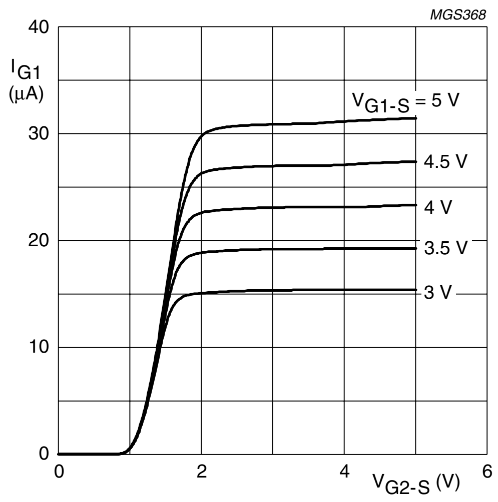
$V_{G2\text{-}S}$ = 4 V; T_j = 25 °C.
R_{G1} connected to V_{GG}; see Fig.17.

Fig.9 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values.



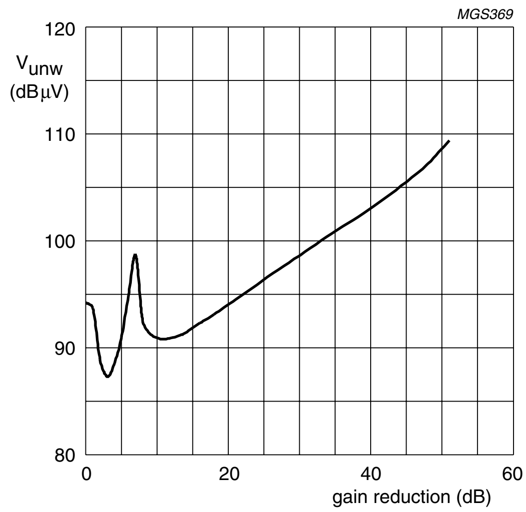
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}); see Fig.17.

Fig.10 Drain current as a function of gate 2 voltage; typical values.



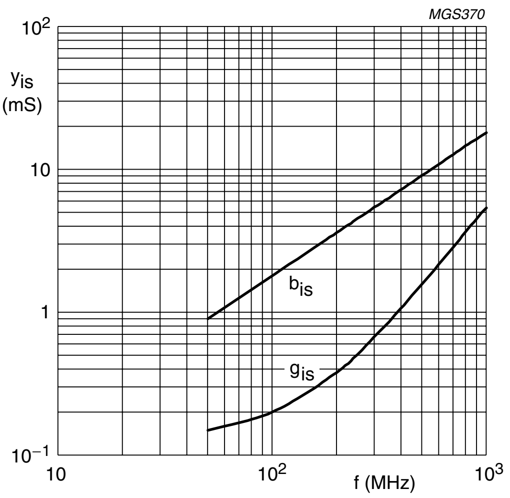
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}); see Fig.17.

Fig.11 Gate 1 current as a function of gate 2 voltage; typical values.



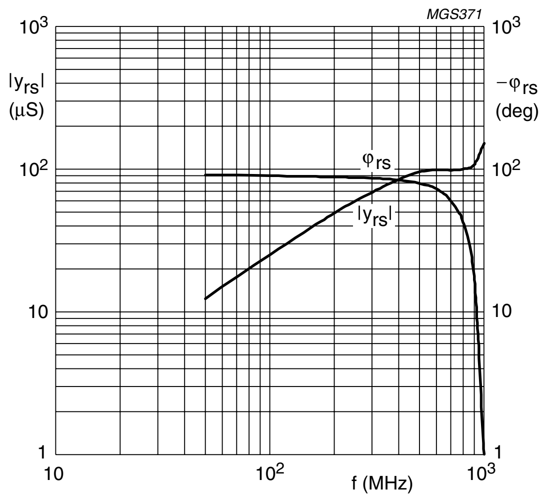
V_{DS} = 5 V; V_{GG} = 5 V; f_w = 50 MHz; f_{unw} = 60 MHz; T_{amb} = 25 °C;
R_{G1} = 120 kΩ (connected to V_{GG}); see Fig.17.

Fig.12 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values.



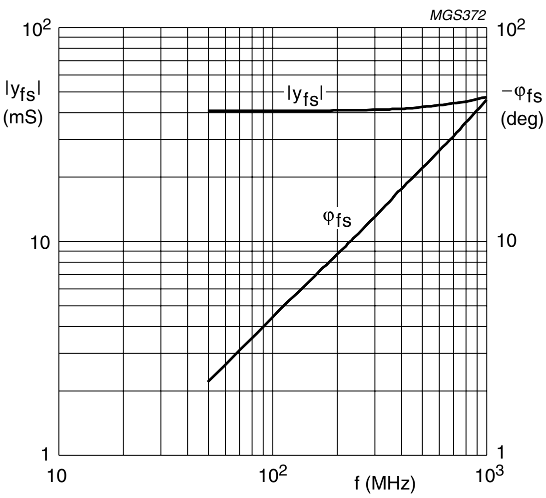
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.13 Input admittance as a function of frequency; typical values.



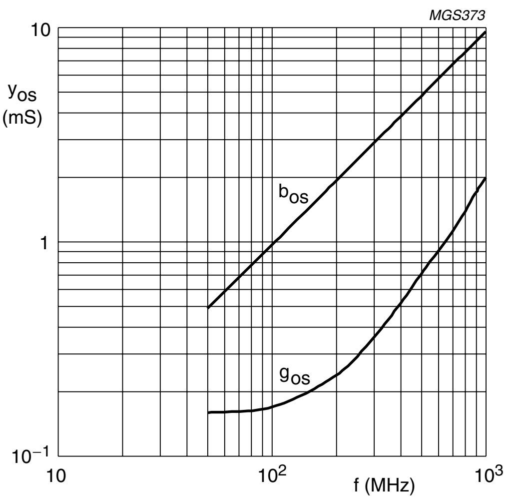
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.14 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.15 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.16 Output admittance as a function of frequency; typical values.

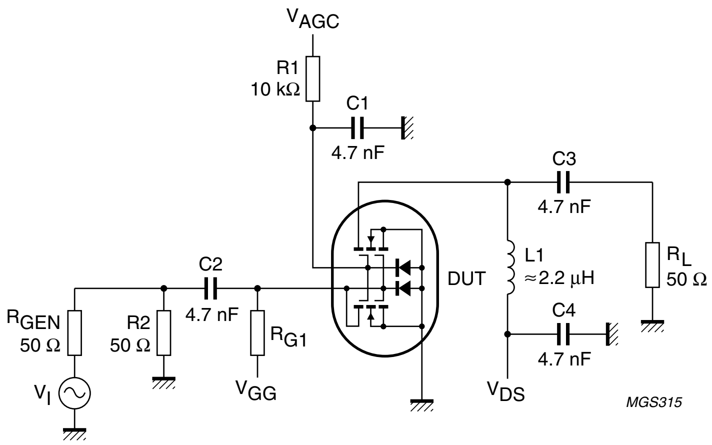
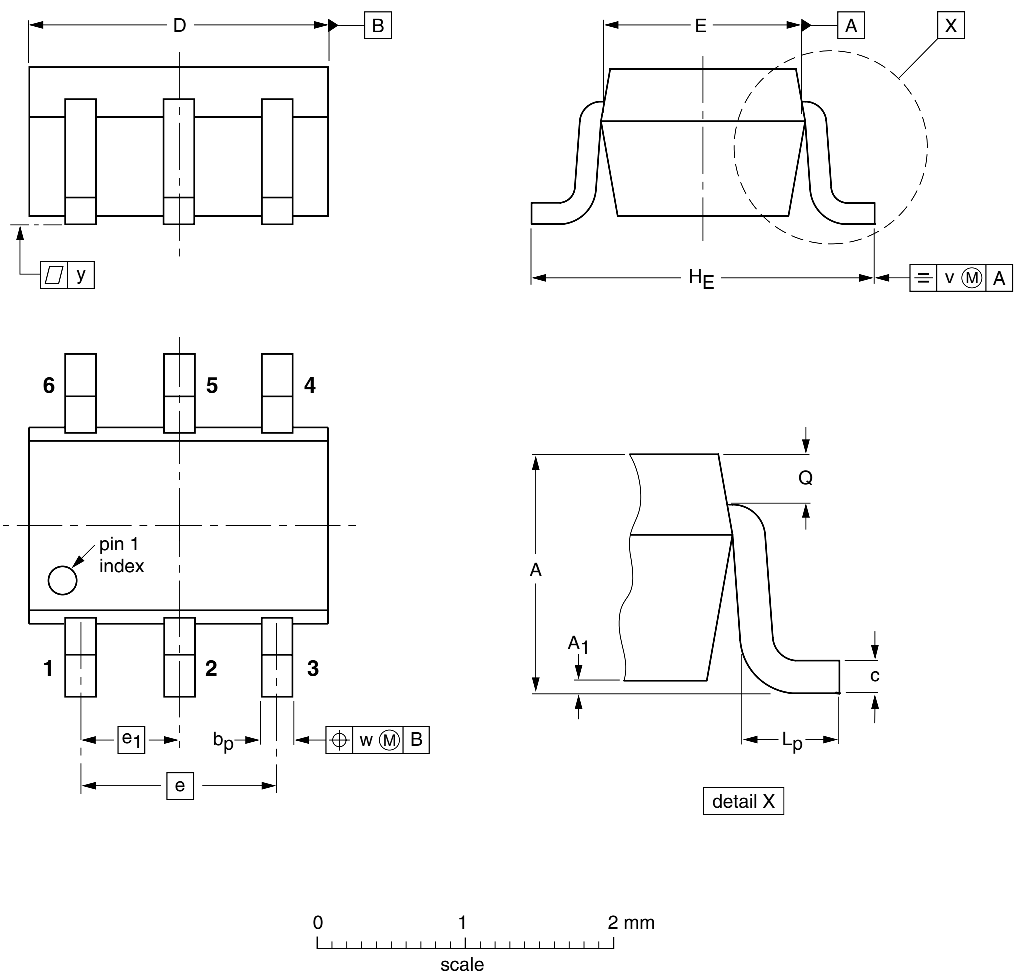


Fig.17 Cross-modulation test set-up (for one MOS-FET).

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads **SOT363**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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