

DATA SHEET

BF1105; BF1105R; BF1105WR N-channel dual-gate MOS-FETs

Product specification
Supersedes data of 1997 Dec 01
File under Discrete Semiconductors, SC07

1997 Dec 02

N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz.
- Internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

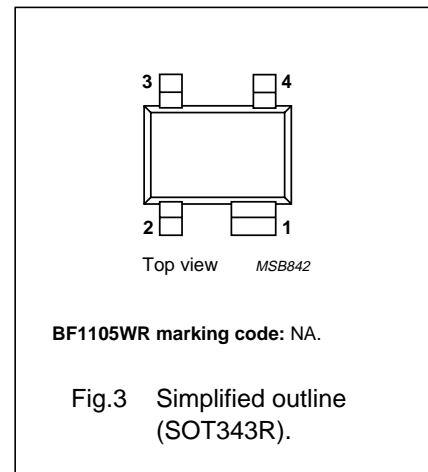
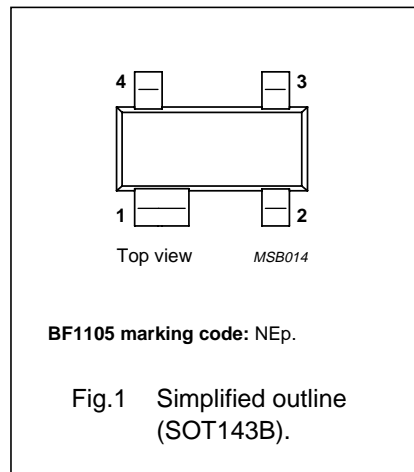
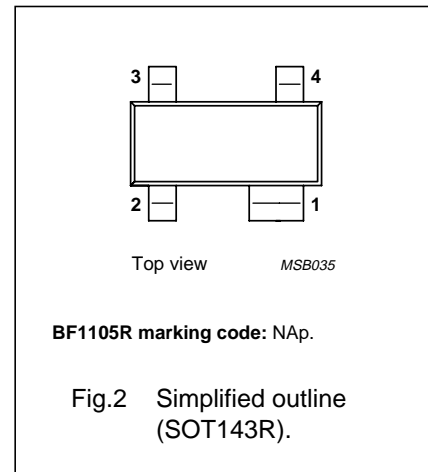
- VHF and UHF applications with 5 V supply voltage, such as television tuners and professional communications equipment.

DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1105, BF1105R and BF1105WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation	$T_{amb} \leq 80^\circ C$	–	–	200	mW
$ y_{fs} $	forward transfer admittance		25	31	–	mS
C_{ig1-ss}	input capacitance at gate 1		–	2.2	2.7	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	25	40	fF
F	noise figure	$f = 800\text{ MHz}$	–	1.7	2.5	dB
X_{mod}	cross-modulation	input level for $k = 1\%$ at 40 dB AGC	100	–	–	dB μ V
T_j	operating junction temperature		–	–	150	$^\circ C$

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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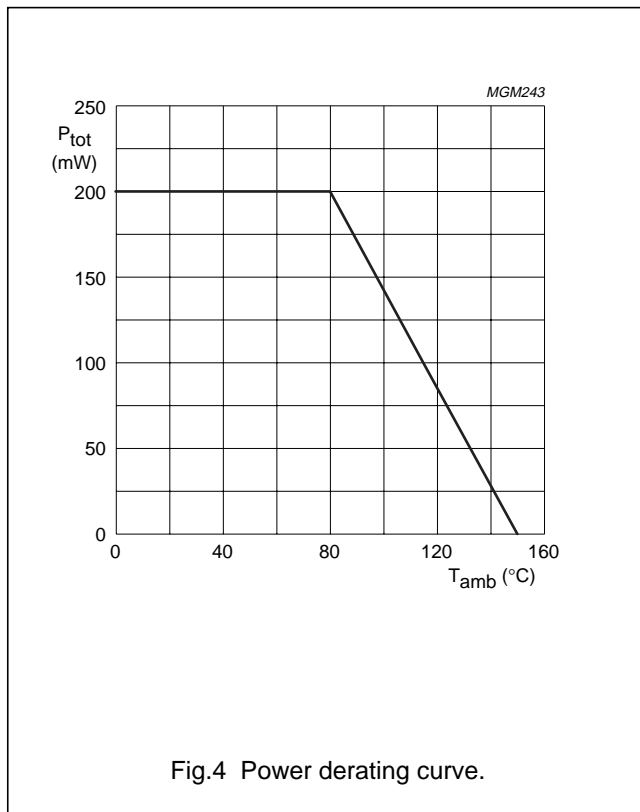
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage		–	7	V
I _D	drain current		–	30	mA
I _{G1}	gate 1 current		–	±10	mA
I _{G2}	gate 2 current		–	±10	mA
P _{tot}	total power dissipation	T _{amb} ≤ 80 °C; note 1; see Fig.4	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.



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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	note 1	350	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point		200	K/W

Note

1. Device mounted on a printed-circuit board.

STATIC CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$; $I_D = 10\ \mu\text{A}$	7	–	–	V
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = 0$; $I_D = 0$; $I_{G1-S} = 10\ \mu\text{A}$	7	–	–	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10\ \mu\text{A}$	7	–	–	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = 5\ \text{V}$; $V_{DS} = 5\ \text{V}$; $I_D = 20\ \mu\text{A}$	0.3	0.8	1.2	V
I_{DSX}	self-biasing drain current	$V_{G2-S} = 4\ \text{V}$; $V_{DS} = 5\ \text{V}$	8	–	16	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G1-S} = 5\ \text{V}$; $V_{G2-S} = 0$; $I_D = 0$	–	–	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = 4\ \text{V}$	–	–	20	nA

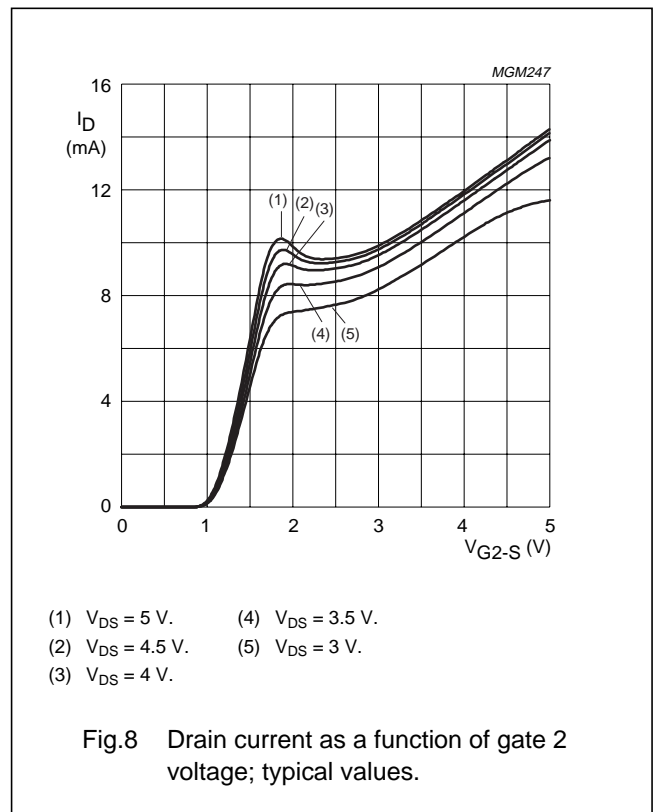
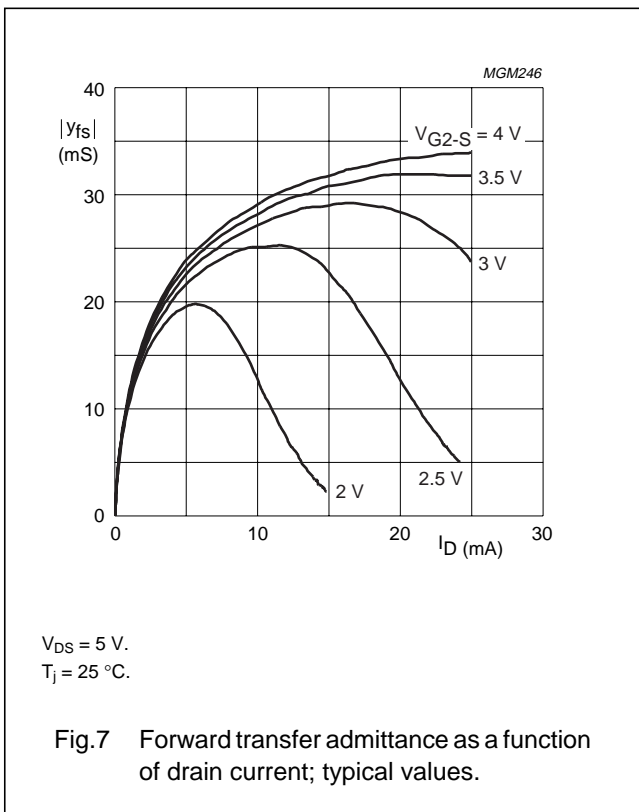
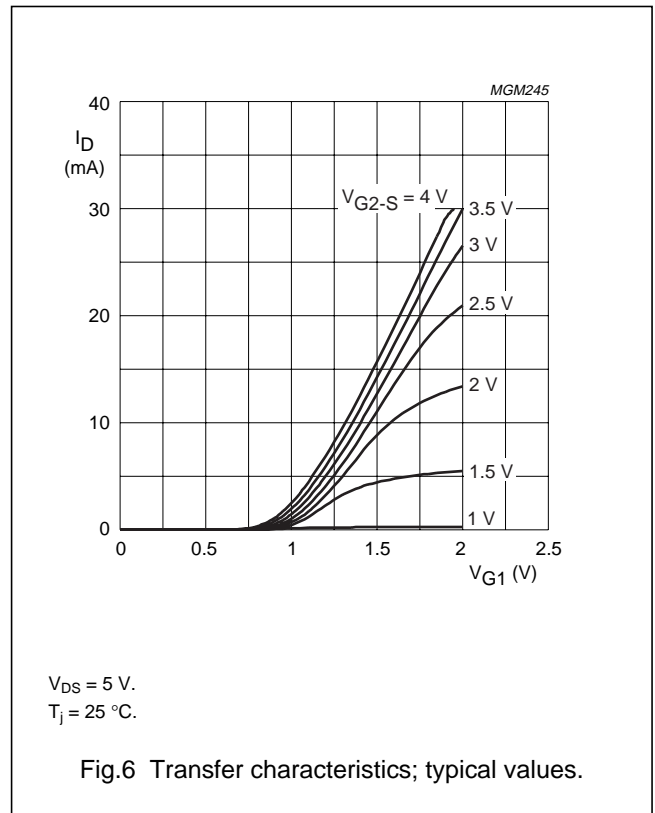
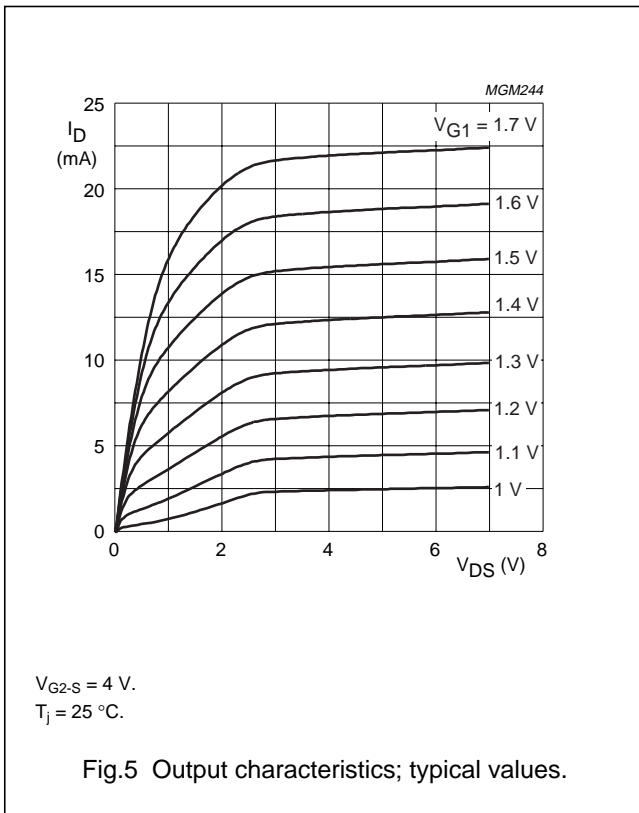
DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\text{ }^\circ\text{C}$; $V_{G2-S} = 4\ \text{V}$; $V_{DS} = 5\ \text{V}$; self-biasing current; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ }^\circ\text{C}$	25	31	–	mS
C_{ig1-ss}	input capacitance at gate 1	$f = 1\ \text{MHz}$	–	2.2	2.7	pF
C_{ig2-ss}	input capacitance at gate 2	$f = 1\ \text{MHz}$	–	1.6	–	pF
C_{oss}	output capacitance	$f = 1\ \text{MHz}$	–	1.2	–	pF
C_{rss}	reverse transfer capacitance	$f = 1\ \text{MHz}$	–	25	40	fF
F	noise figure	$f = 800\ \text{MHz}$; $Y_S = Y_{S\ opt}$	–	1.7	2.5	dB
G_p	power gain	$G_S = 2\ \text{mS}$; $B_S = B_{S\ opt}$; $G_L = 0.5\ \text{mS}$; $B_L = B_{L\ opt}$; $f = 200\ \text{MHz}$; see Fig.16	–	38	–	dB
		$G_S = 3.3\ \text{mS}$; $B_S = B_{S\ opt}$; $G_L = 1\ \text{mS}$; $B_L = B_{L\ opt}$; $f = 800\ \text{MHz}$; see Fig.17	–	20	–	dB
X_{mod}	cross-modulation	input level for $k = 1\%$ at 0 dB AGC; $f_w = 50\ \text{MHz}$; $f_{unw} = 60\ \text{MHz}$; see Fig.18	85	–	–	dB μV
		input level for $k = 1\%$ at 40 dB AGC; $f_w = 50\ \text{MHz}$; $f_{unw} = 60\ \text{MHz}$; see Fig.18	100	–	–	dB μV

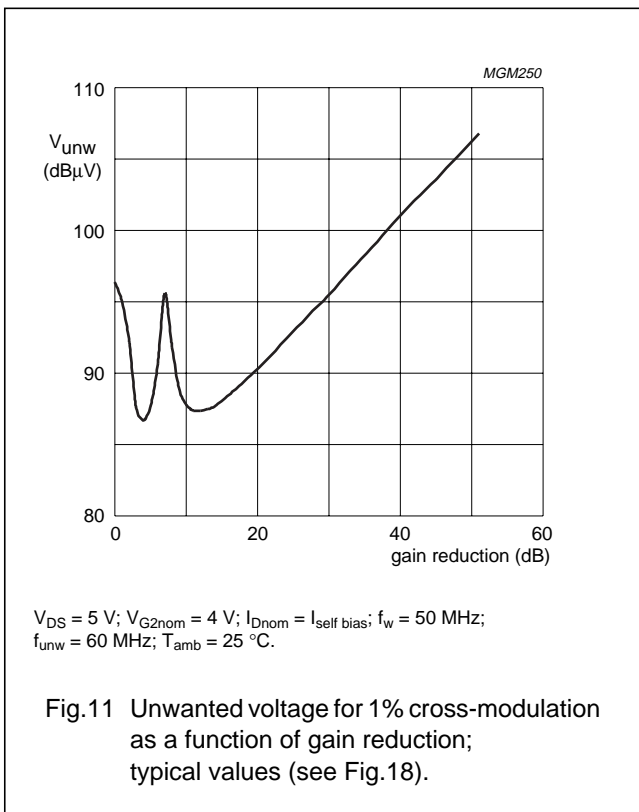
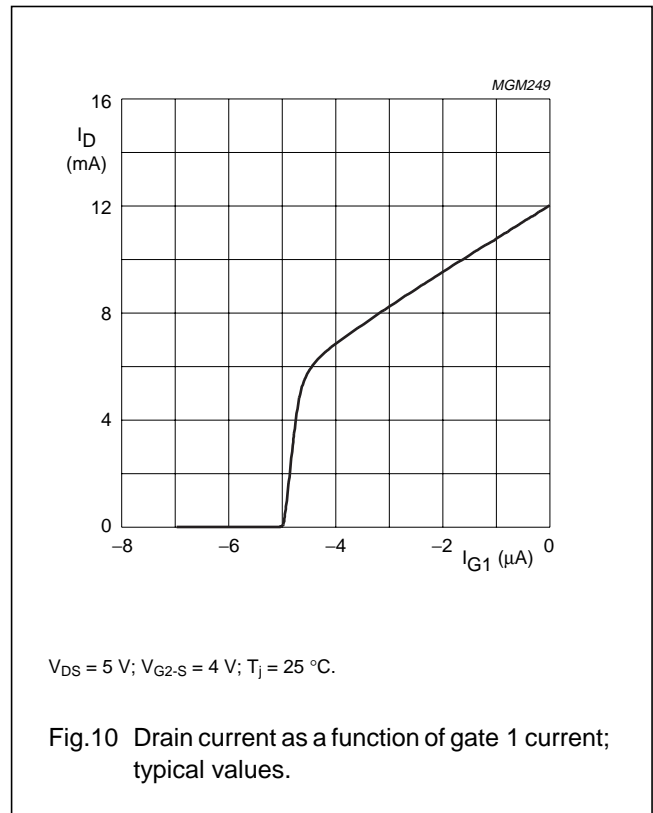
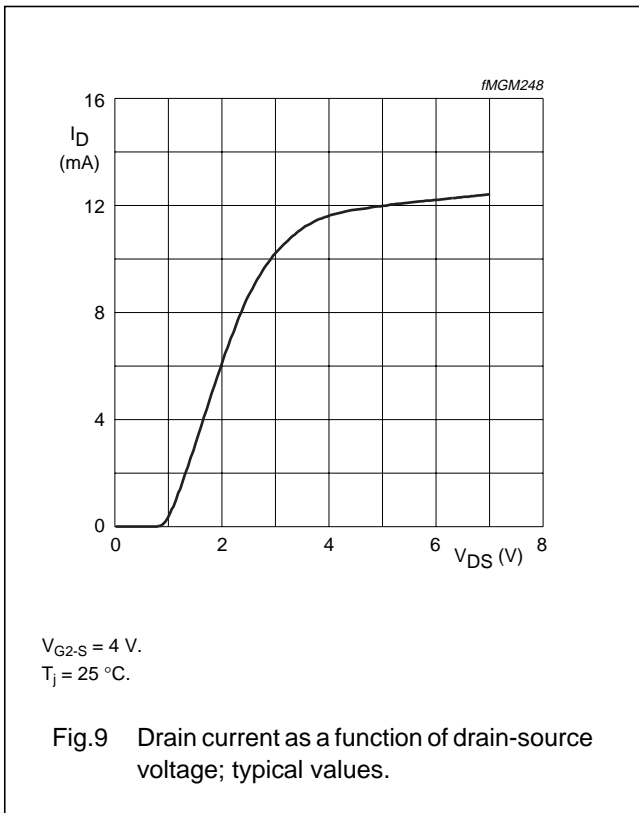
N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR



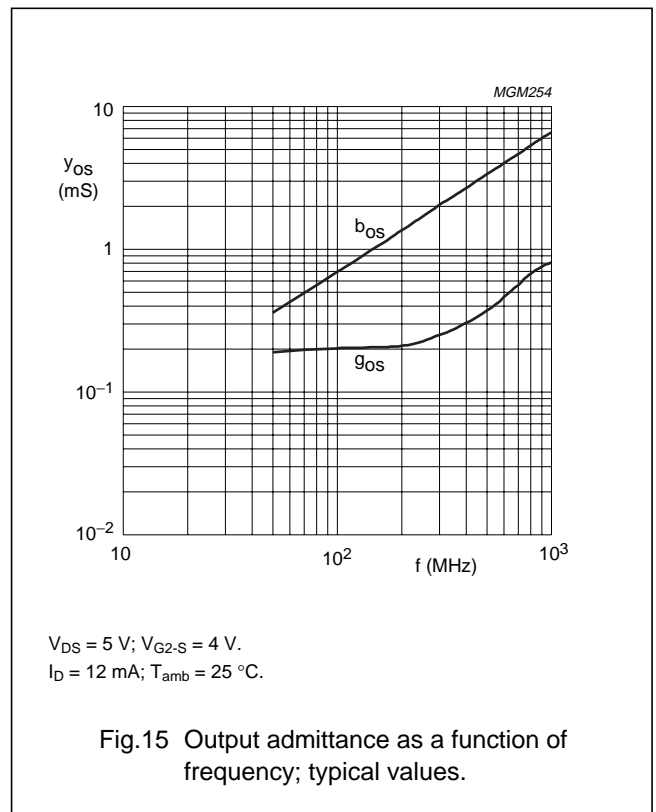
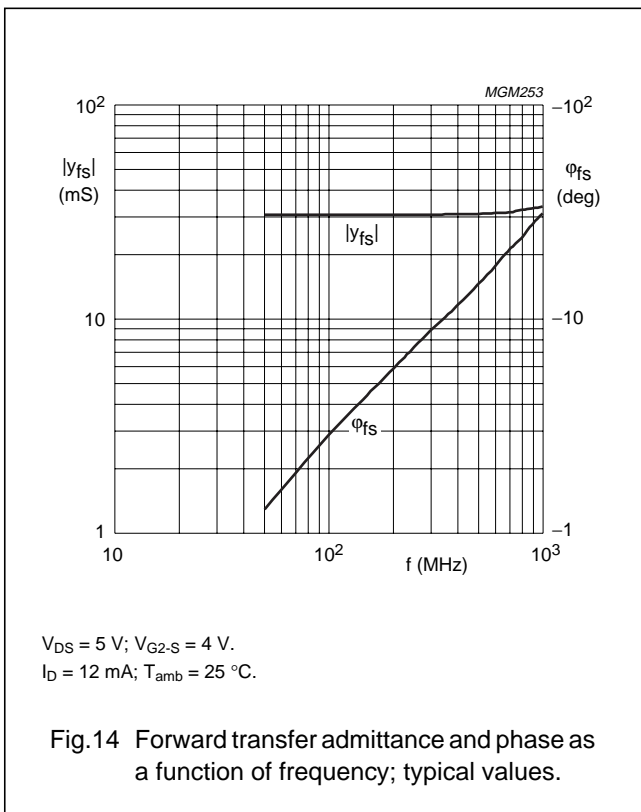
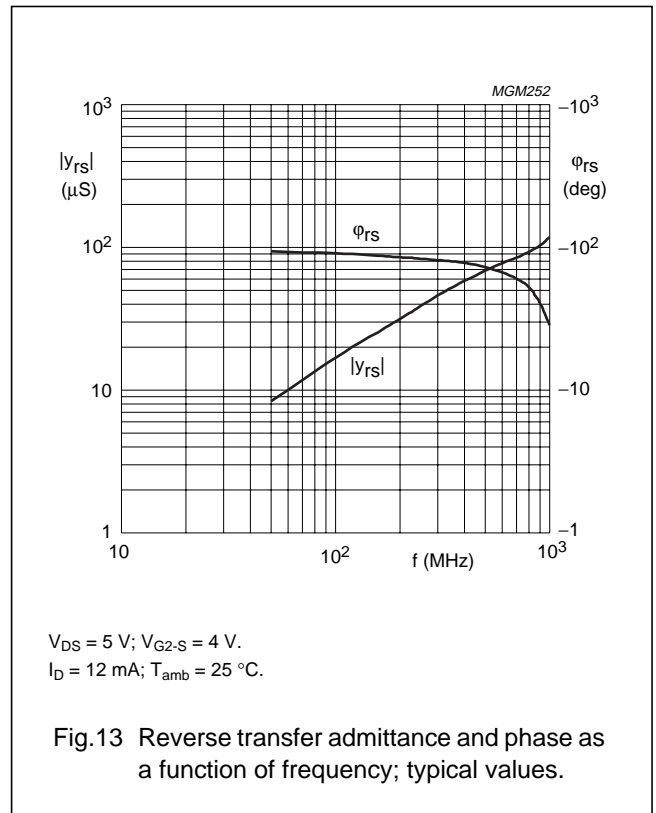
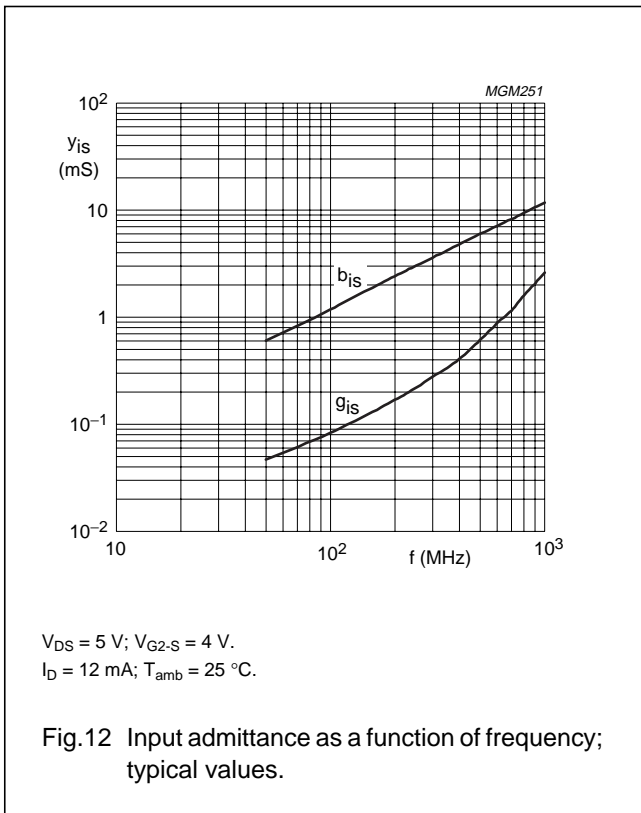
N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR



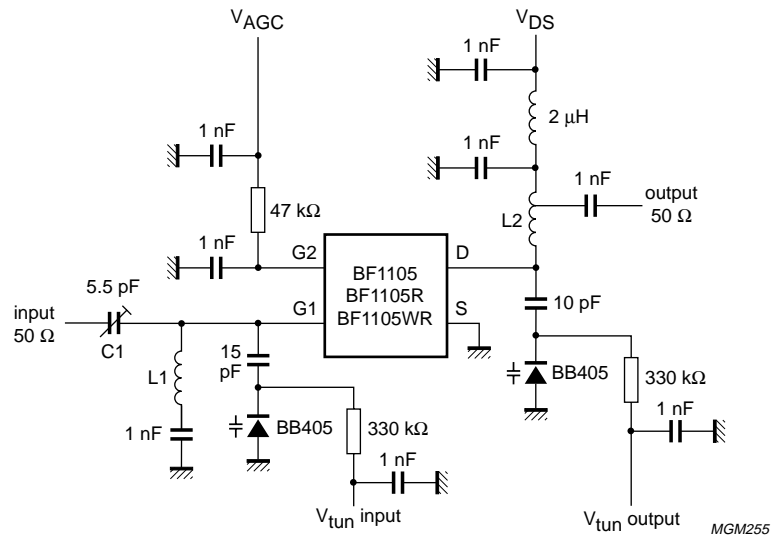
N-channel dual-gate MOS-FETs

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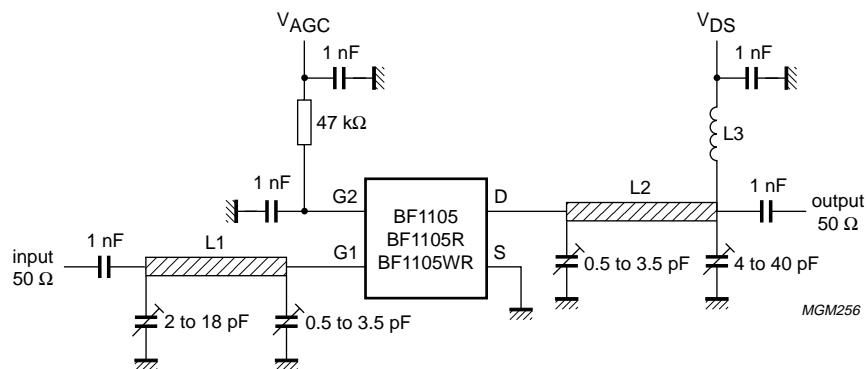
N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR



$V_{DS} = 5\text{ V}$, $G_S = 2\text{ mS}$, $G_L = 0.5\text{ mS}$, $f = 200\text{ MHz}$.
 $L1 = 45\text{ nH}$, 4 turns, internal diameter = 4 mm, 0.8 mm copper wire.
 $L2 = 160\text{ nH}$, 3 turns, internal diameter = 8 mm, 0.8 mm copper wire; tapped at approximately half a turn from the cold side, to set $G_L = 0.5\text{ mS}$.
 $C1$ adjusted for $G_S = 2\text{ mS}$.

Fig.16 Gain test circuit.



$V_{DS} = 5\text{ V}$, $G_S = 3.3\text{ mS}$, $G_L = 1\text{ mS}$, $f = 800\text{ MHz}$.
 $L1 = 2\text{ cm}$, silvered 0.8 mm copper wire 4 mm above ground plane.
 $L2 = 2\text{ cm}$, silvered 0.8 mm copper wire 4 mm above ground plane.
 $L3 = 11\text{ turns}$ 0.5 mm copper wire without spacing, internal diameter = 3 mm, $L = \text{approx. } 200\text{ nH}$.

Fig.17 Gain test circuit.

N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR

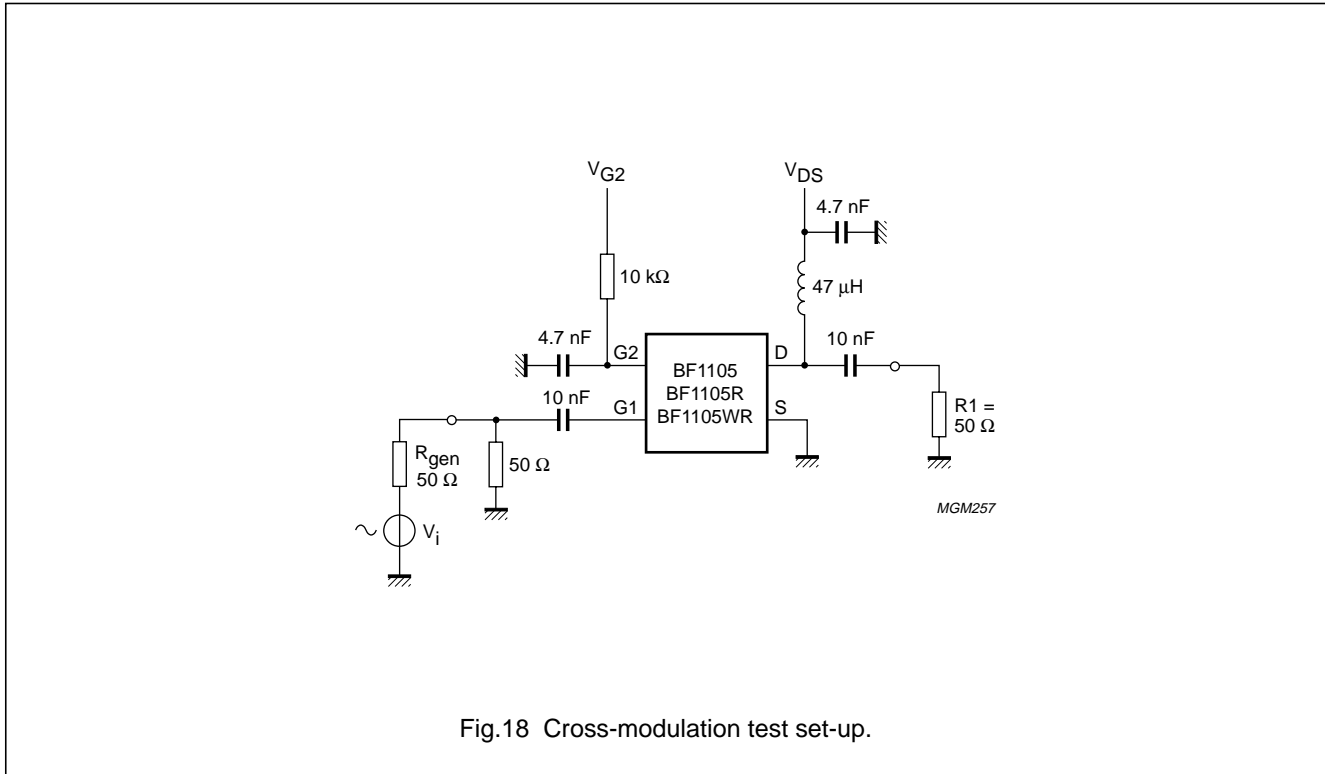


Fig.18 Cross-modulation test set-up.

Table 1 Scattering parameters: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 12\text{ mA}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.994	-3.8	3.060	175.4	0.000	86.9	0.985	-2.1
100	0.991	-7.5	3.047	170.9	0.002	86.1	0.983	-4.2
200	0.982	-14.7	3.004	162.1	0.003	82.7	0.980	-8.3
300	0.968	-21.7	2.932	153.4	0.004	79.7	0.976	-12.1
400	0.956	-28.8	2.896	145.3	0.006	77.8	0.972	-16.2
500	0.937	-35.4	2.815	137.1	0.007	76.7	0.967	-20.0
600	0.918	-41.8	2.735	129.2	0.007	76.3	0.961	-23.7
700	0.897	-48.1	2.651	121.5	0.008	76.7	0.955	-27.3
800	0.878	-54.0	2.575	114.0	0.008	79.7	0.948	-30.9
900	0.858	-59.9	2.482	106.5	0.008	82.2	0.941	-34.4
1000	0.840	-65.5	2.396	99.5	0.008	88.0	0.935	-37.9

Table 2 Noise data: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 12\text{ mA}$

f (MHz)	F _{min} (dB)	Γ _{opt}		R _n (Ω)
		(ratio)	(deg)	
800	1.5	0.674	39.7	37.15

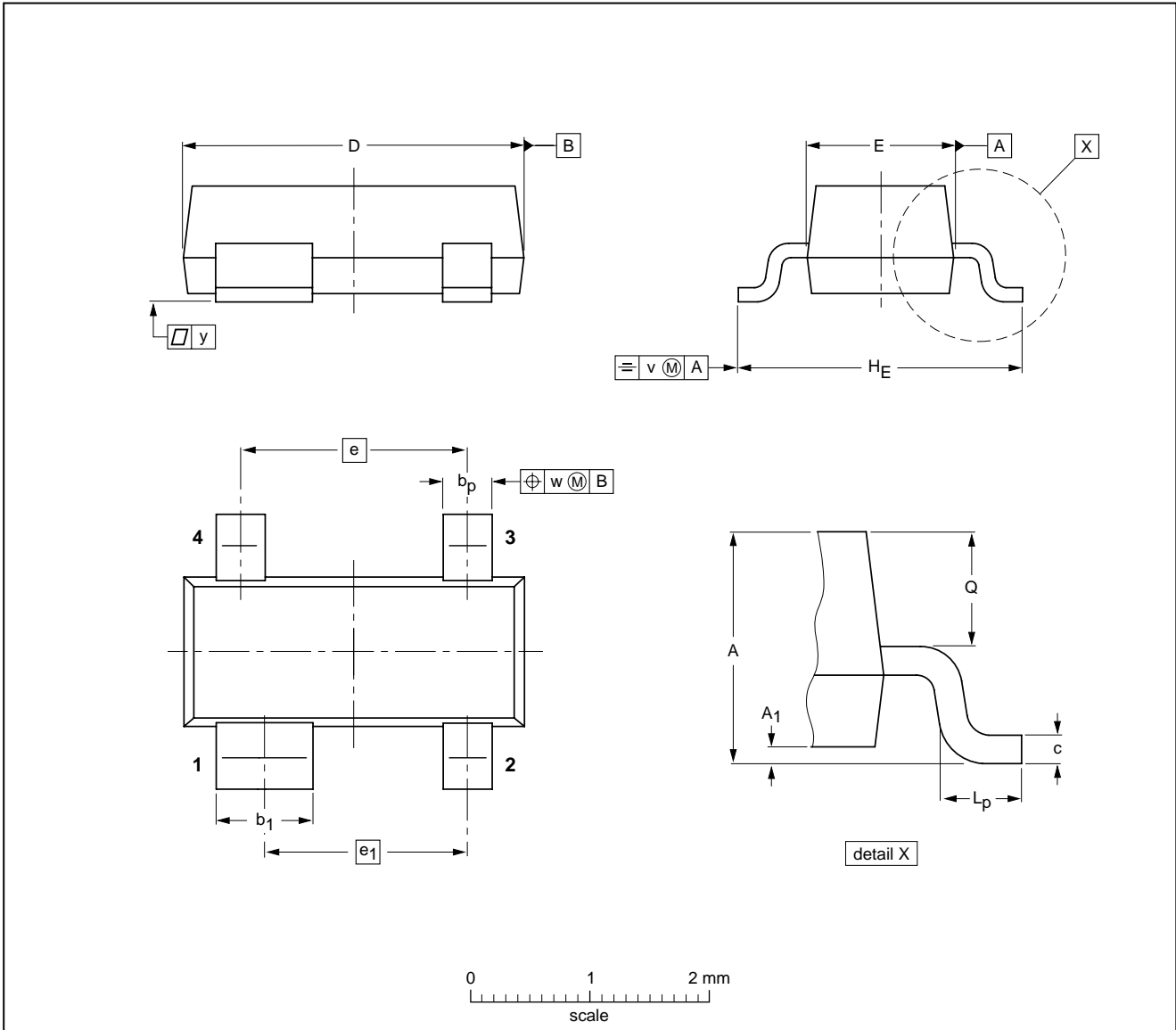
N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR

PACKAGE OUTLINES

Plastic surface mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

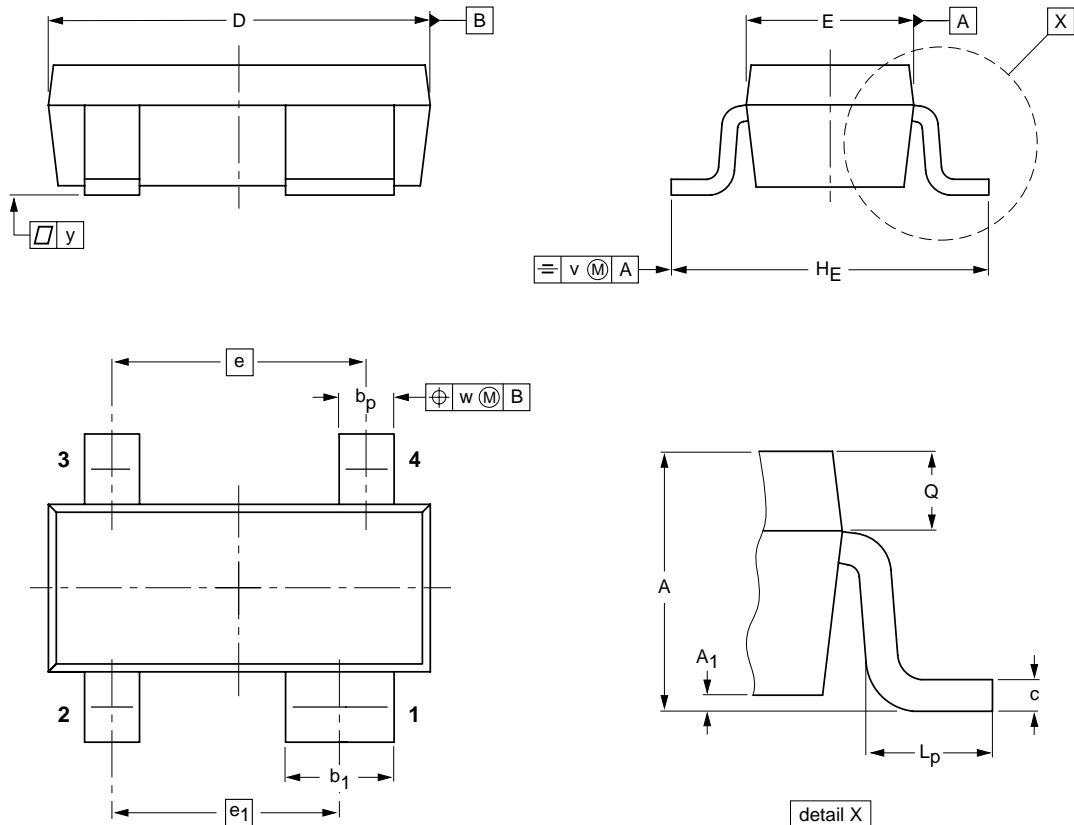
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	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR

Plastic surface mounted package; reverse pinning; 4 leads

SOT143R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

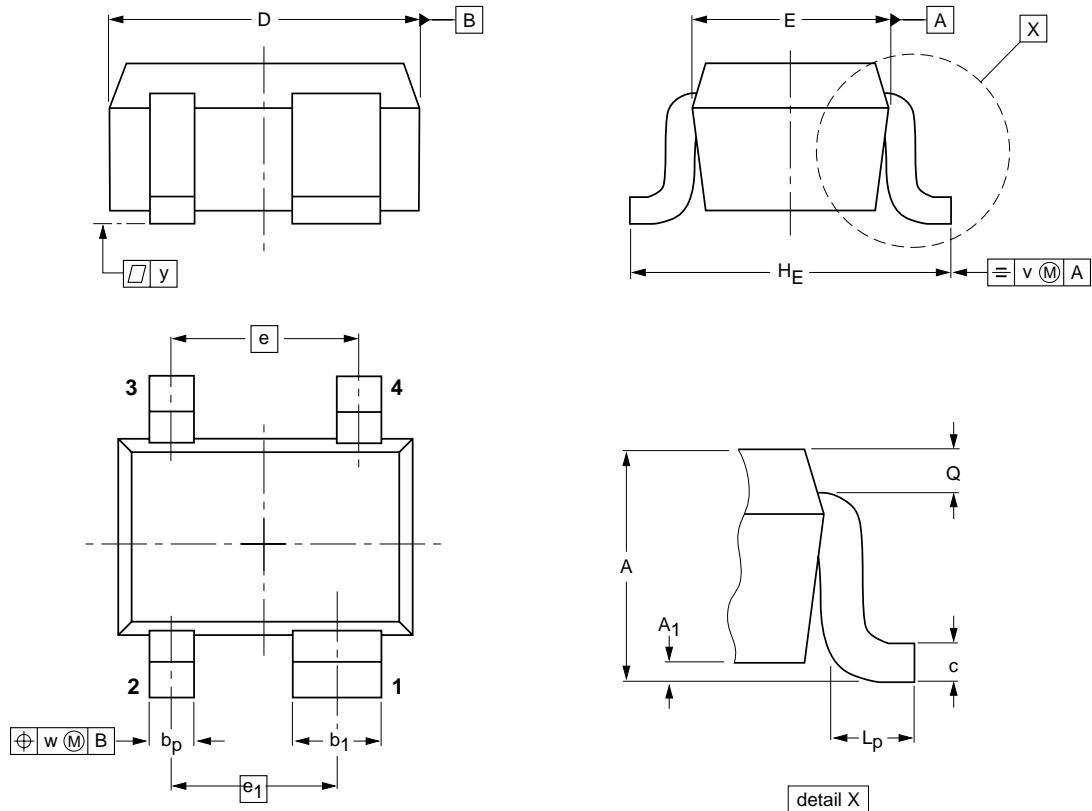
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SOT143R						97-03-10

N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR

Plastic surface mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21

N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR

NOTES

N-channel dual-gate MOS-FETs

BF1105; BF1105R; BF1105WR

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p,
P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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西安分公司：西安高新开发区 20 所(中国电子科技集团导航技术研究所)

西安劳动南路 88 号电子商城二楼 D23 号

TEL: 029-81022619 13072977981 FAX:029-88789382