

DATA SHEET

BF1201; BF1201R; BF1201WR
N-channel dual-gate PoLo
MOS-FETs

Preliminary specification

1999 Nov 26

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier
- Partly internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

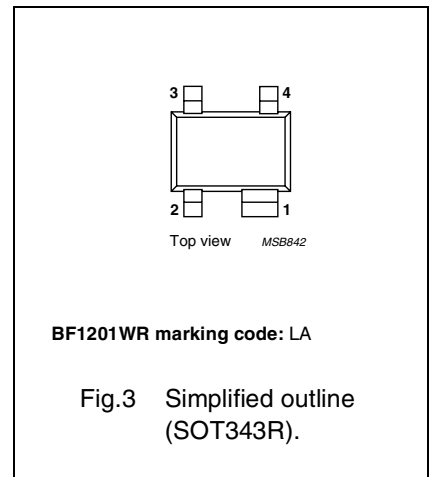
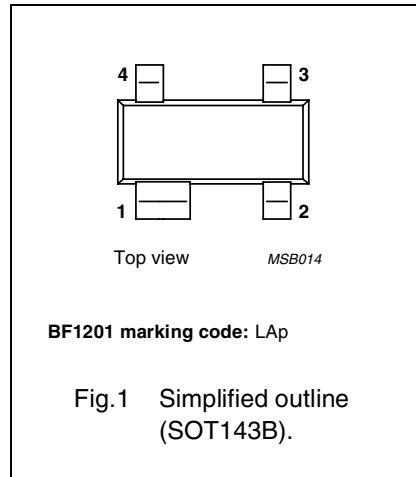
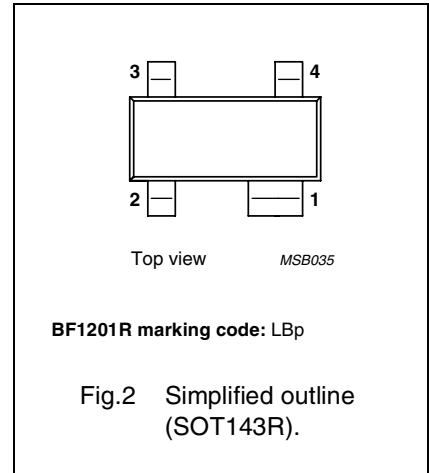
- VHF and UHF applications with 3 - 9 V supply voltage, such as digital and analogue television tuners and professional communications equipment.

DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1201, BF1201R and BF1201WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	10	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	200	mW
$ y_{fs} $	forward transfer admittance		23	28	35	mS
C_{ig1-ss}	input capacitance at gate 1		–	2.6	3.1	pF
C_{rss}	reverse transfer capacitance	$f = 1 \text{ MHz}$	–	15	30	fF
F	noise figure	$f = 400 \text{ MHz}$	–	1	1.8	dB
X_{mod}	cross-modulation	input level for $k = 1\%$ at 40 dB AGC	105	–	–	dB μ V
T_j	operating junction temperature		–	–	150	°C

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

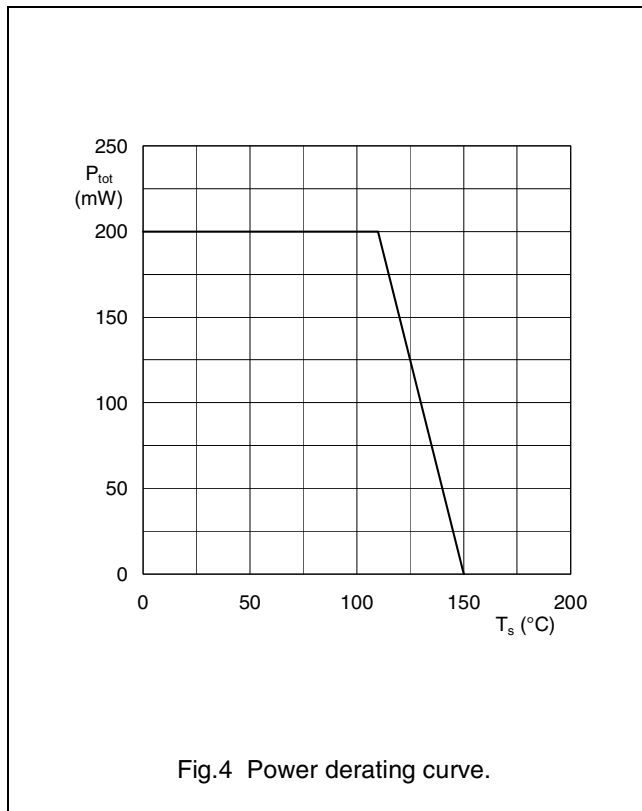
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage		–	10	V
I _D	drain current		–	30	mA
I _{G1}	gate 1 current		–	±10	mA
I _{G2}	gate 2 current		–	±10	mA
P _{tot}	total power dissipation	T _s ≤ 110 °C; note 1		200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	+150	°C

Note

1. T_s is the temperature of the soldering point of the source lead.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-s}	thermal resistance from junction to soldering point		200	K/W



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STATIC CHARACTERISTICS

 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$; $I_D = 10\text{ }\mu\text{A}$	10	–	V
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; $I_{G1-S} = 10\text{ mA}$	6	–	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10\text{ mA}$	6	–	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10\text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10\text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 100\text{ }\mu\text{A}$	0.3	1.0	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = 5\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 100\text{ }\mu\text{A}$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $R_{G1} = 62\text{ k}\Omega$; note 1	11	19	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$; $V_{G1-S} = 5\text{ V}$	–	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = 4\text{ V}$	–	20	nA

Note

- R_{G1} connects G_1 to $V_{GG} = 5\text{ V}$

DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\text{ }^\circ\text{C}$; $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 15\text{ mA}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ }^\circ\text{C}$	23	28	35	mS
C_{ig1-ss}	input capacitance at gate 1	$f = 1\text{ MHz}$	–	2.6	3.1	pF
C_{ig2-ss}	input capacitance at gate 2	$f = 1\text{ MHz}$	–	1.1	–	pF
C_{oss}	output capacitance	$f = 1\text{ MHz}$	–	0.9	–	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	15	30	fF
NF	noise figure	$f = 400\text{ MHz}$; $Y_S = Y_{S\text{ opt}}$	–	1	1.8	dB
		$f = 800\text{ MHz}$; $Y_S = Y_{S\text{ opt}}$	–	1.8	2.5	dB
X_{mod}	cross-modulation	input level for $k = 1\%$ at 0 dB AGC; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; note 1	90	–	–	dB μ V
		input level for $k = 1\%$ at 10 dB AGC; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; note 1	–	95	–	dB μ V
		input level for $k = 1\%$ at 40 dB AGC; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; note 1	105	–	–	dB μ V

Note

- Measured in test circuit of Fig.5.

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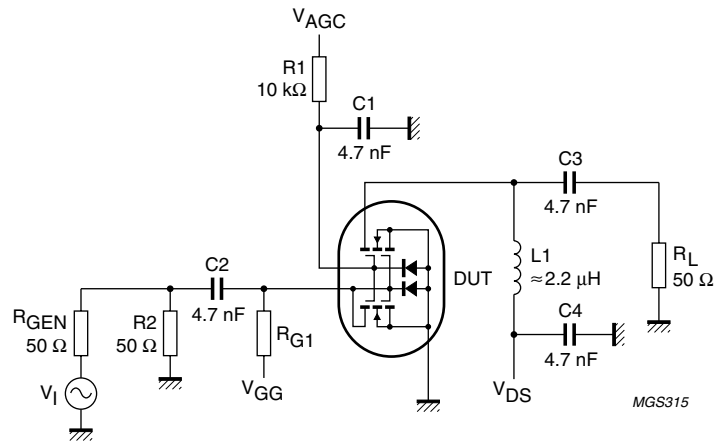


Fig.5 Cross-modulation test set-up.

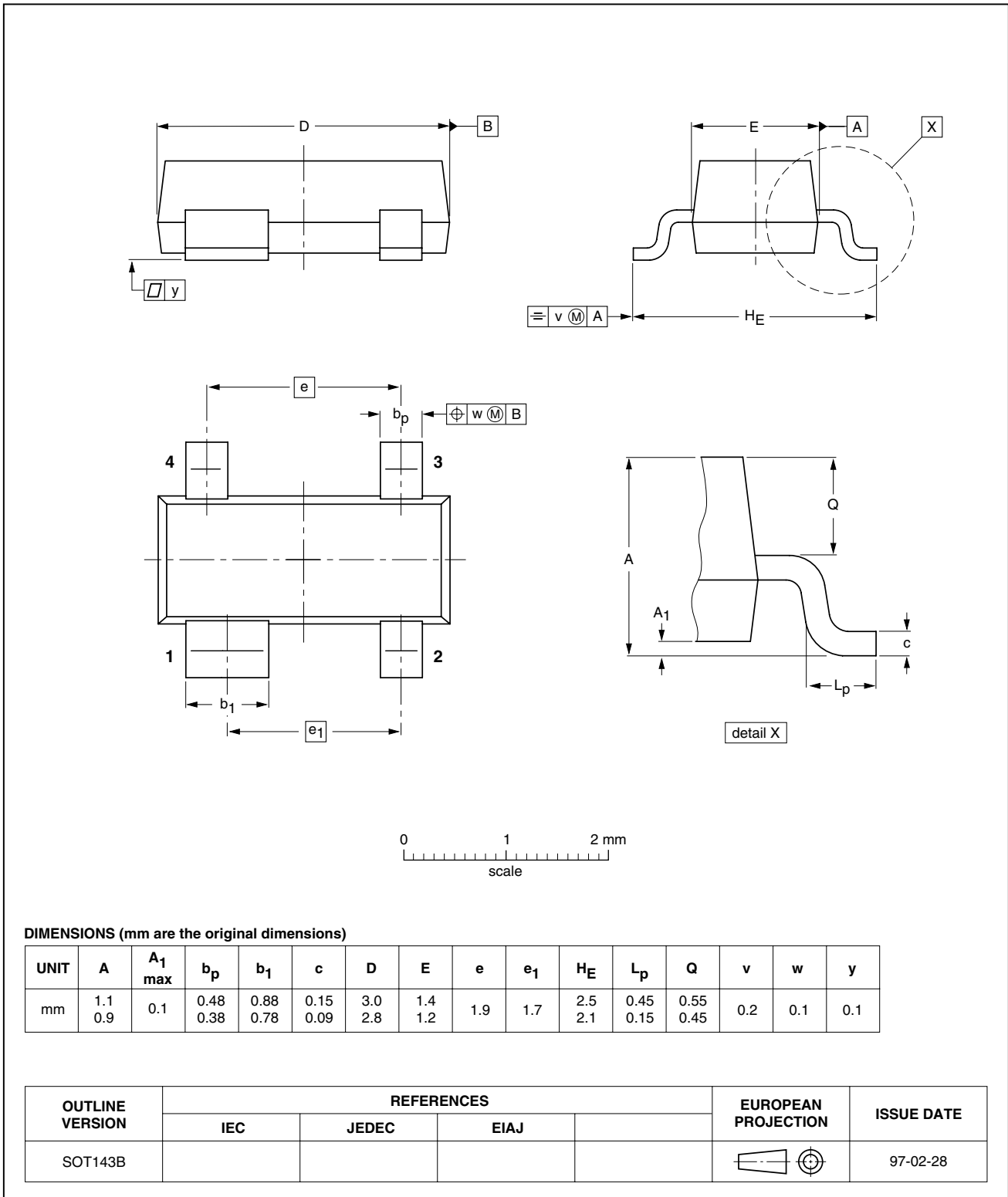
N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R;
BF1201WR

PACKAGE OUTLINES

Plastic surface mounted package; 4 leads

SOT143B

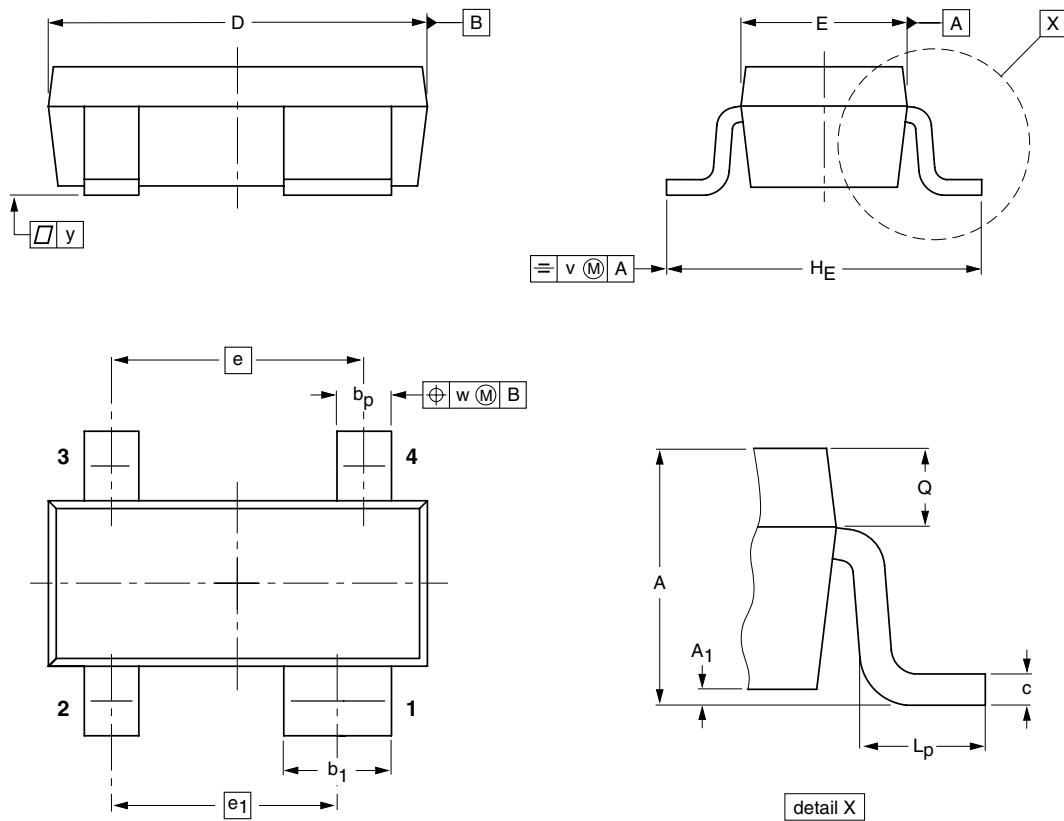


N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R;
BF1201WR

Plastic surface mounted package; reverse pinning; 4 leads

SOT143R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

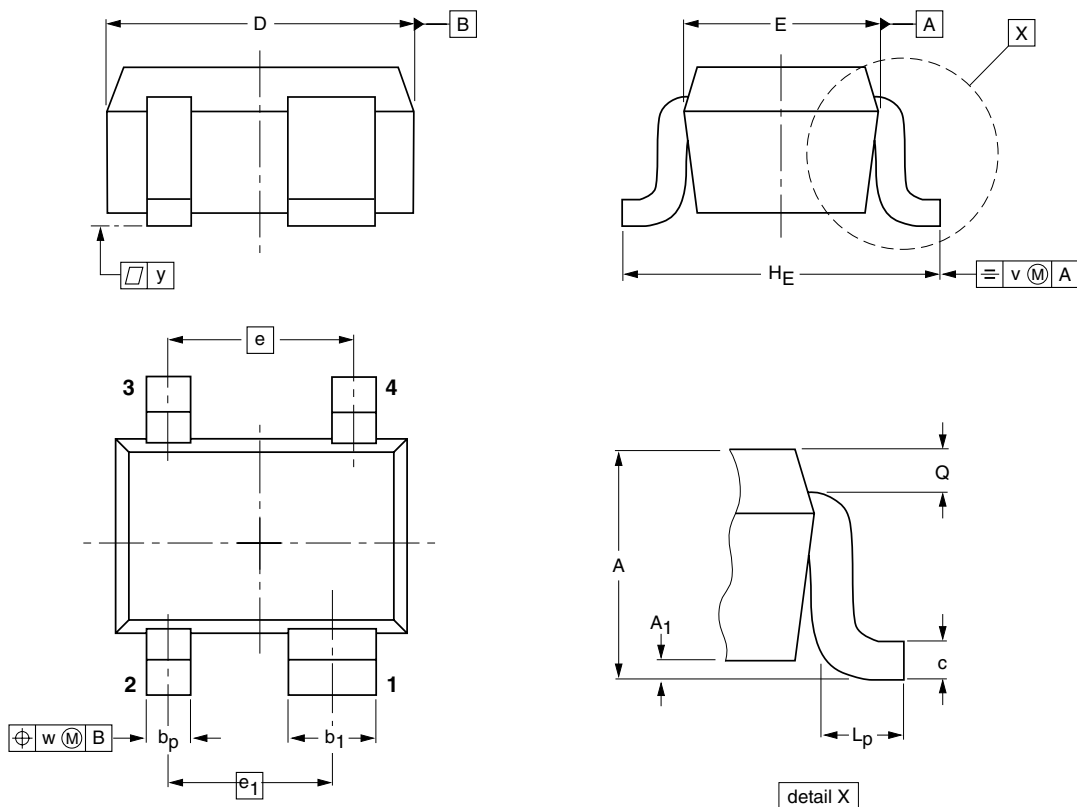
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143R			SC-61B			97-03-10 99-09-13

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R;
BF1201WR

Plastic surface mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R;
BF1201WR**DEFINITIONS**

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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