

# DATA SHEET

## **BF904A; BF904AR; BF904AWR** N-channel dual gate MOS-FETs

Product specification  
Supersedes data of 1999 Feb 01

1999 May 14

# N-channel dual gate MOS-FETs

# BF904A; BF904AR; BF904AWR

### FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

### APPLICATIONS

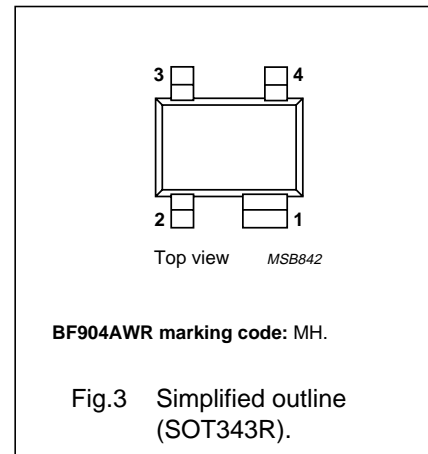
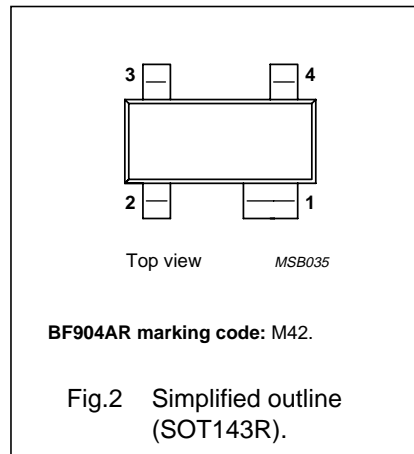
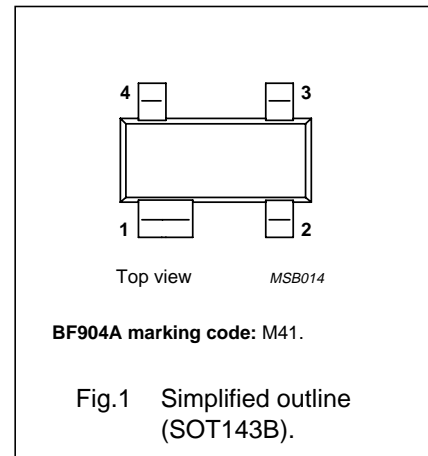
- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

### DESCRIPTION

Enhancement type field-effect transistors. The transistors consist of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC. The BF904A, BF904AR and BF904AWR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

### PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	–	7	V
$I_D$	drain current		–	–	30	mA
$P_{tot}$	total power dissipation	$T_s \leq 110\text{ }^\circ\text{C}$	–	–	200	mW
$ y_{fs} $	forward transfer admittance		22	25	30	mS
$C_{ig1-ss}$	input capacitance at gate 1		–	2.2	2.6	pF
$C_{rss}$	reverse transfer capacitance	$f = 1\text{ MHz}$	–	25	35	fF
F	noise figure	$f = 800\text{ MHz}$	–	2	–	dB
$T_j$	operating junction temperature		–	–	150	$^\circ\text{C}$

### CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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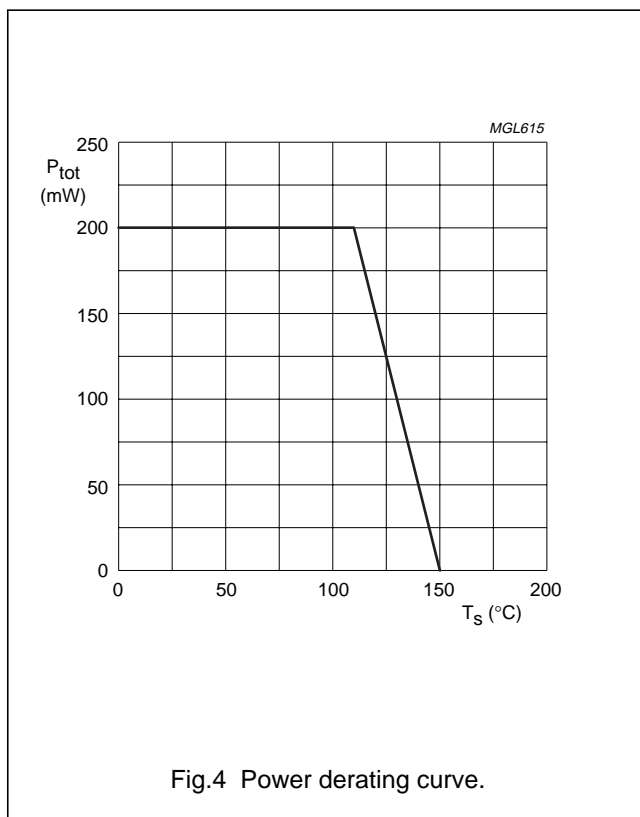
**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>DS</sub>	drain-source voltage		–	7	V
I <sub>D</sub>	drain current		–	30	mA
I <sub>G1</sub>	gate 1 current		–	±10	mA
I <sub>G2</sub>	gate 2 current		–	±10	mA
P <sub>tot</sub>	total power dissipation	T <sub>s</sub> ≤ 110 °C; note 1; see Fig.4	–	200	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	operating junction temperature		–	150	°C

**Note**

1. T<sub>s</sub> is the temperature of the soldering point of the source lead.



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## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	note 1	200	K/W

## Note

- Soldering point of the source lead.

## STATIC CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$ ; $I_{G1-S} = 10\text{ mA}$	6	15	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$ ; $I_{G2-S} = 10\text{ mA}$	6	15	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$ ; $I_{S-G1} = 10\text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$ ; $I_{S-G2} = 10\text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4\text{ V}$ ; $V_{DS} = 5\text{ V}$ ; $I_D = 20\text{ }\mu\text{A}$	0.3	1	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = V_{DS} = 5\text{ V}$ ; $I_D = 20\text{ }\mu\text{A}$	0.3	1.2	V
$I_{DSX}$	drain-source current	$V_{G2-S} = 4\text{ V}$ ; $V_{DS} = 5\text{ V}$ ; $R_{G1} = 120\text{ k}\Omega$ ; note 1	8	13	mA
$I_{G1-SS}$	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$ ; $V_{G1-S} = 5\text{ V}$	–	50	nA
$I_{G2-SS}$	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$ ; $V_{G2-S} = 5\text{ V}$	–	50	nA

## Note

- $R_{G1}$  connects gate 1 to  $V_{GG} = 5\text{ V}$ ; see Fig.21.

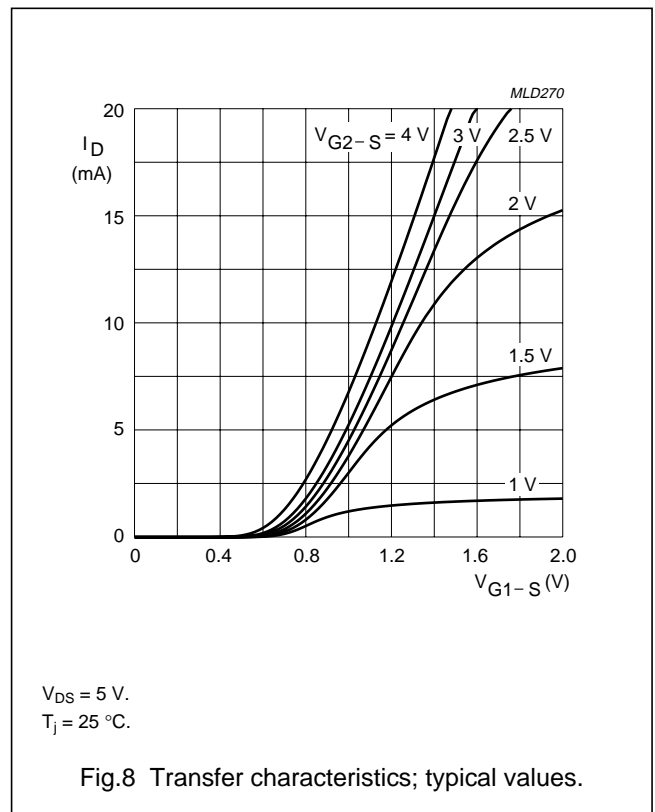
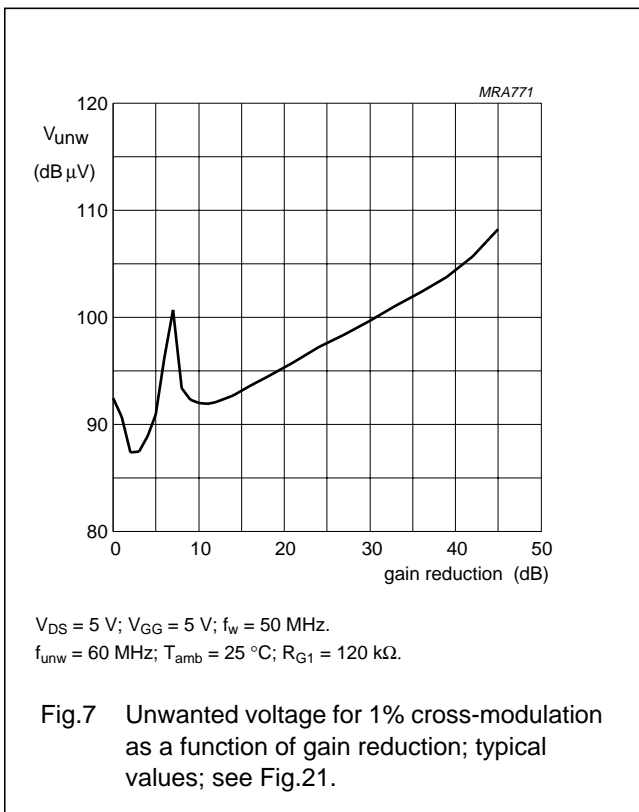
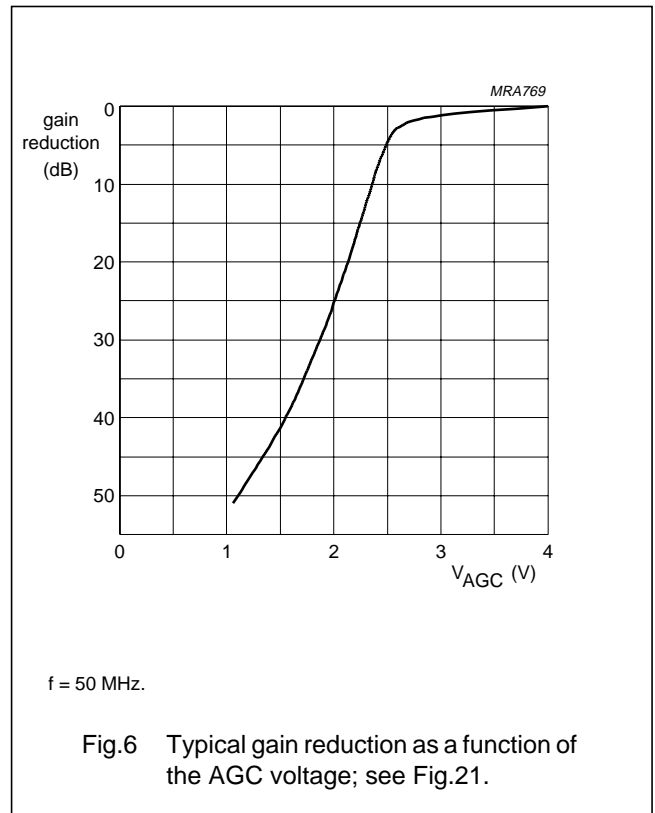
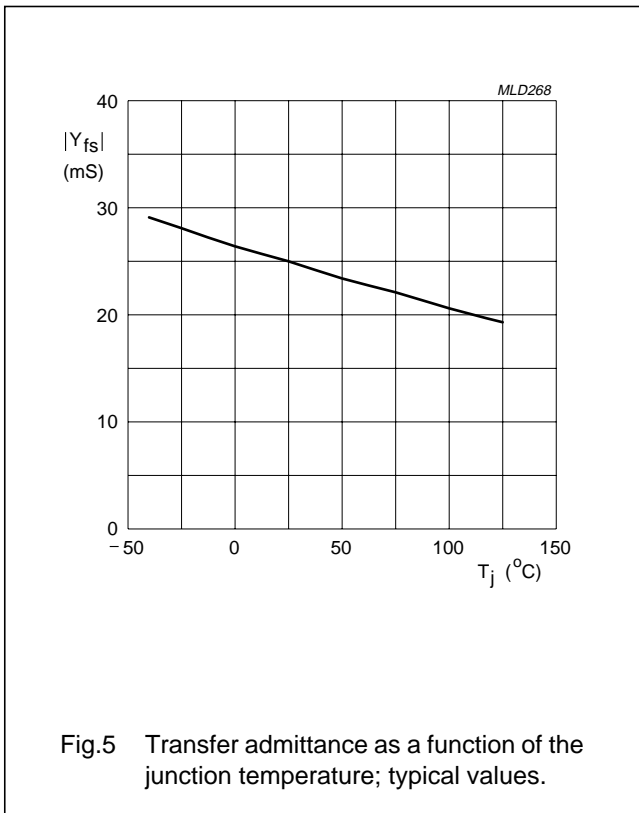
## DYNAMIC CHARACTERISTICS

Common source;  $T_{amb} = 25\text{ °C}$ ;  $V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 10\text{ mA}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ °C}$	22	25	30	mS
$C_{ig1-s}$	input capacitance at gate 1	$f = 1\text{ MHz}$	–	2.2	2.6	pF
$C_{ig2-s}$	input capacitance at gate 2	$f = 1\text{ MHz}$	1	1.5	2	pF
$C_{os}$	drain-source capacitance	$f = 1\text{ MHz}$	1	1.4	1.7	pF
$C_{rs}$	reverse transfer capacitance	$f = 1\text{ MHz}$	–	25	35	fF
F	noise figure	$f = 200\text{ MHz}$ ; $G_S = 2\text{ mS}$ ; $B_S = B_{Sopt}$	–	1	1.5	dB
		$f = 800\text{ MHz}$ ; $G_S = G_{Sopt}$ ; $B_S = B_{Sopt}$	–	2	2.8	dB

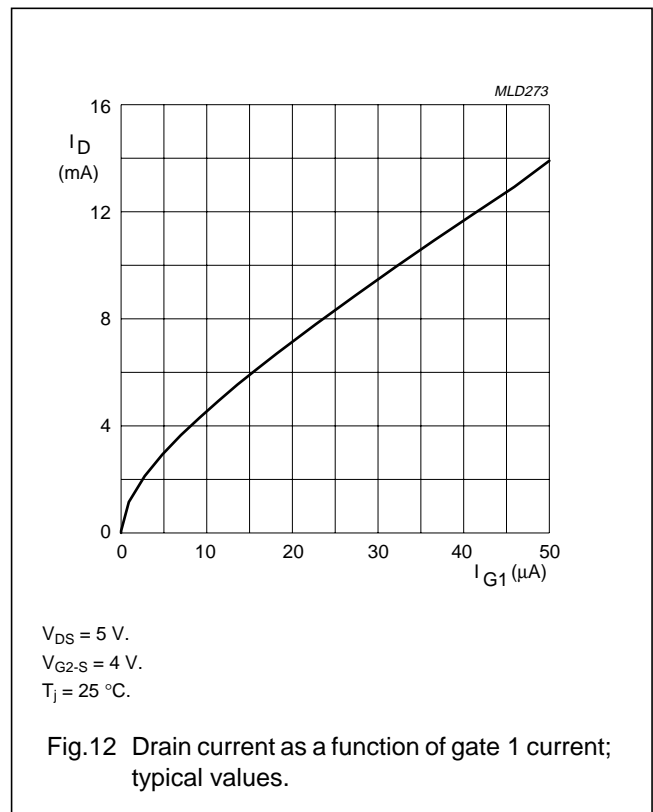
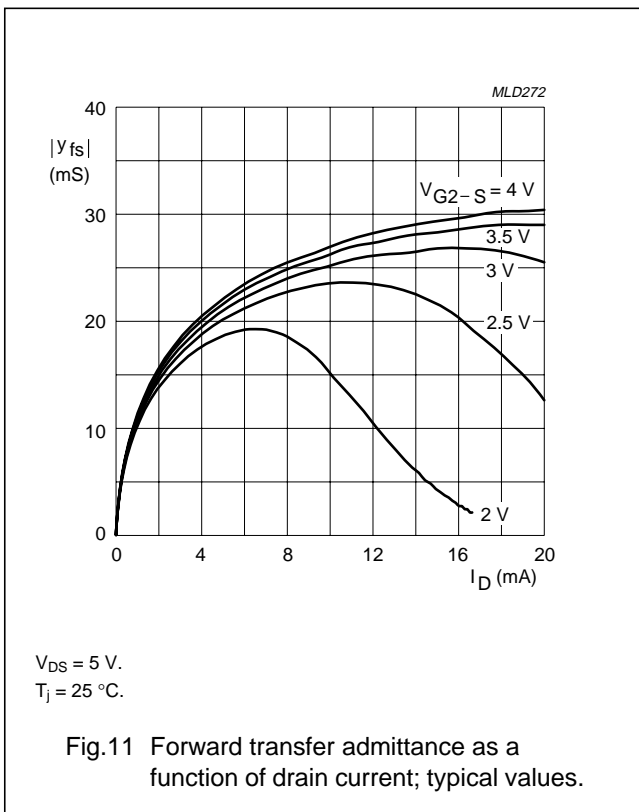
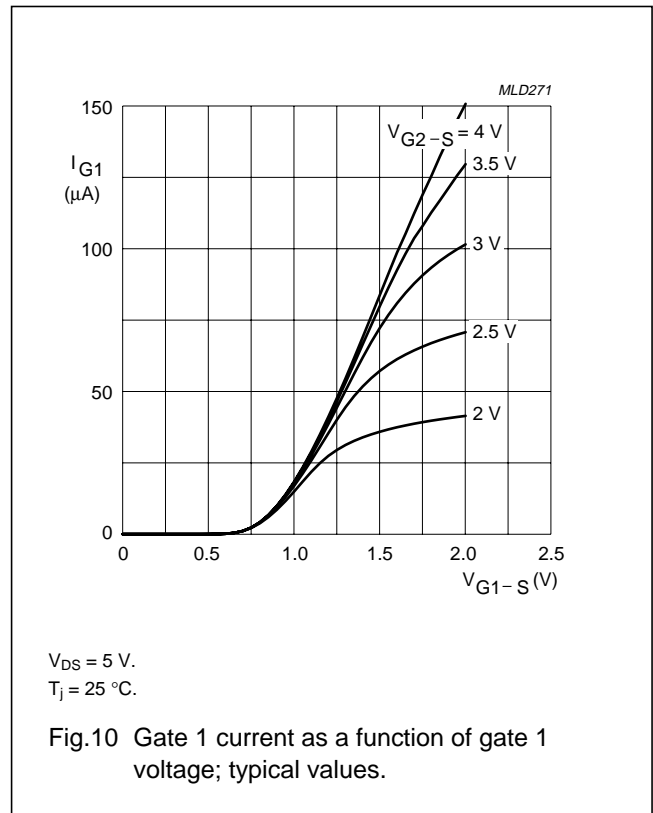
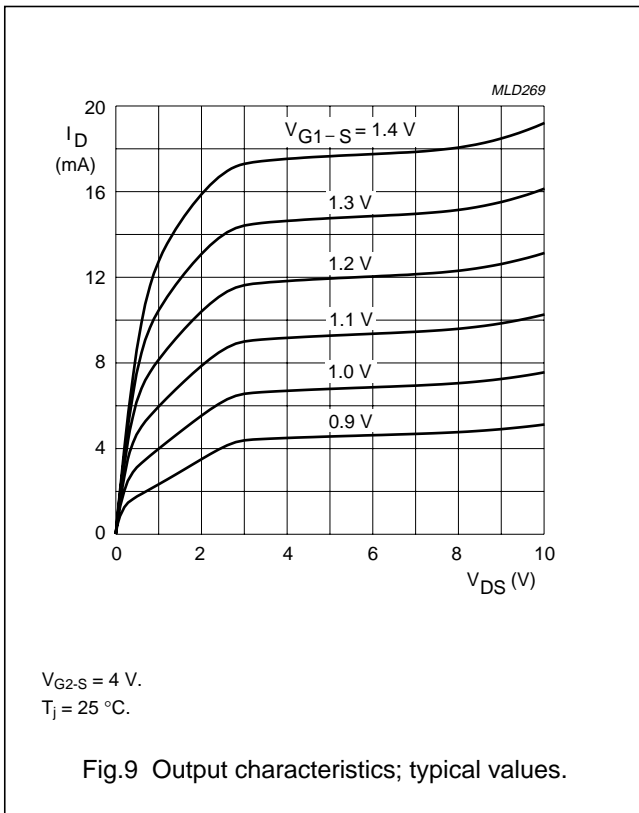
N-channel dual gate MOS-FETs

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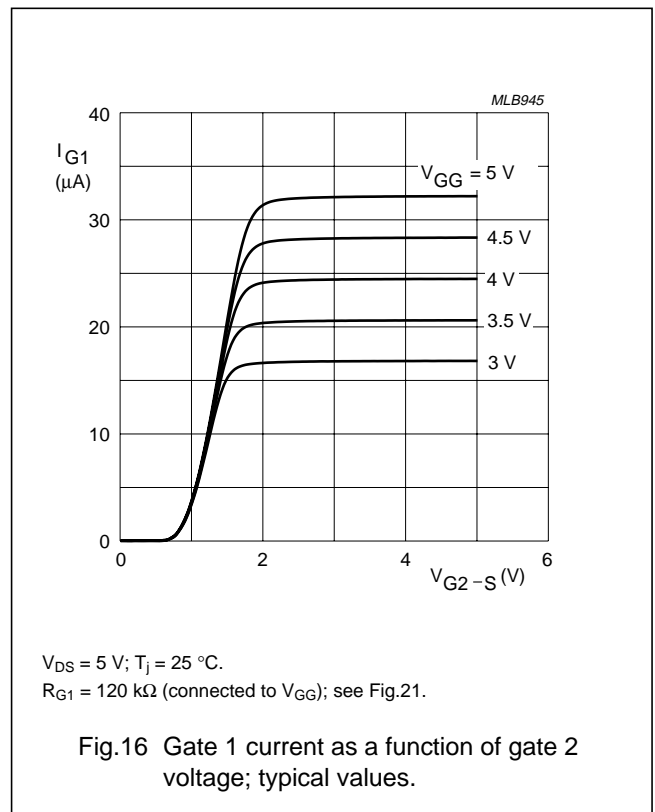
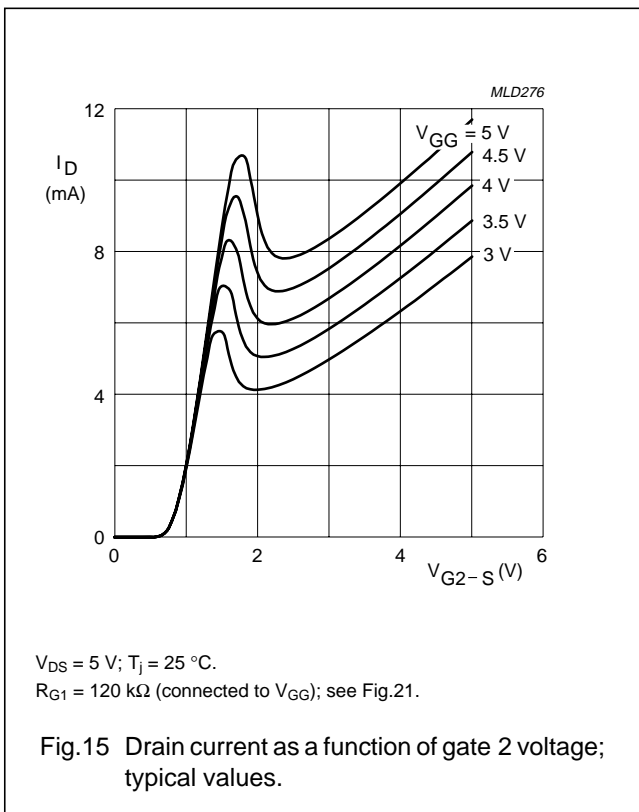
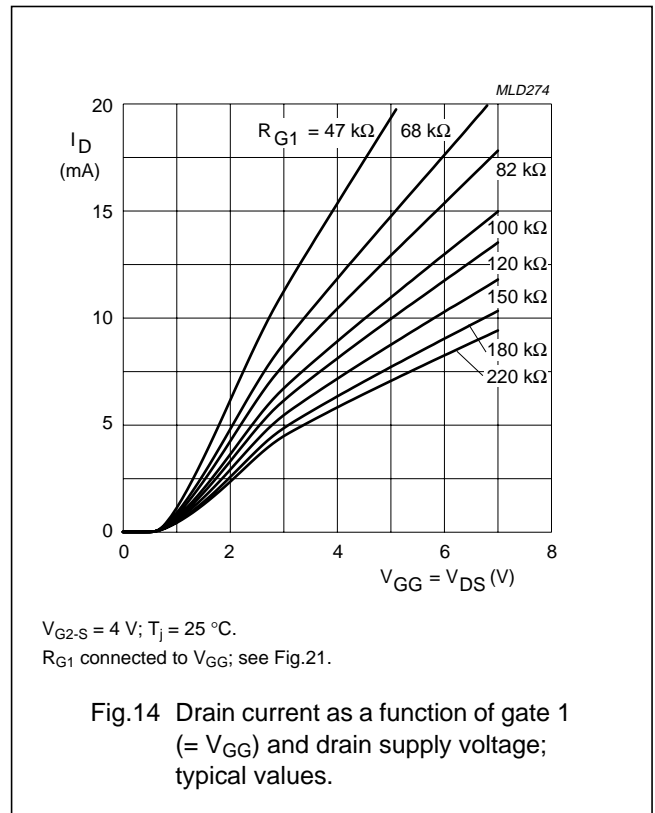
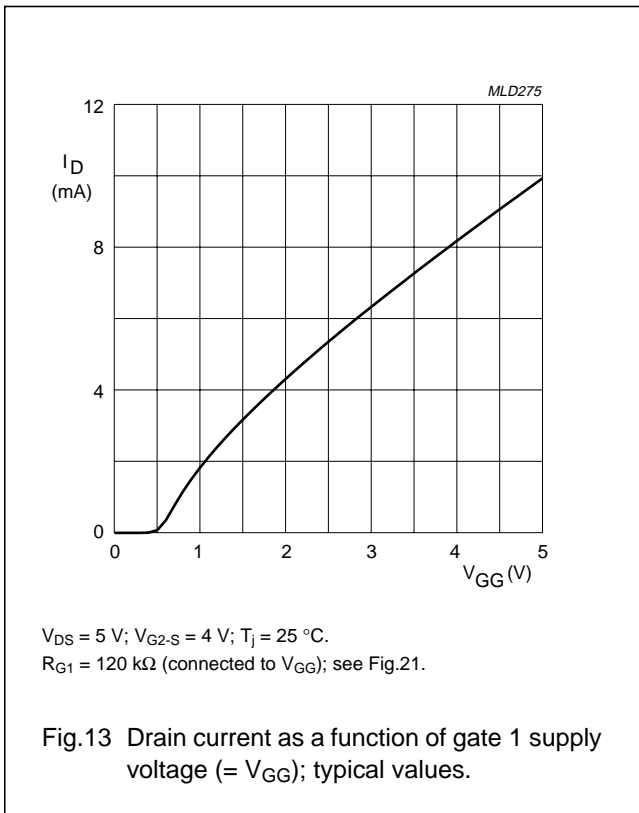
N-channel dual gate MOS-FETs

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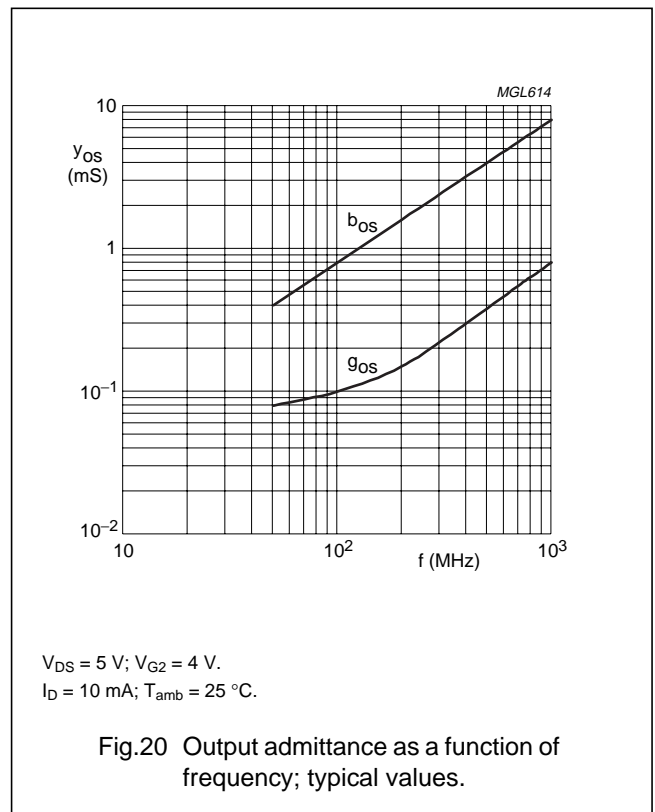
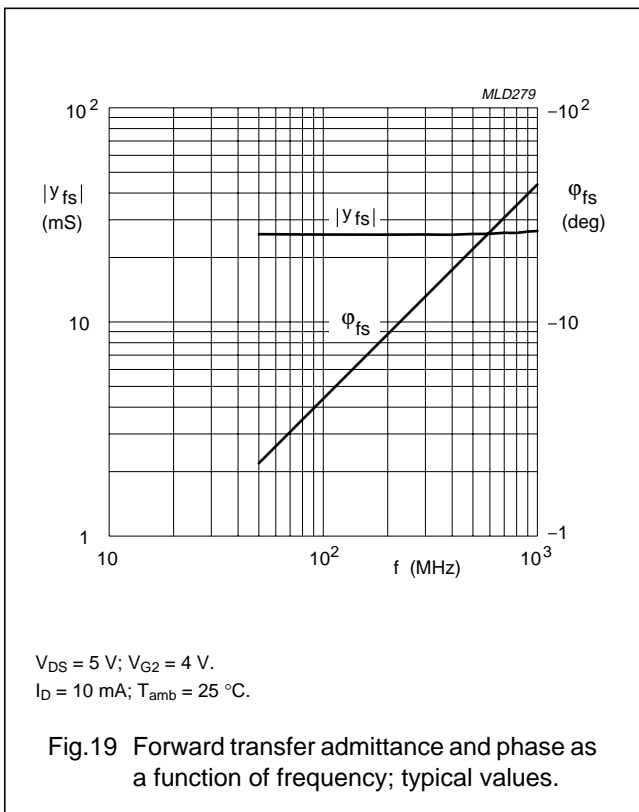
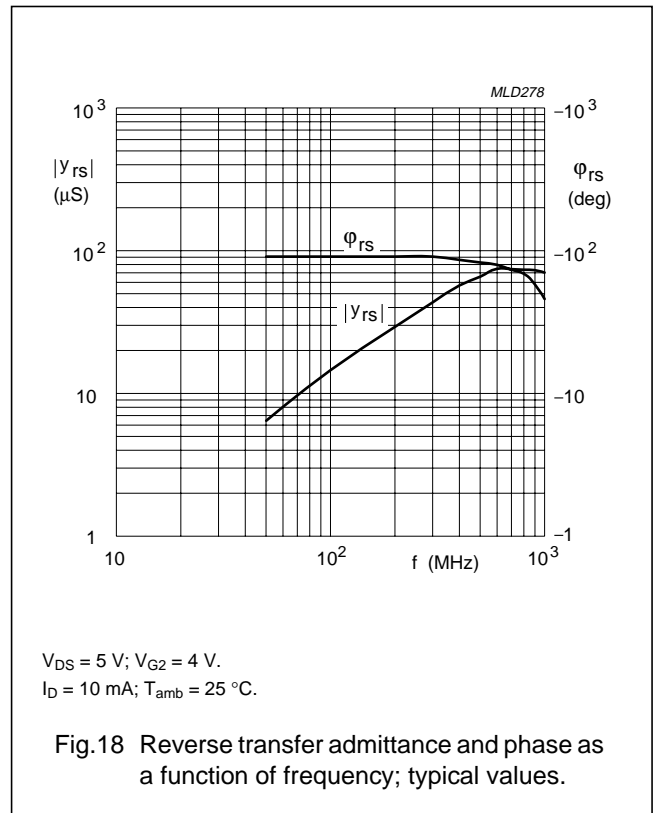
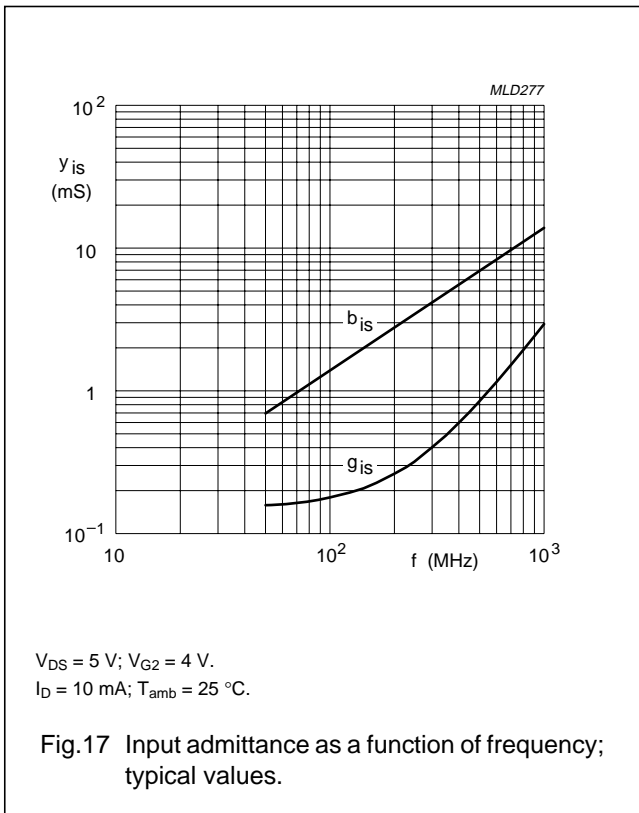
N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR



N-channel dual gate MOS-FETs

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N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR

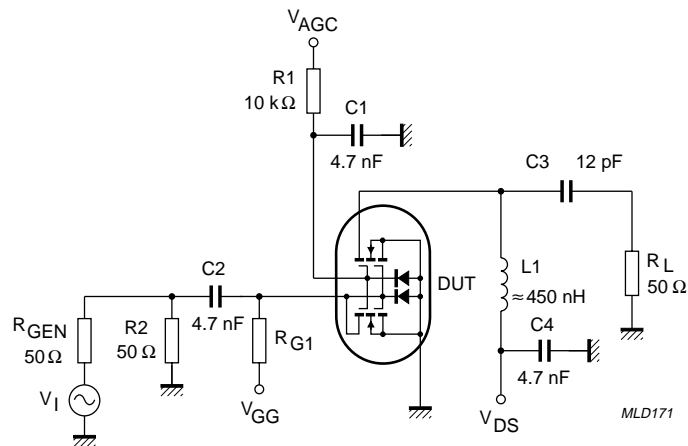


Fig.21 Cross-modulation test set-up.

## N-channel dual gate MOS-FETs

## BF904A; BF904AR; BF904AWR

**Table 1** Scattering parameters:  $V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 10\text{ mA}$ ;  $T_{amb} = 25\text{ °C}$ 

f (MHz)	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
40	0.989	-3.2	2.52	175.9	0.001	87.9	0.989	-1.7
100	0.987	-7.9	2.52	169.4	0.001	86.1	0.988	-4.3
200	0.976	-15.7	2.47	159.2	0.003	81.4	0.984	-8.6
300	0.972	-23.3	2.43	150.5	0.004	80.5	0.985	-12.7
400	0.947	-30.6	2.36	139.6	0.005	76.9	0.975	-16.9
500	0.925	-37.6	2.26	130.3	0.005	75.6	0.968	-20.8
600	0.905	-44.4	2.19	121.1	0.005	75.5	0.961	-24.7
700	0.883	-50.9	2.10	112.3	0.006	78.0	0.954	-28.4
800	0.861	-57.0	2.01	103.6	0.006	85.3	0.946	-32.0
900	0.841	-63.0	1.93	95.5	0.006	90.7	0.934	-35.6
1000	0.822	-68.4	1.85	87.8	0.006	102.6	0.931	-39.3
1200	0.787	-78.9	1.71	72.3	0.007	127.1	0.923	-46.7
1400	0.752	-88.1	1.59	57.3	0.011	143.7	0.926	-54.2
1600	0.723	-97.3	1.47	40.1	0.019	150.0	0.935	-62.2
1800	0.685	-106.3	1.36	25.0	0.021	149.4	0.931	-69.3
2000	0.665	-114.0	1.31	7.7	0.026	151.5	0.930	-77.7
2200	0.659	-119.8	1.30	-14.0	0.035	158.2	0.944	-89.1
2400	0.670	-124.2	1.26	-42.2	0.050	163.4	0.941	-103.5
2600	0.700	-129.3	1.10	-78.2	0.076	162.2	0.849	-119.7
2800	0.729	-138.7	0.82	-120.8	0.106	150.5	0.642	-130.9
3000	0.726	-150.1	0.52	-162.8	0.128	137.4	0.480	-130.6

**Table 2** Noise data:  $V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 10\text{ mA}$ ;  $T_{amb} = 25\text{ °C}$ 

f (MHz)	F <sub>min</sub> (dB)	Γ <sub>opt</sub>		R <sub>n</sub> (Ω)
		(ratio)	(deg)	
800	2.0	0.686	49.6	50.4

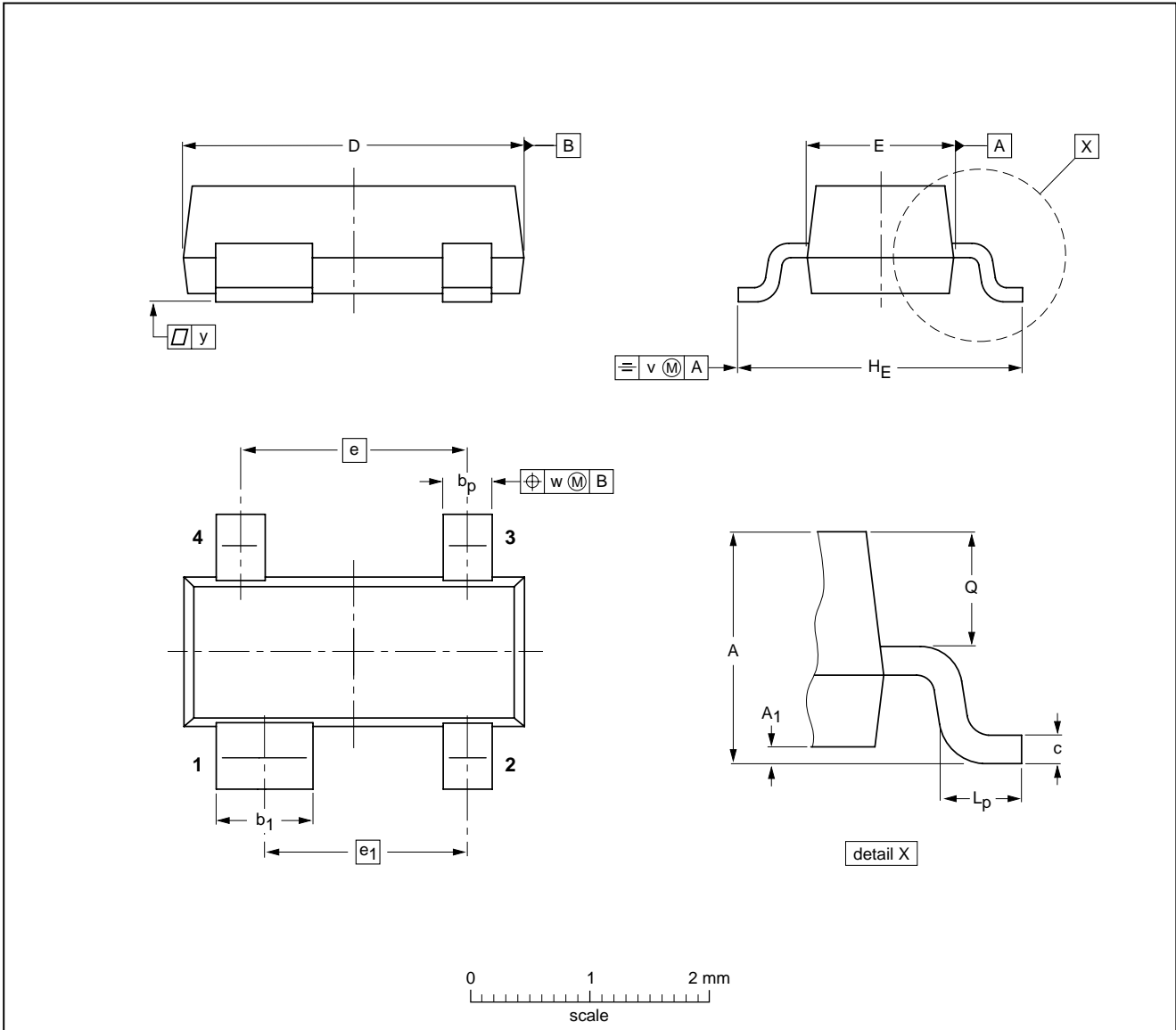
N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR

PACKAGE OUTLINES

Plastic surface mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

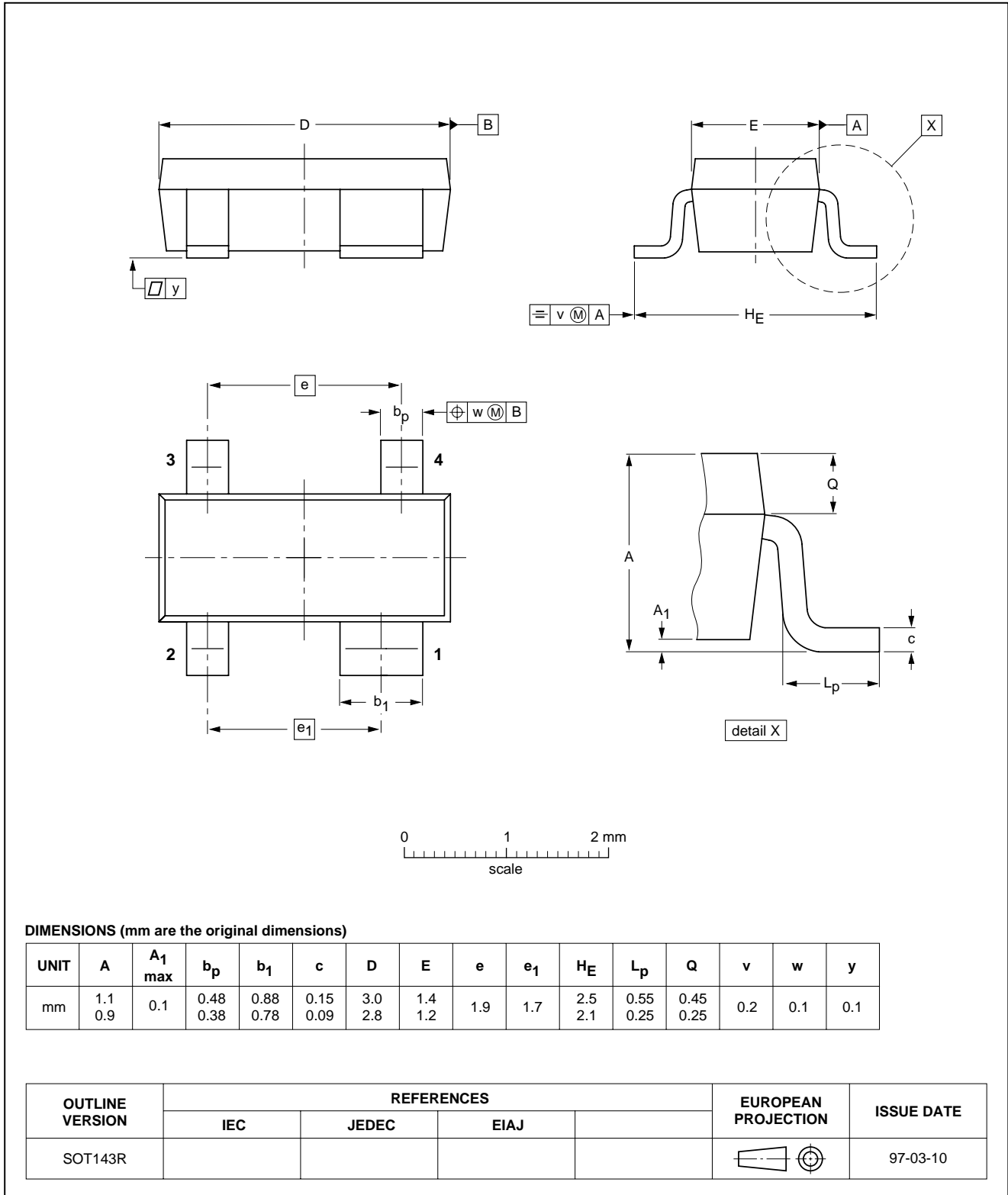
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	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR

Plastic surface mounted package; reverse pinning; 4 leads

SOT143R

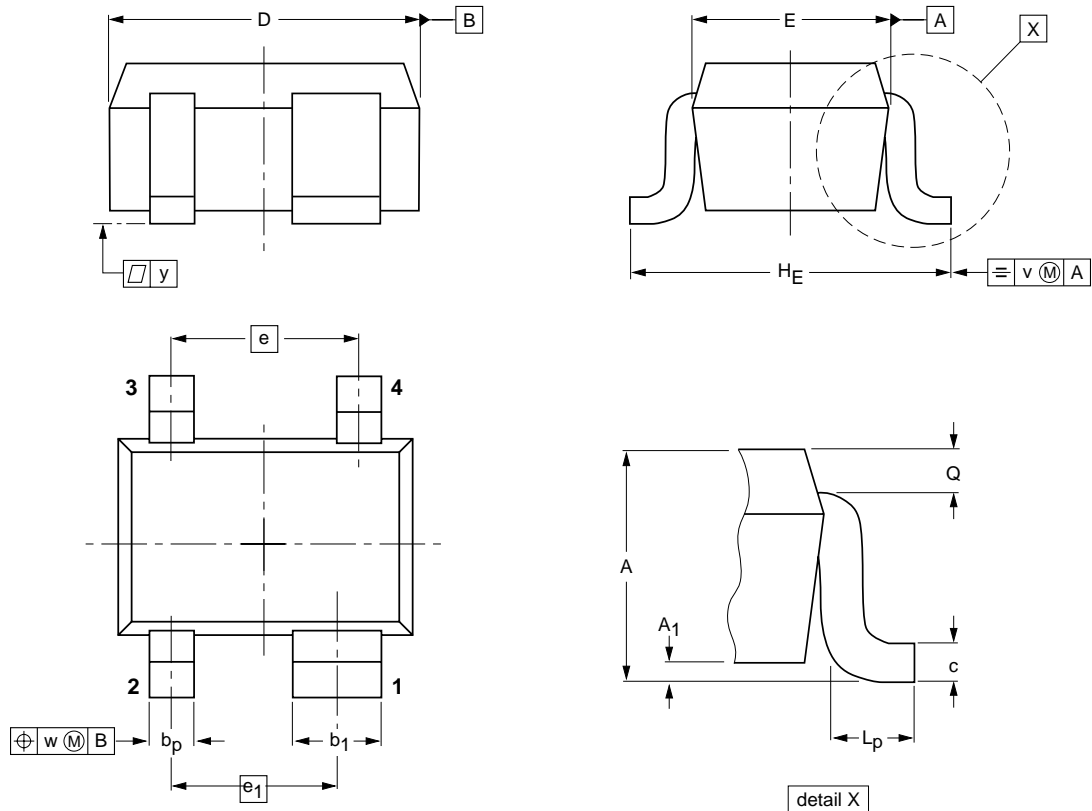


N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR

Plastic surface mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21

## N-channel dual gate MOS-FETs

## BF904A; BF904AR; BF904AWR

**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

N-channel dual gate MOS-FETs

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