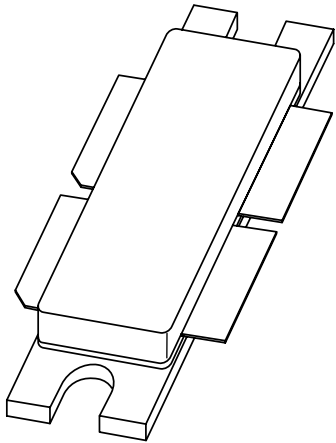


DATA SHEET



BLF2048 UHF push-pull power LDMOS transistor

Preliminary specification

1999 Nov 23

UHF push-pull power LDMOS transistor

BLF2048

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (HF to 2.2 GHz).

APPLICATIONS

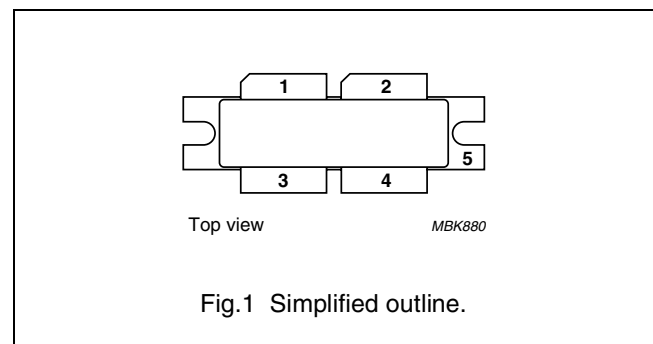
- Common source class-AB operation for PCN and PCS applications in the 1800 to 2200 MHz frequency range.

DESCRIPTION

Push-pull silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 4-lead flange package (SOT539A) with a ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT539A

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source connected to flange



QUICK REFERENCE DATA

RF performance at $T_h = 25^\circ\text{C}$ in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
class-AB (2-tone)	$f_1 = 2200; f_2 = 2200.1$	26	120 (PEP)	>10	>30	≤ -26
		28	140 (PEP)	typ. 11.2	typ. 31	typ. -25

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	± 15	V
I_D	drain current (DC)		–	18	A
T_{stg}	storage temperature		–65	+150	$^\circ\text{C}$
T_j	junction temperature		–	200	$^\circ\text{C}$

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-mb}$	thermal resistance from junction to mounting-base	$P_L = 120\text{ W}$; $T_{mb} = 50\text{ }^\circ\text{C}$, note 1	0.35	K/W
$R_{th\ mb-h}$	thermal resistance from mounting-base to heatsink		0.15	K/W

Note

1. Thermal resistance is determined under nominal 2-tone RF operating conditions.

CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$; per section; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 1.4\text{ mA}$	65	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 140\text{ mA}$	1.5	–	3.5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 26\text{ V}$	–	–	10	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 9\text{ V}$; $V_{DS} = 10\text{ V}$	18	–	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 15\text{ V}$; $V_{DS} = 0$	–	–	250	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 5\text{ A}$	–	4	–	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 9\text{ V}$; $I_D = 5\text{ A}$	–	0.17	–	Ω
C_{rs}	feedback capacitance	$V_{GS} = 0$; $V_{DS} = 26\text{ V}$; $f = 1\text{ MHz}$	–	3.4	–	pF

Notes

1. Capacitance of die only.

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. $T_h = 25\text{ }^\circ\text{C}$; $R_{th\ j-h} = 0.5\text{ K/W}$; unless otherwise specified..

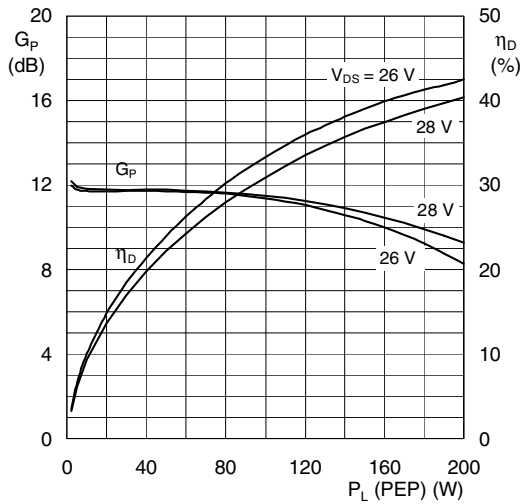
MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
class-AB (2-tone)	$f_1 = 2200$; $f_2 = 2200.1$	26	2 x 400	120 (PEP)	>10	>30	≤ -26
		28	2 x 400	140 (PEP)	typ. 11.2	typ. 31	typ. -25

Ruggedness in class-AB operation

The BLF2048 is capable of withstanding a load mismatch corresponding to $VSWR = 10 : 1$ through all phases under the following conditions: $V_{DS} = 26\text{ V}$; $f = 2200\text{ MHz}$, $P_L = 120\text{ W}$ (CW).

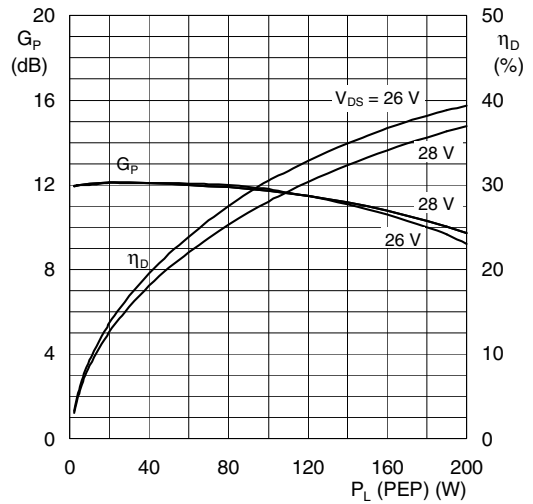
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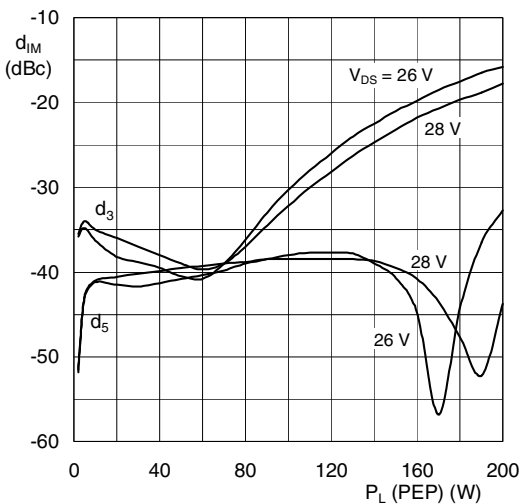
$f_1 = 2000 \text{ MHz}; f_2 = 2000.1 \text{ MHz};$
 $I_{DQ} = 2 \times 400 \text{ mA}; T_h \leq 25 \text{ }^\circ\text{C}.$

Fig.2 Power gain and drain efficiency as functions of peak envelope load power; typical values.



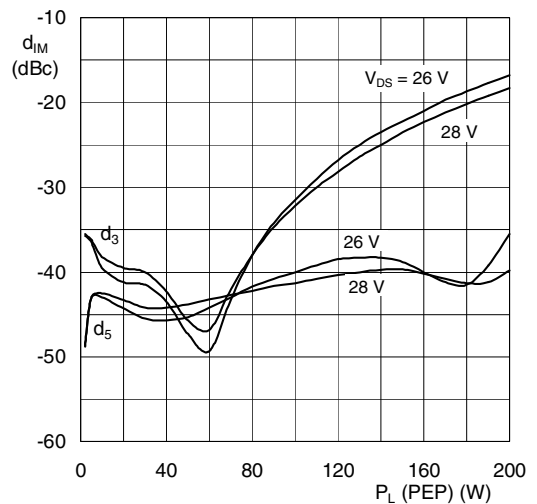
$f_1 = 2200 \text{ MHz}; f_2 = 2200.1 \text{ MHz};$
 $I_{DQ} = 2 \times 400 \text{ mA}; T_h \leq 25 \text{ }^\circ\text{C}.$

Fig.3 Power gain and drain efficiency as functions of peak envelope load power; typical values.



$f_1 = 2000 \text{ MHz}; f_2 = 2000.1 \text{ MHz};$
 $I_{DQ} = 2 \times 400 \text{ mA}; T_h \leq 25 \text{ }^\circ\text{C}.$

Fig.4 Intermodulation distortion as a function of peak envelope load power; typical values.

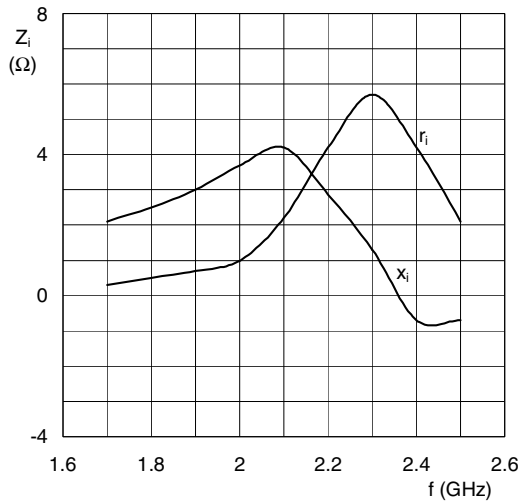


$f_1 = 2200 \text{ MHz}; f_2 = 2200.1 \text{ MHz};$
 $I_{DQ} = 2 \times 400 \text{ mA}; T_h \leq 25 \text{ }^\circ\text{C}.$

Fig.5 Intermodulation distortion as a function of peak envelope load power; typical values.

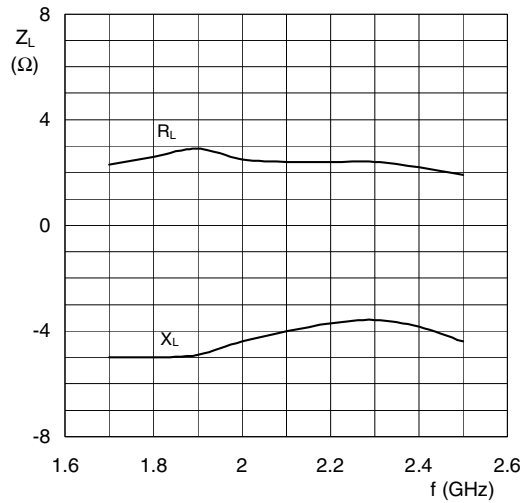
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$V_{DS} = 26 \text{ V}$; $I_{DQ} = 2 \times 400 \text{ mA}$; $P_L = 160 \text{ W}$ (total device);
 $T_h \leq 25 \text{ }^\circ\text{C}$.

Fig.6 Input impedance per section as a function of frequency (series components); typical values.



$V_{DS} = 26 \text{ V}$; $I_{DQ} = 2 \times 400 \text{ mA}$; $P_L = 160 \text{ W}$ (total device);
 $T_h \leq 25 \text{ }^\circ\text{C}$.

Fig.7 Load impedance per section as a function of frequency (series components); typical values.

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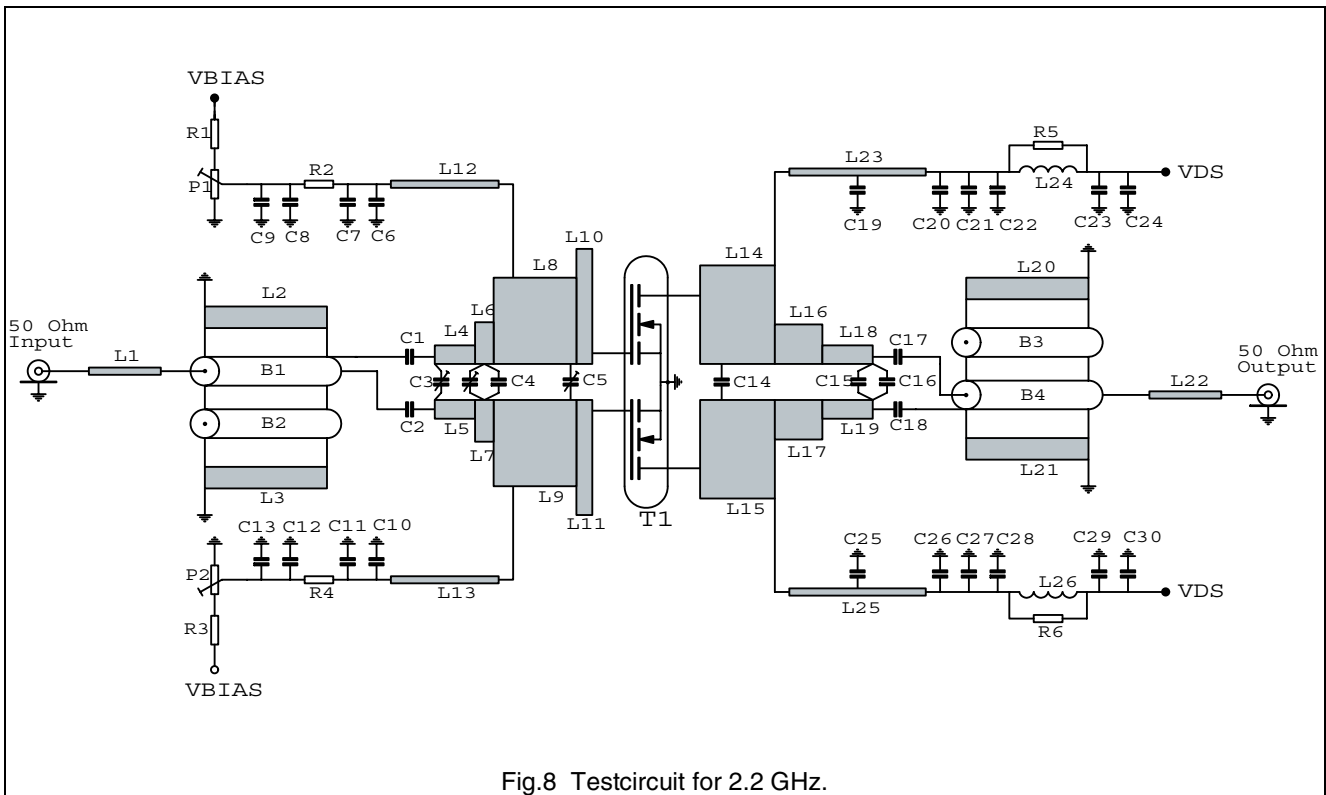


Fig.8 Testcircuit for 2.2 GHz.

List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor; note 1	5.1 pF		
C3, C5	Tekelec variable capacitor	0.6 to 4.5 pF		
C4	Tekelec variable capacitor + multilayer ceramic chip capacitor; note 1	0.6 to 4.5 pF + 2.4 pF		
C6, C10	multilayer ceramic chip capacitor; note 2	100 pF		
C7, C11	multilayer ceramic chip capacitor; note 2	18 pF		
C8, C12, C23, C29	tantal SMD capacitor	4.7 μF; 35 V		
C9, C13, C24, C30	tantal SMD capacitor	10 μF; 35 V		
C14	multilayer ceramic chip capacitor; note 3	0.5 pF		
C15	multilayer ceramic chip capacitor; note 3	1 pF		
C16	multilayer ceramic chip capacitor; note 1	1.5 pF		
C17, C18	multilayer ceramic chip capacitor; note 1	10 pF		
C19, C25	MKT ceramic chip capacitor	33 nF		2222 370 11333
C20, C26	multilayer ceramic chip capacitor; note 2	6.2 pF		
C21, C27	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C22, C28	multilayer ceramic chip capacitor; note 1	8.2 pF		

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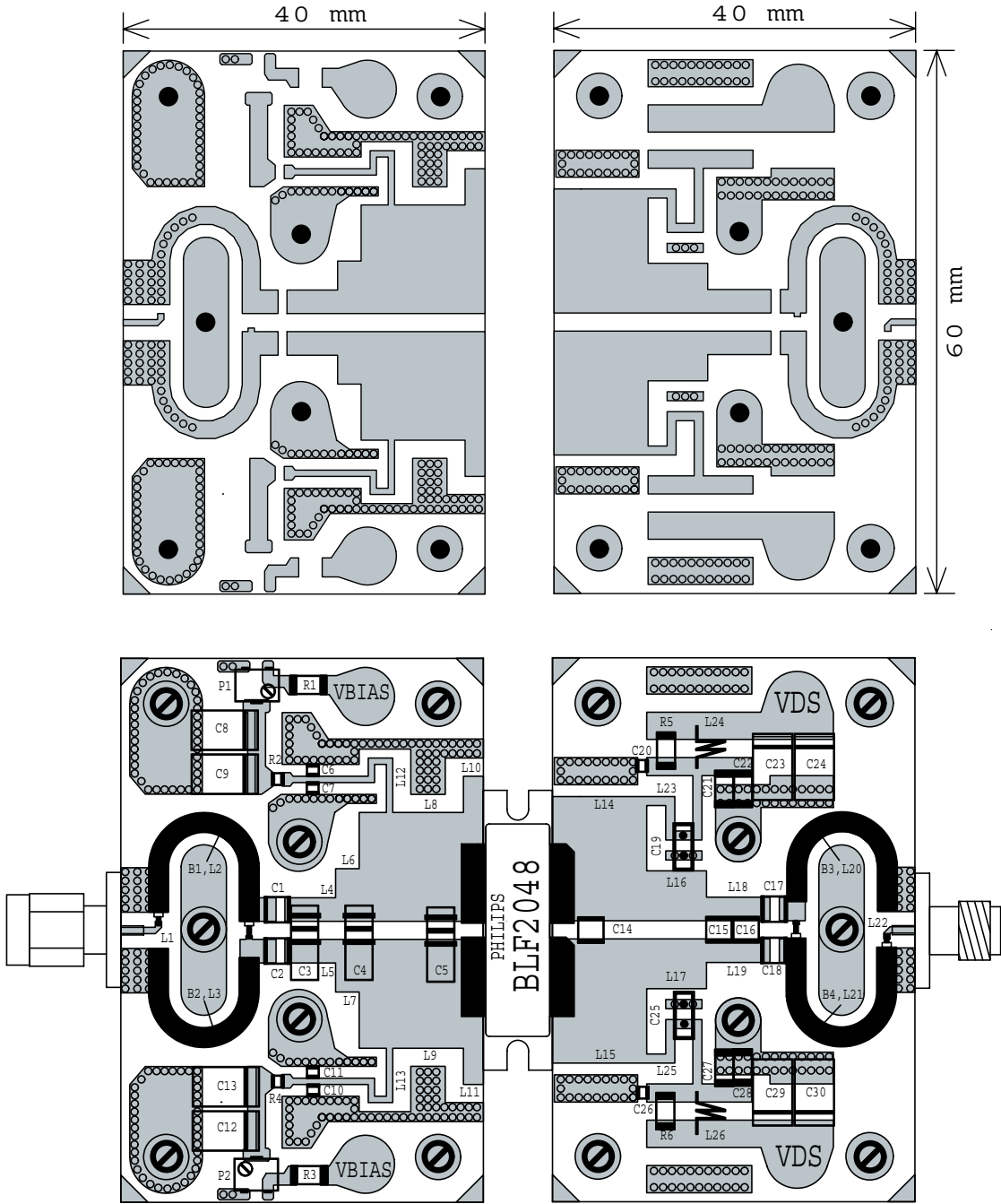
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L1	stripline; note 4	47 Ω	4.5 \times 1 mm	
L2, L3, L20, L21	stripline; note 4		15 \times 2 mm	
L4, L5	stripline; note 4		5.6 \times 2.6 mm	
L6, L7	stripline; note 4		2.6 \times 5.8 mm	
L8, L9	stripline; note 4		11.5 \times 12 mm	
L10, L11	stripline; note 4		2.2 \times 16 mm	
L12, L13	stripline; note 4	57 Ω	1/4 λ @ 2.2 GHz	
L14, L15	stripline; note 4		10.4 \times 13.7 mm	
L16, L17	stripline; note 4		6.6 \times 5.5 mm	
L18, L19	stripline; note 4		7 \times 2.6 mm	
L22	stripline; note 4	47 Ω	4 x 1 mm	
L23, L25	stripline; note 4	47 Ω	1/4 λ @ 2.2 GHz	
L24, L26	1 turn enamelled 0.7 mm copper wire		int.dia. 7 mm; length mm	
B1, B4	balun of semi-rigid cable	50 Ω		
B2, B3	semi-rigid cable; note 5	50 Ω		
R1, R3, R5, R6	metal film resistor	5.6 Ω , 0.6 W		
R2, R4	metal film resistor	10 Ω , 0.6 W		
P1, P2	variable resistor (multiturn)	5 k Ω		

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. American Technical Ceramics type 100A or capacitor of same quality.
3. American Technical Ceramics type 180R or capacitor of same quality.
4. Semi-rigid cable soldered along the stub to establish balance.
5. The striplines are on a double copper-clad PCB with Teflon dielectric ($\epsilon_r = 6.15$); thickness 0.64 mm.

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Dimensions in mm.
The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric ($\epsilon_r = 6.15$), thickness 0.64 mm.
The other side is unetched and serves as a ground plane.

Fig.9 Component layout for 2.2 GHz class-AB testcircuit.

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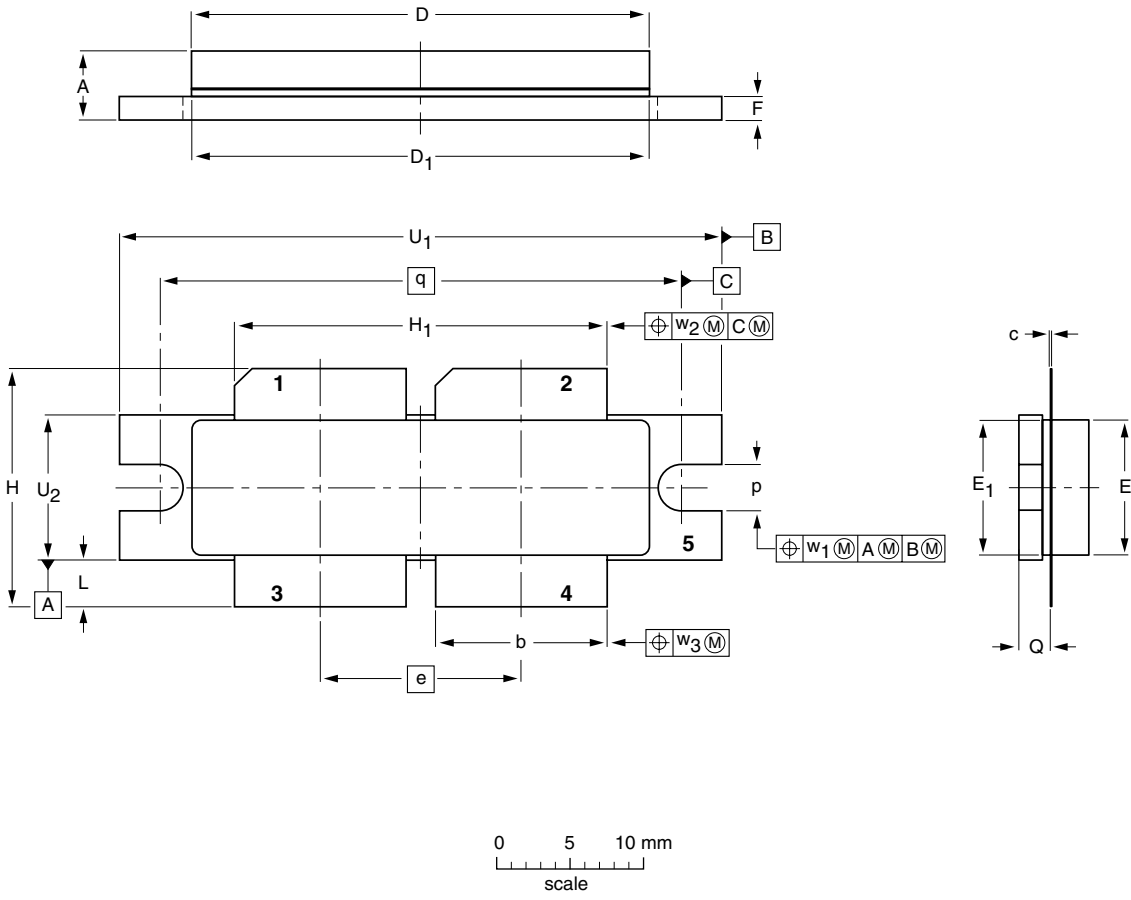
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PACKAGE OUTLINE

Flanged balanced LDMOST package; 2 mounting holes; 4 leads

SOT539A

Package under development
 Philips Semiconductors reserves the right to make changes without notice.



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	w ₁	w ₂	w ₃
mm	5.33 3.96	11.81 11.56	0.15 0.08	31.55 30.94	31.65 30.96	13.72	9.50 9.20	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.73 2.72	3.30 3.05	2.31 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.210 0.156	0.465 0.455	0.006 0.003	1.242 1.218	1.246 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.147 0.107	0.130 0.120	0.091 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						99-05-10 99-06-25

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 62 5344, Fax.+381 11 63 5777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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Printed in The Netherlands

125108/00/01/pp11

Date of release: 1999 Nov 23

Document order number: 9397 750 06582

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传真：0755-83376182 (0) 13823648918 MSN: SUNS8888@hotmail.com

邮编：518033 E-mail:szss20@163.com QQ: 195847376

深圳赛格展销部：深圳华强北路赛格电子市场 2583 号 电话：0755-83665529 25059422

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西安分公司：西安高新开发区 20 所(中国电子科技集团导航技术研究所)

西安劳动南路 88 号电子商城二楼 D23 号

TEL: 029-81022619 13072977981 FAX:029-88789382