DATA SHEET

BLF245B
VHF push-pull power MOS transistor

Product specification

September 1992

Philips Semiconductors

PHILIPS

VHF push-pull power MOS transistor BLF245B

FEATURES

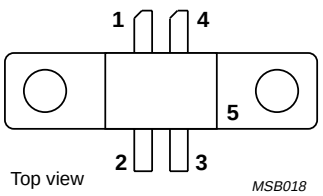
- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT279 balanced flange envelope, with a ceramic cap. The mounting flange provides the common source connection for the transistors.

PIN CONFIGURATION



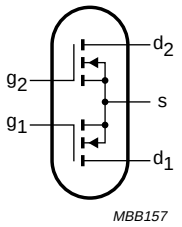


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

PINNING - SOT279

PIN	DESCRIPTION
1	gate 1
2	drain 1
3	gate 2
4	drain 2
5	source

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_P (dB)	η_D (%)
CW, class-B	175	28	30	> 14	> 55

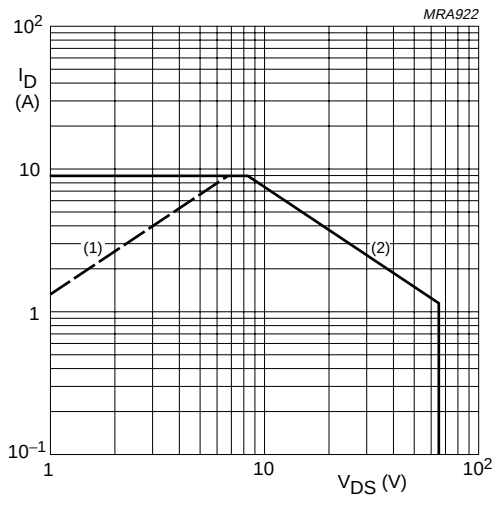
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	4.5	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	75	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

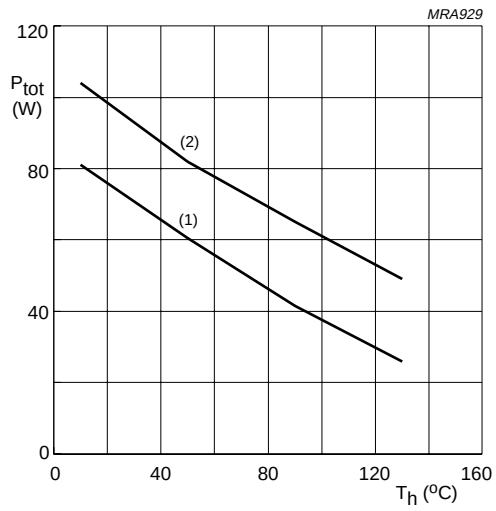
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	2.3 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.3 K/W



(1) Current in this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



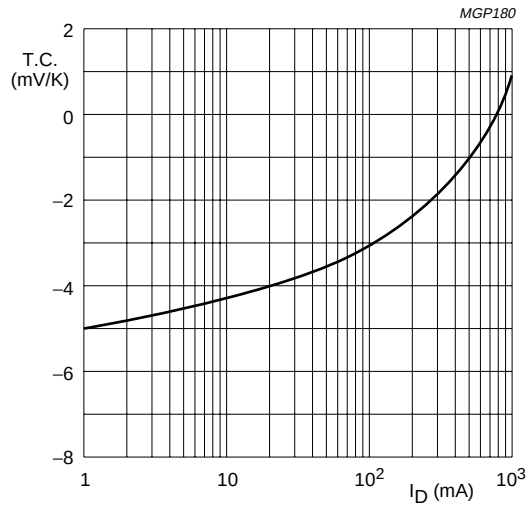
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

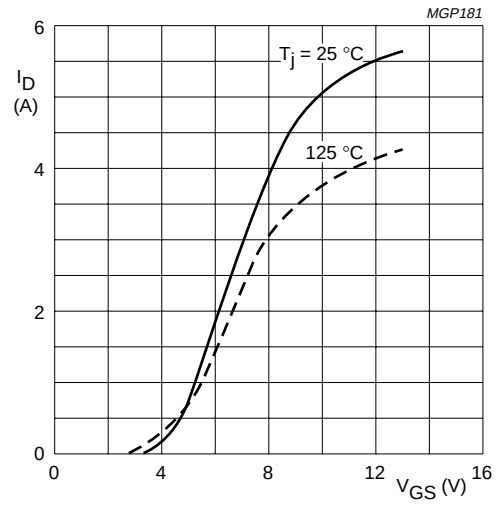
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 5 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	µA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 5 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.75 A; V_{DS} = 10 V	600	850	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.75 A; V_{GS} = 10 V	–	0.8	1.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	5	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	60	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	40	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	4.5	–	pF



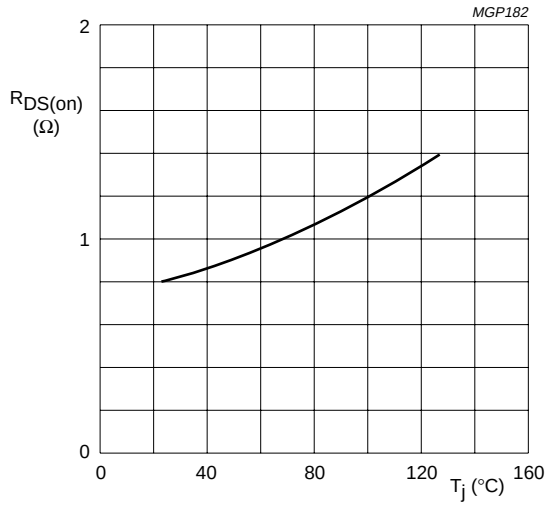
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



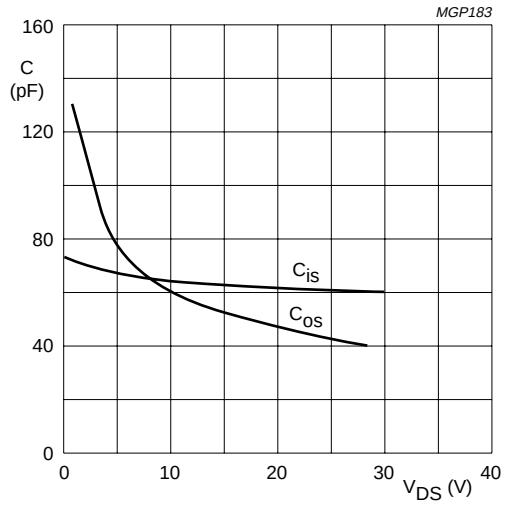
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



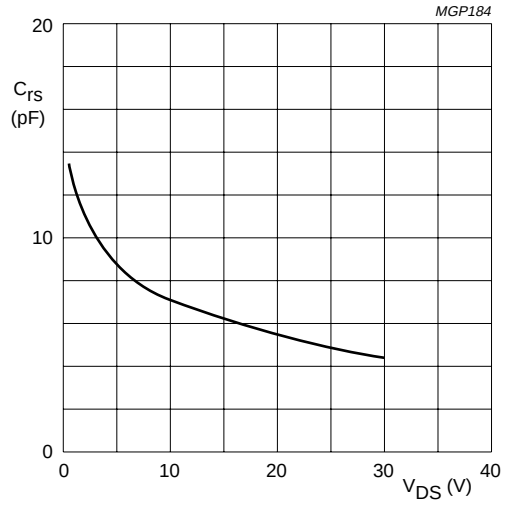
I_D = 0.75 A; V_{GS} = 10 V

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W; unless otherwise specified.

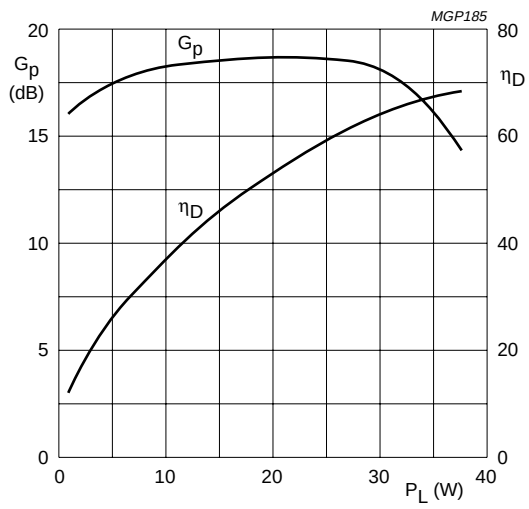
RF performance in a push-pull, common source, class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_P (dB)	η_D (%)
CW, class-B	175	28	2×25	30	> 14 typ. 18	> 55 typ. 65

Ruggedness in class-B operation

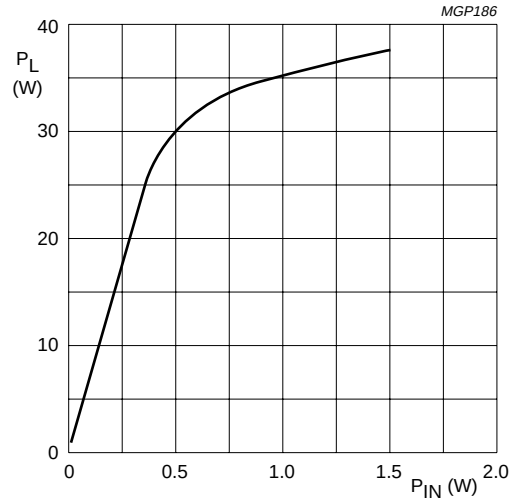
The BLF245B is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases, under the following conditions:

V_{DS} = 28 V, f = 175 MHz at rated output power.



Class-B operation; V_{DS} = 28 V; $I_{DQ} = 2 \times 25$ mA; $Z_L = 8.8 + j12.7\ \Omega$; f = 175 MHz.

Fig.9 Power gain and efficiency as functions of output power, typical values.



Class-B operation; V_{DS} = 28 V; $I_{DQ} = 2 \times 25$ mA; $Z_L = 8.8 + j12.7\ \Omega$; f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.

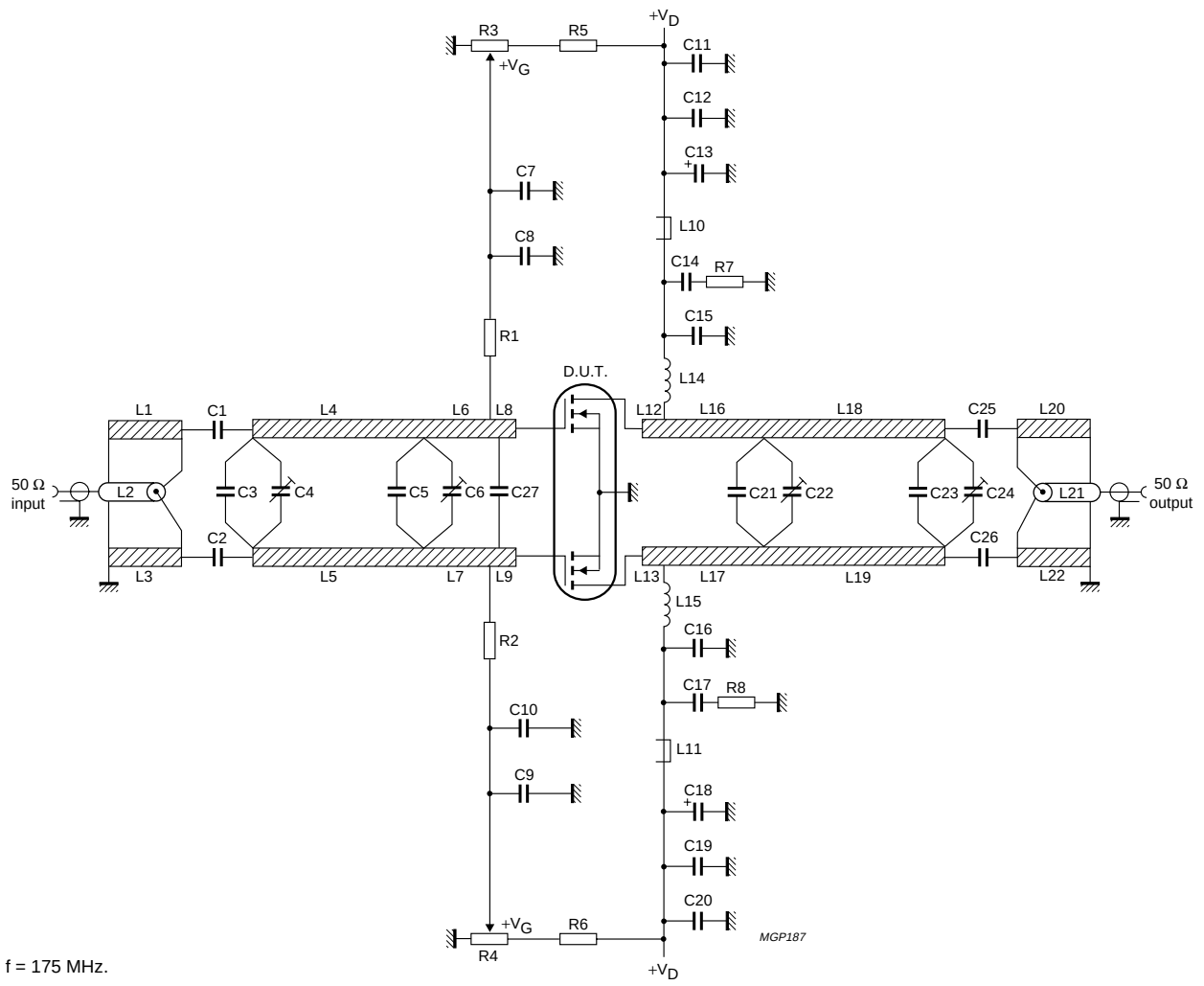


Fig.11 Test circuit for class-B operation.

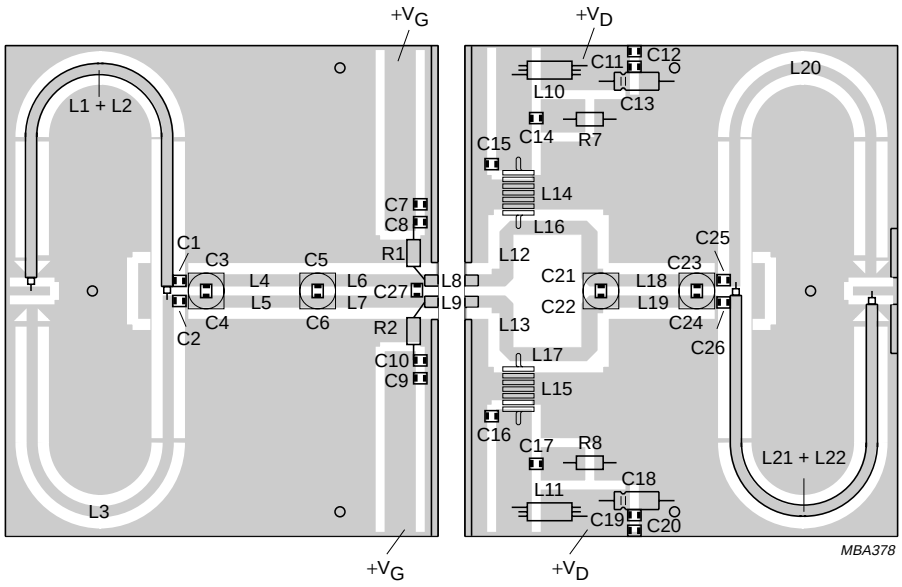
List of components (see test circuit)

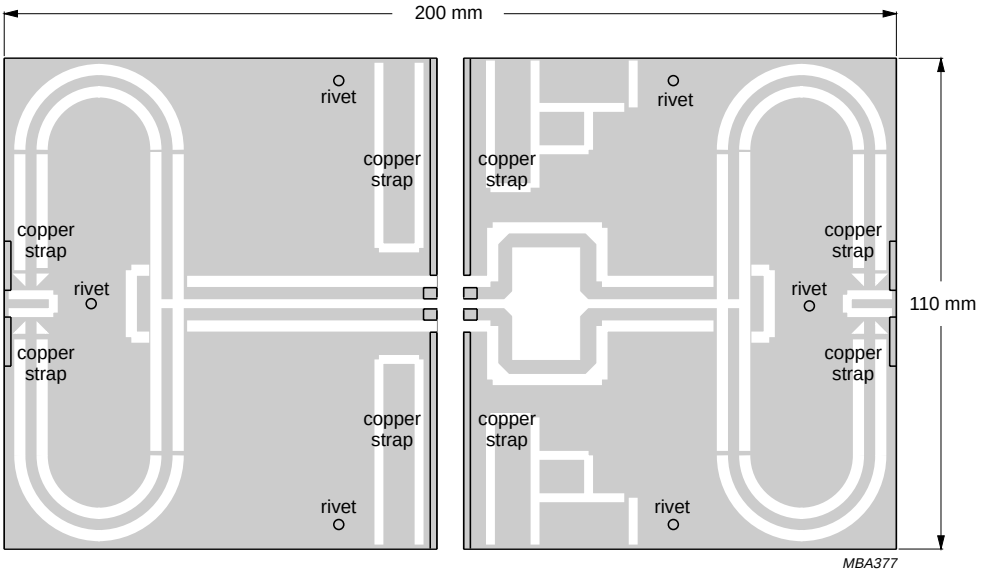
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	270 pF		
C3	multilayer ceramic chip capacitor (note 1)	24 pF		
C4	film dielectric trimmer	4 to 60 pF		2222 809 08002
C5, C25, C26	multilayer ceramic chip capacitor (note 1)	91 pF		
C6, C22, C24	film dielectric trimmer	5 to 60 pF		2222 809 08003
C7, C9, C12, C14, C17, C19	multilayer ceramic chip capacitor	100 nF		2222 852 47104

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C8, C10	multilayer ceramic chip capacitor (note 1)	680 pF		
C11, C20	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C13, C18	electrolytic capacitor	10 μF, 63 V		
C15, C16	multilayer ceramic chip capacitor (note 1)	100 pF		
C21, C27	multilayer ceramic chip capacitor (note 1)	75 pF		
C23	multilayer ceramic chip capacitor (note 1)	36 pF		
L1, L3, L20, L22	stripline (note 2)	55 Ω	length 111 mm width 2.5 mm	
L2, L21	semi-rigid cable	50 Ω	length 111 mm ext. dia. 2.2 mm	
L4, L5	stripline (note 2)	49.5 Ω	length 28 mm width 3 mm	
L6, L7	stripline (note 2)	49.5 Ω	length 22.5 mm width 3 mm	
L8, L9	stripline (note 2)	49.5 Ω	length 4.5 mm width 3 mm	
L10, L11	grade 3B Ferroxcube RF choke			4312 020 36642
L12, L13	stripline (note 2)	49.5 Ω	length 21 mm width 3 mm	
L14, L15	4 turns enamelled 1 mm copper wire	70 nH	length 9 mm int. dia. 6 mm leads 2 × 5 mm	
L16, L17	stripline (note 2)	49.5 Ω	length 30 mm width 3 mm	
L18, L19	stripline (note 2)	49.5 Ω	length 26 mm width 3 mm	
R1, R2	0.4 W metal film resistor	10 Ω		
R3, R4	10 turns potentiometer	50 Ω		
R5, R6	0.4 W metal film resistor	205 kΩ		
R7, R8	0.4 W metal film resistor	10 Ω		

Notes

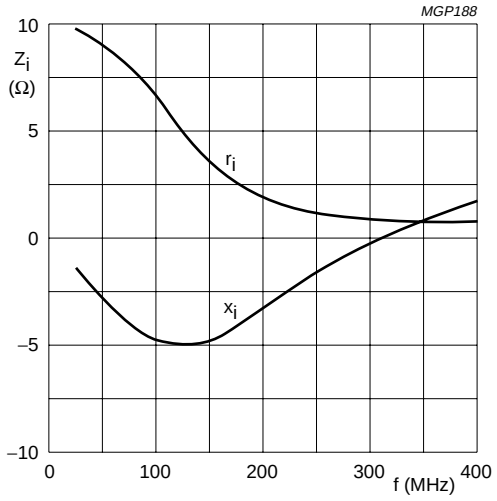
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy glass dielectric ($\varepsilon_r = 4.5$), thickness $\frac{1}{16}$ inch. The other side of the board is fully metallized and used as a ground plane. The ground planes on each side of the board are connected together by means of copper straps and hollow rivets.





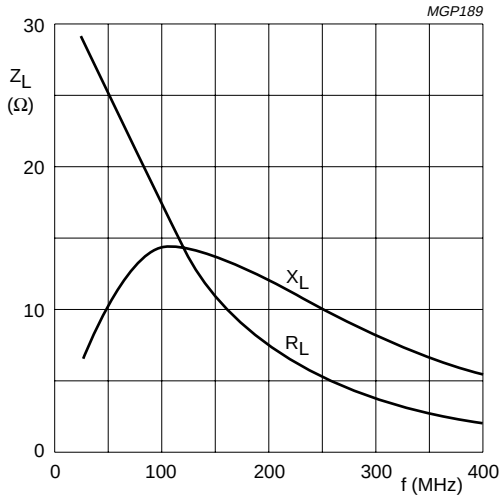
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as a ground. Earth connections are made by means of copper straps and hollow rivets for a direct contact between the upper and lower sheets.

Fig.12 Component layout for 175 MHz test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 25 mA;
R_{GS} = 10 Ω; P_L = 30 W (total device).

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 25 mA;
R_{GS} = 10 Ω; P_L = 30 W (total device).

Fig.14 Load impedance as a function of frequency (series components), typical values per section.

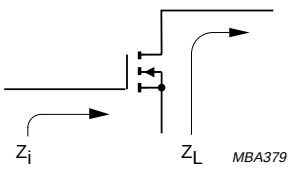
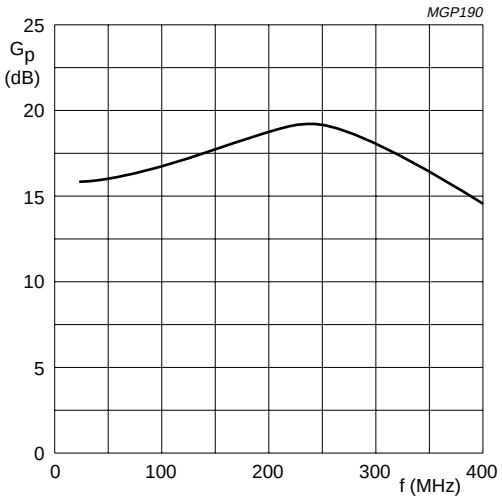


Fig.15 Definition of MOS impedance.

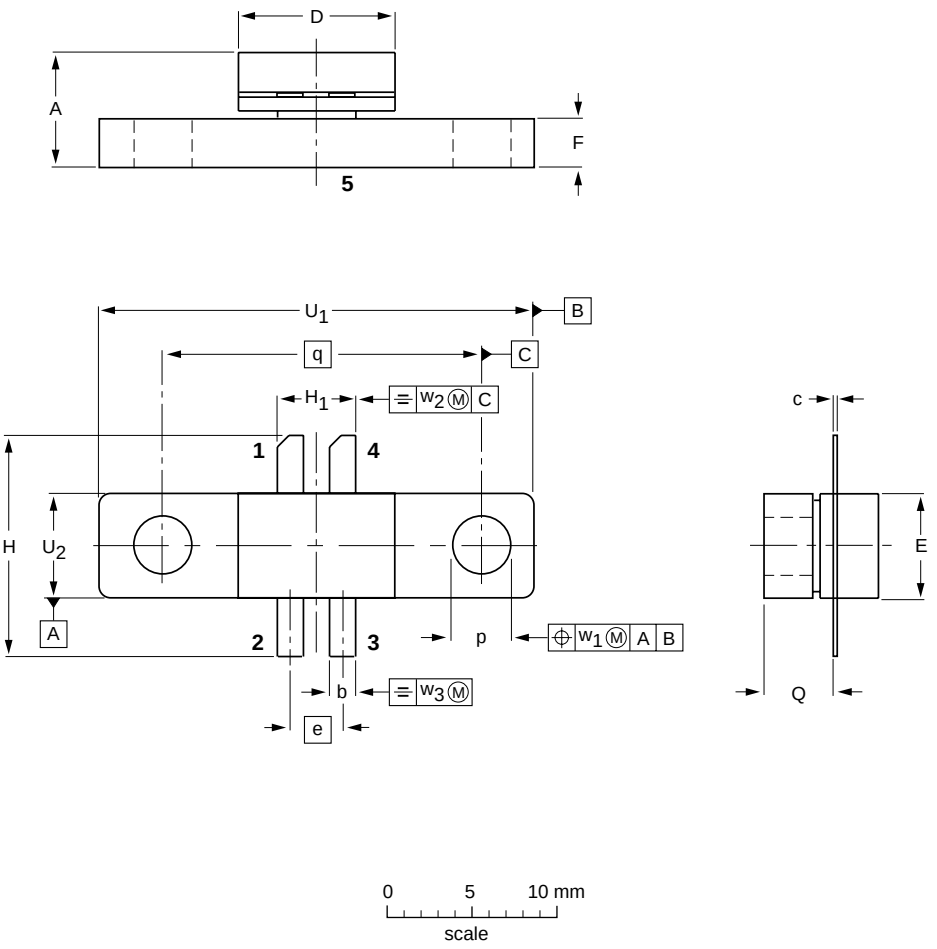


Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 25 mA;
R_{GS} = 10 Ω; P_L = 30 W (total device).

Fig.16 Power gain as a function of frequency, typical values per section.

PACKAGE OUTLINE

Flanged double-ended ceramic package; 2 mounting holes; 4 leads **SOT279A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	6.84 6.01	1.66 1.39	0.16 0.10	9.28 9.01	5.97 5.71	3.05	3.05 2.54	12.96 11.93	4.96 4.19	3.48 3.22	4.35 4.03	18.42	24.90 24.63	5.97 5.71	0.51	1.02	0.25
inches	0.269 0.237	0.065 0.055	0.006 0.004	0.365 0.355	0.235 0.225	0.12	0.120 0.100	0.51 0.47	0.195 0.165	0.137 0.127	0.171 0.159	0.725	0.98 0.97	0.235 0.225	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT279A						97-06-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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