

DATA SHEET

BLF548 UHF push-pull power MOS transistor

Product specification

October 1992

UHF push-pull power MOS transistor

BLF548

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT262A2 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PIN CONFIGURATION

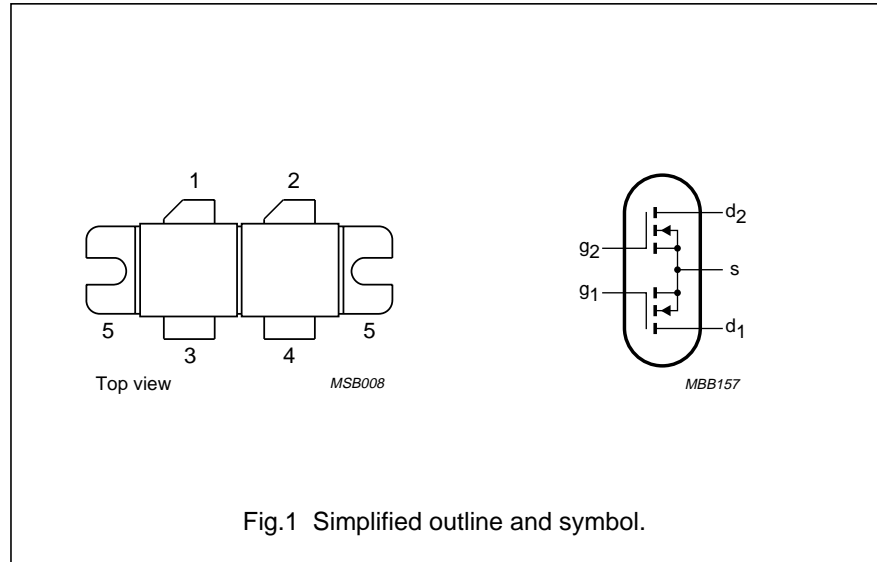


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

PINNING - SOT262A2

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at $T_h = 25\text{ °C}$ in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	150	> 10	> 50

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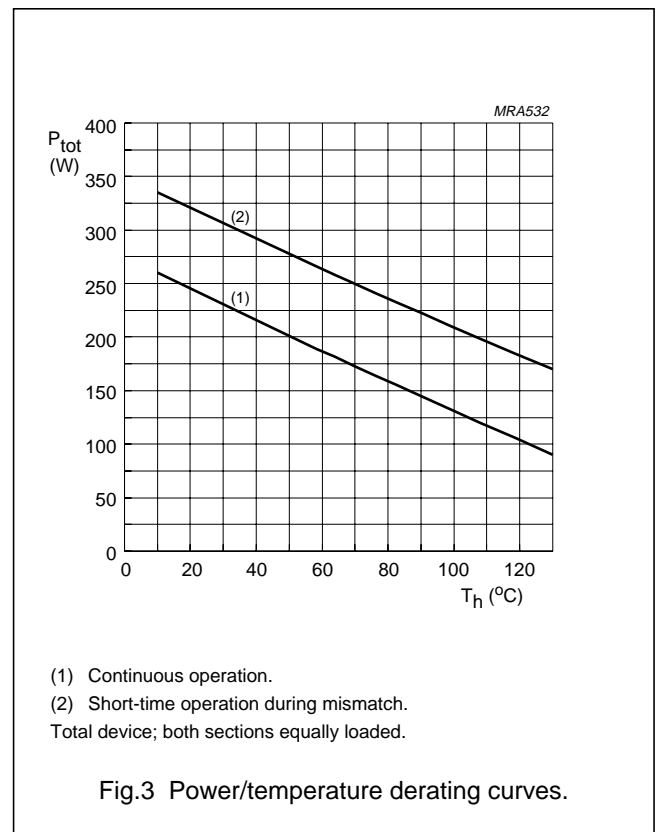
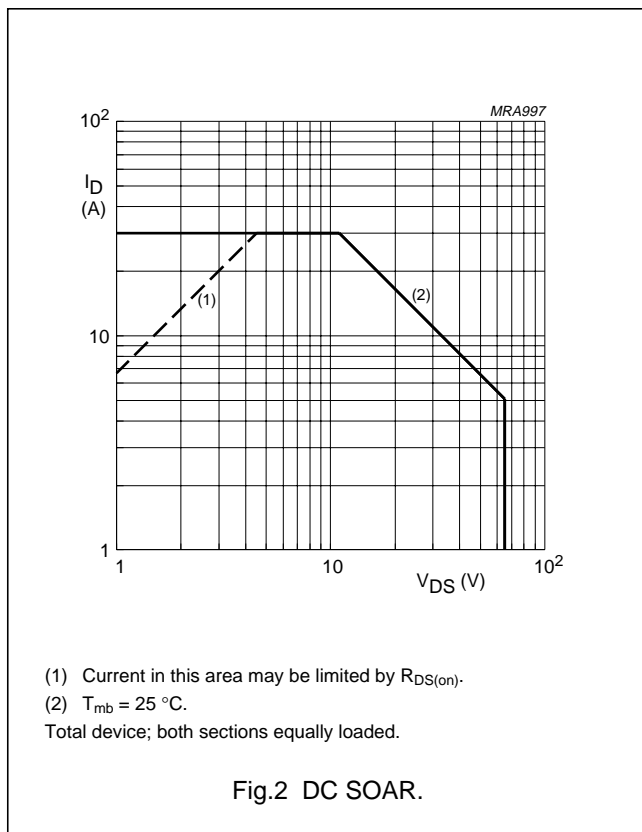
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	15	A
P_{tot}	total power dissipation	up to $T_{mb} = 25\text{ }^\circ\text{C}$; total device; both sections equally loaded	–	330	W
T_{stg}	storage temperature		–65	150	$^\circ\text{C}$
T_j	junction temperature		–	200	$^\circ\text{C}$

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	$T_{mb} = 25\text{ }^\circ\text{C}$; $P_{tot} = 330\text{ W}$; total device; both sections equally loaded	0.5 K/W
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.15 K/W



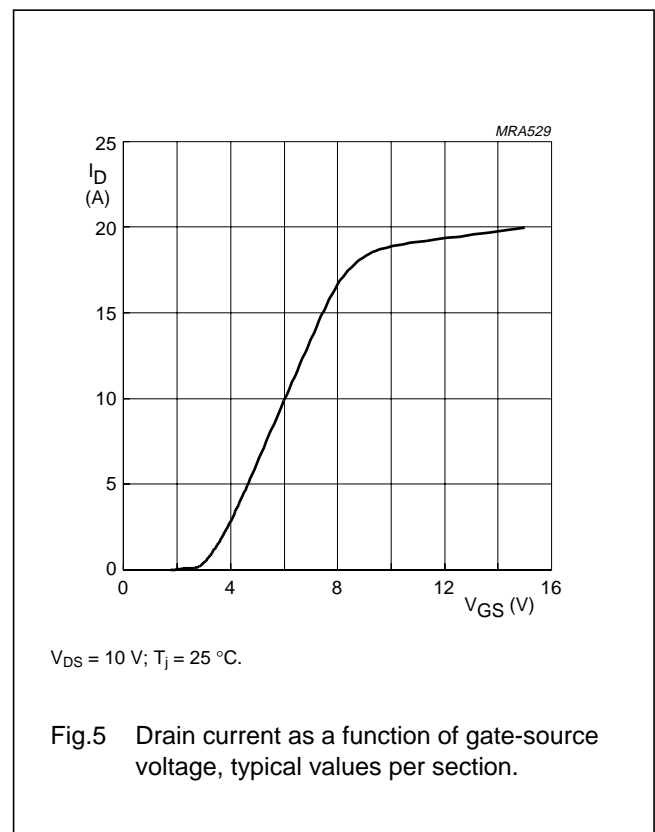
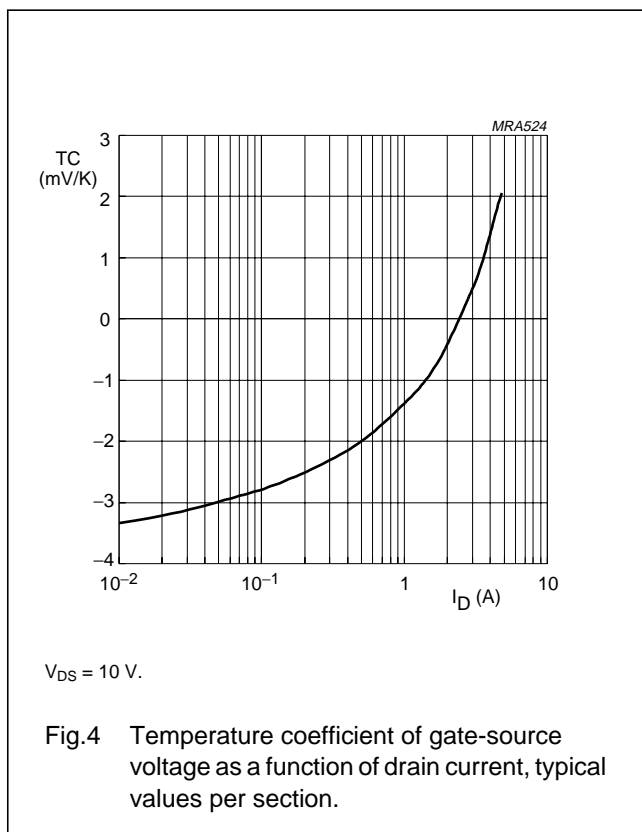
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CHARACTERISTICS (per section)

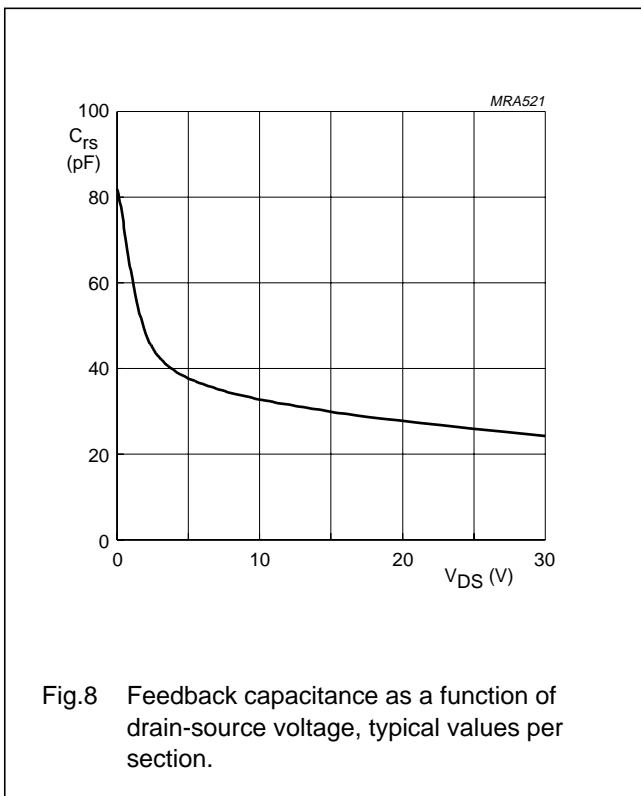
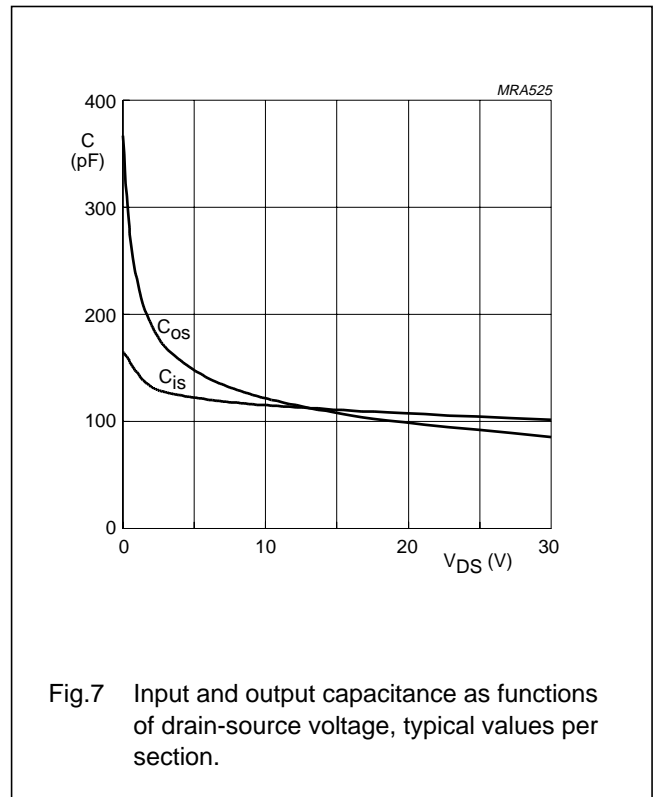
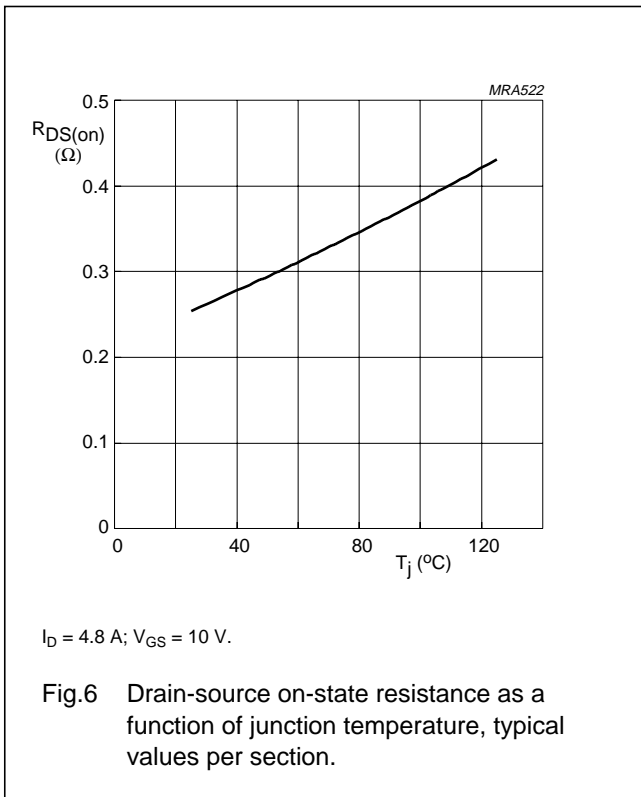
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = 40\text{ mA}$	65	–	–	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0; V_{DS} = 28\text{ V}$	–	–	0.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS} = 20\text{ V}; V_{DS} = 0$	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 160\text{ mA}; V_{DS} = 10\text{ V}$	2	–	4	V
g_{fs}	forward transconductance	$I_D = 4.8\text{ A}; V_{DS} = 10\text{ V}$	2.4	3.5	–	S
$R_{DS(on)}$	drain-source on-state resistance	$I_D = 4.8\text{ A}; V_{GS} = 10\text{ V}$	–	0.25	0.3	Ω
I_{DSX}	on-state drain current	$V_{GS} = 15\text{ V}; V_{DS} = 10\text{ V}$	16	20	–	A
C_{is}	input capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	105	–	pF
C_{os}	output capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	90	–	pF
C_{rs}	feedback capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	25	–	pF



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APPLICATION INFORMATION FOR CLASS-B OPERATION

$T_h = 25\text{ }^\circ\text{C}$; $R_{th\text{ mb-h}} = 0.15\text{ K/W}$, unless otherwise specified.

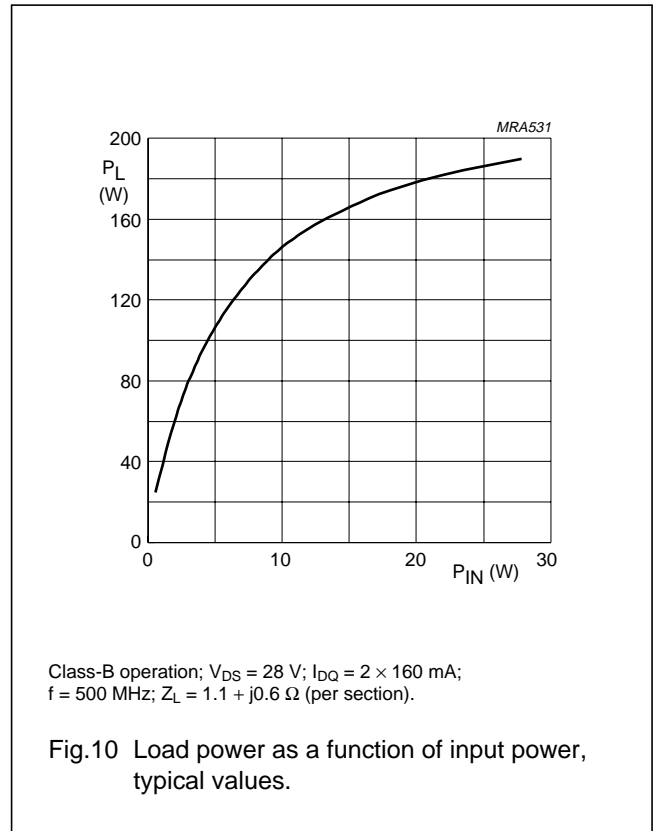
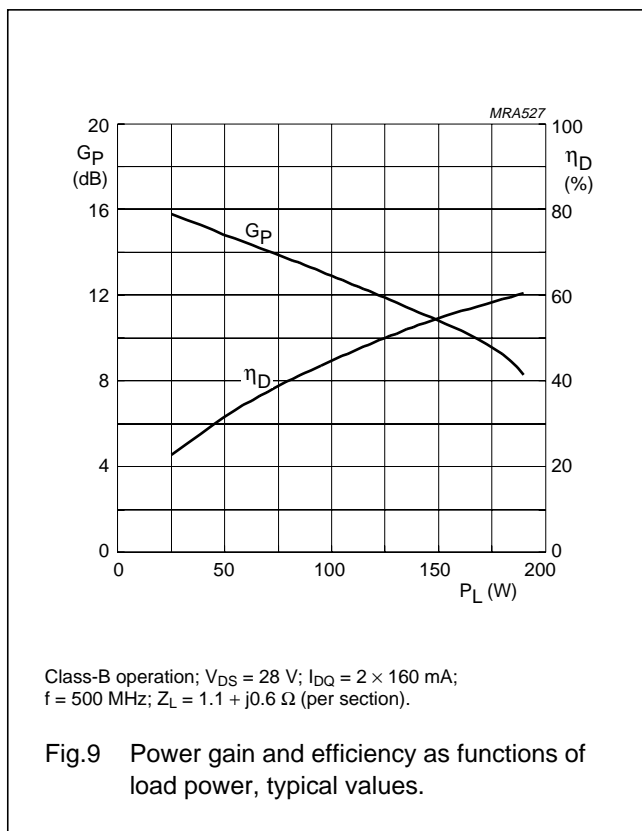
RF performance in a common source, push-pull, class-B test circuit.

MODE OF OPERATION	f (MHz)	V _{DS} (V)	I _{DQ} (mA)	P _L (W)	G _p (dB)	η _D (%)
CW, class-B	500	28	2 x 160	150	> 10 typ. 11	> 50 typ. 55

Ruggedness in class-B operation

The BLF548 is capable of withstanding a load mismatch corresponding to VSWR = 10 through all phases under the following conditions:

V_{DS} = 28 V; f = 500 MHz at rated output power.



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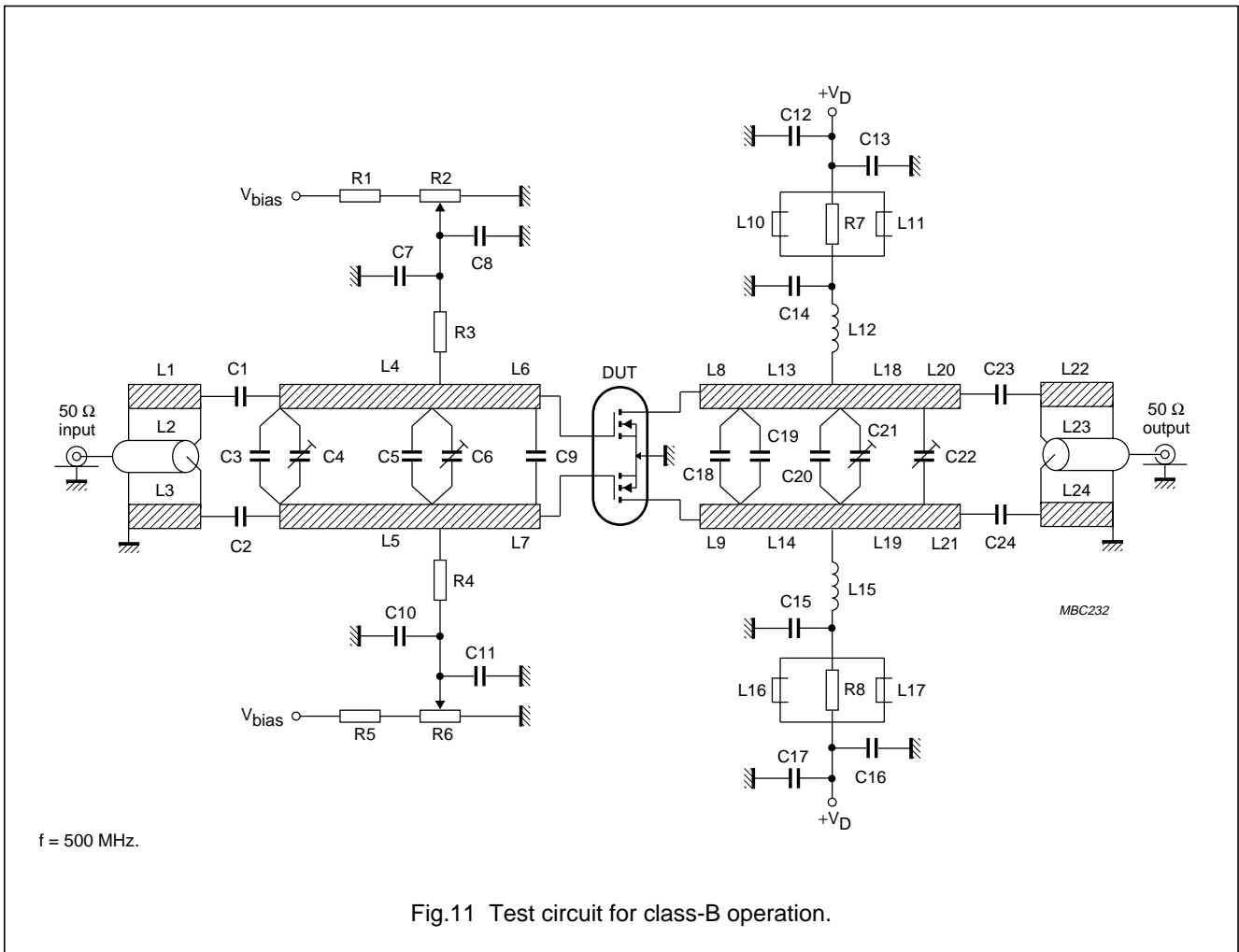


Fig.11 Test circuit for class-B operation.

List of components (see class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	22 pF		
C3	multilayer ceramic chip capacitor (note 1)	16 pF		
C4	film dielectric trimmer	2 to 9 pF		2222 809 09005
C5	multilayer ceramic chip capacitor (note 2)	27 pF		
C6, C21, C22	film dielectric trimmer	2 to 18 pF		2222 809 09006
C7, C10, C14, C15	multilayer ceramic chip capacitor (note 1)	390 pF		
C8, C11, C12, C17	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C9	multilayer ceramic chip capacitor (note 3)	2 × 56 pF in series		

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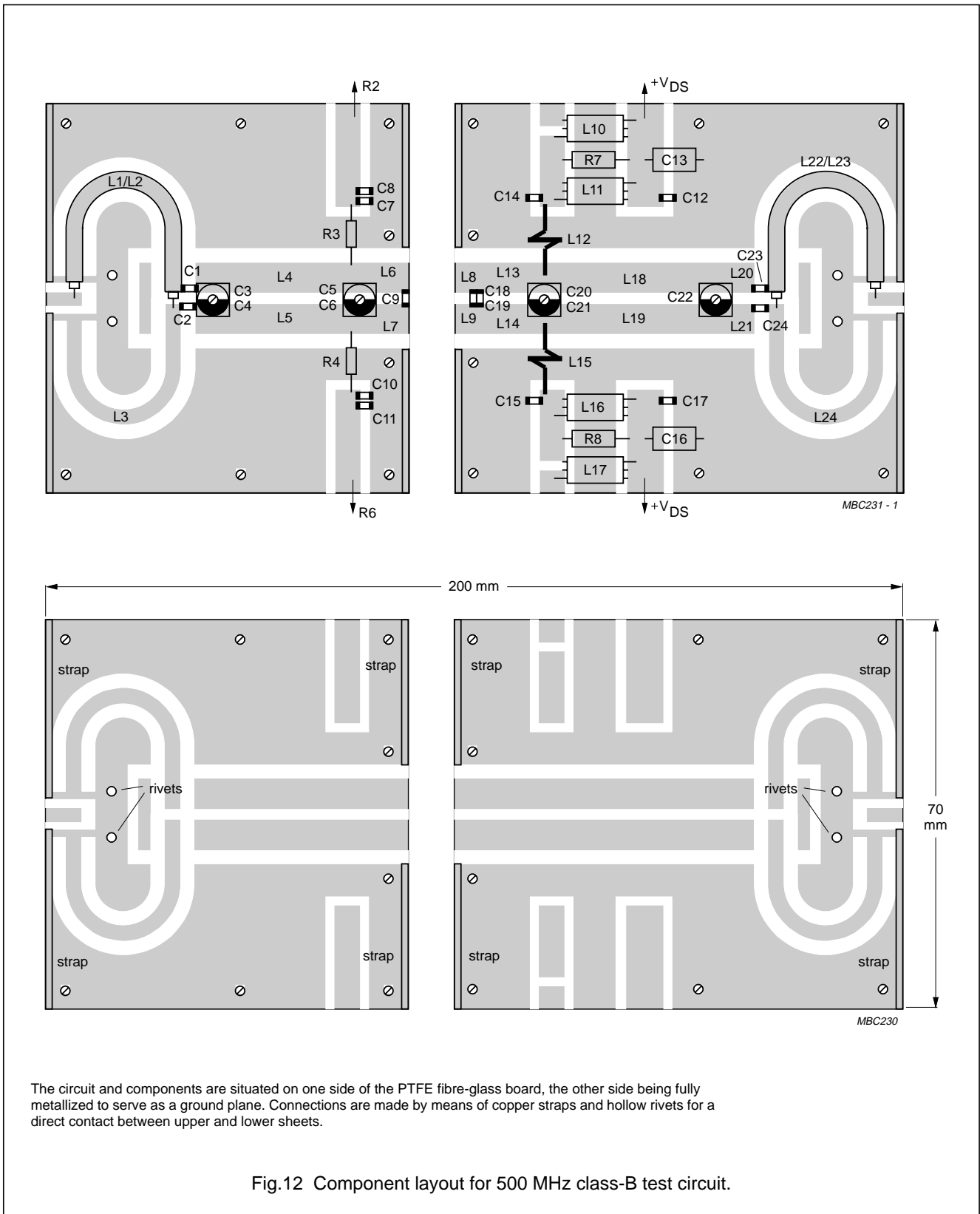
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C13, C16	electrolytic capacitor	10 μ F, 63 V		2222 030 38109
C18	multilayer ceramic chip capacitor (note 2)	18 pF		
C19	multilayer ceramic chip capacitor (note 2)	12 pF		
C20	multilayer ceramic chip capacitor (note 2)	8.2 pF		
C23, C24	multilayer ceramic chip capacitor (note 1)	30 pF		
L1, L3, L22, L24	stripline (note 4)	34.5 Ω	length 66.5 mm width 4 mm	
L2, L23	semi-rigid cable (note 5)	50 Ω	length 66.5 mm width 3.6 mm	
L4, L5	stripline (note 4)	22.3 Ω	length 35 mm width 7 mm	
L6, L7	stripline (note 4)	22.3 Ω	length 10 mm width 7 mm	
L8, L9	stripline (note 4)	22.3 Ω	length 5.5 mm width 7 mm	
L10, L11, L16, L17	grade 3B Ferroxcube wideband RF choke			4312 020 36642
L12, L15	1 turn enamelled 1.5 mm copper wire	17 nH	length 5 mm int. dia. 9 mm leads 2 \times 5 mm	
L13, L14	stripline (note 4)	22.3 Ω	length 15 mm width 7 mm	
L18, L19	stripline (note 4)	22.3 Ω	length 36 mm width 7 mm	
L20, L21	stripline (note 4)	22.3 Ω	length 8.5 mm width 7 mm	
R1, R5	0.4 W metal film resistor	24.7 k Ω		2322 151 72473
R2, R6	10 turn potentiometer	5 k Ω		
R3, R4	0.4 W metal film resistor	10.5 k Ω		2322 151 71053
R7, R8	1 W metal film resistor	10 Ω		2322 151 51009

Notes

- American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
- American Technical Ceramics (ATC) capacitor, type 175B or other capacitor of the same quality.
- American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
- The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric ($\epsilon_r = 2.2$), thickness 0.79 mm.
- Cables L2 and L23 are soldered to striplines L1 and L22 respectively.

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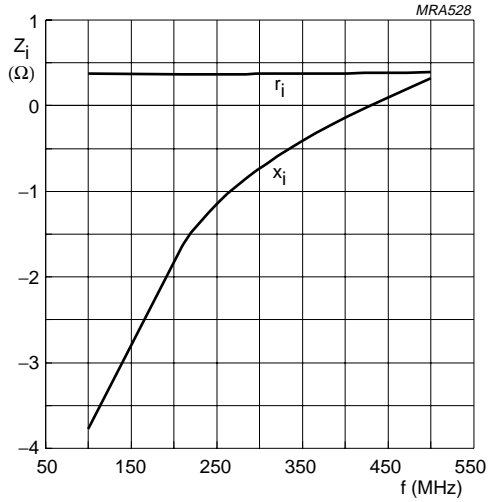


The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as a ground plane. Connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz class-B test circuit.

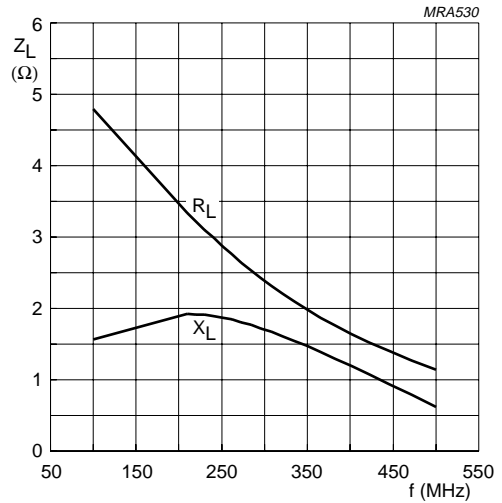
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Class-B operation; $V_{DS} = 28\text{ V}$; $I_{DQ} = 160\text{ mA}$ (per section); $P_L = 150\text{ W}$ (total device).

Fig. 13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; $V_{DS} = 28\text{ V}$; $I_{DQ} = 160\text{ mA}$ (per section); $P_L = 150\text{ W}$ (total device).

Fig. 14 Load impedance as a function of frequency (series components), typical values per section.

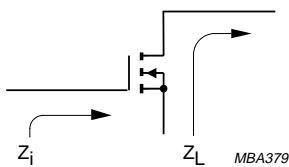
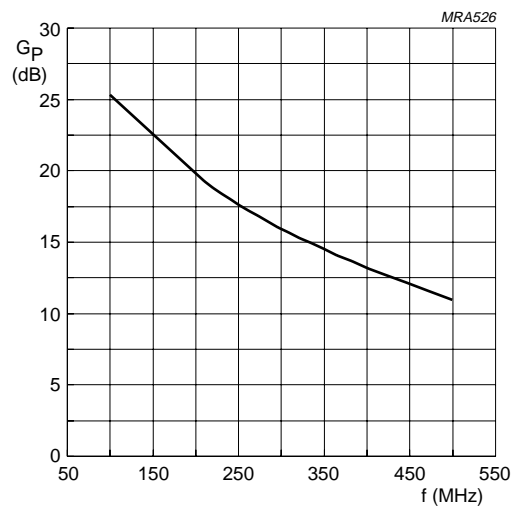


Fig. 15 Definition of MOS impedance.



Class-B operation; $V_{DS} = 28\text{ V}$; $I_{DQ} = 160\text{ mA}$ (per section); $P_L = 150\text{ W}$ (total device).

Fig. 16 Power gain as a function of frequency, typical values per section.

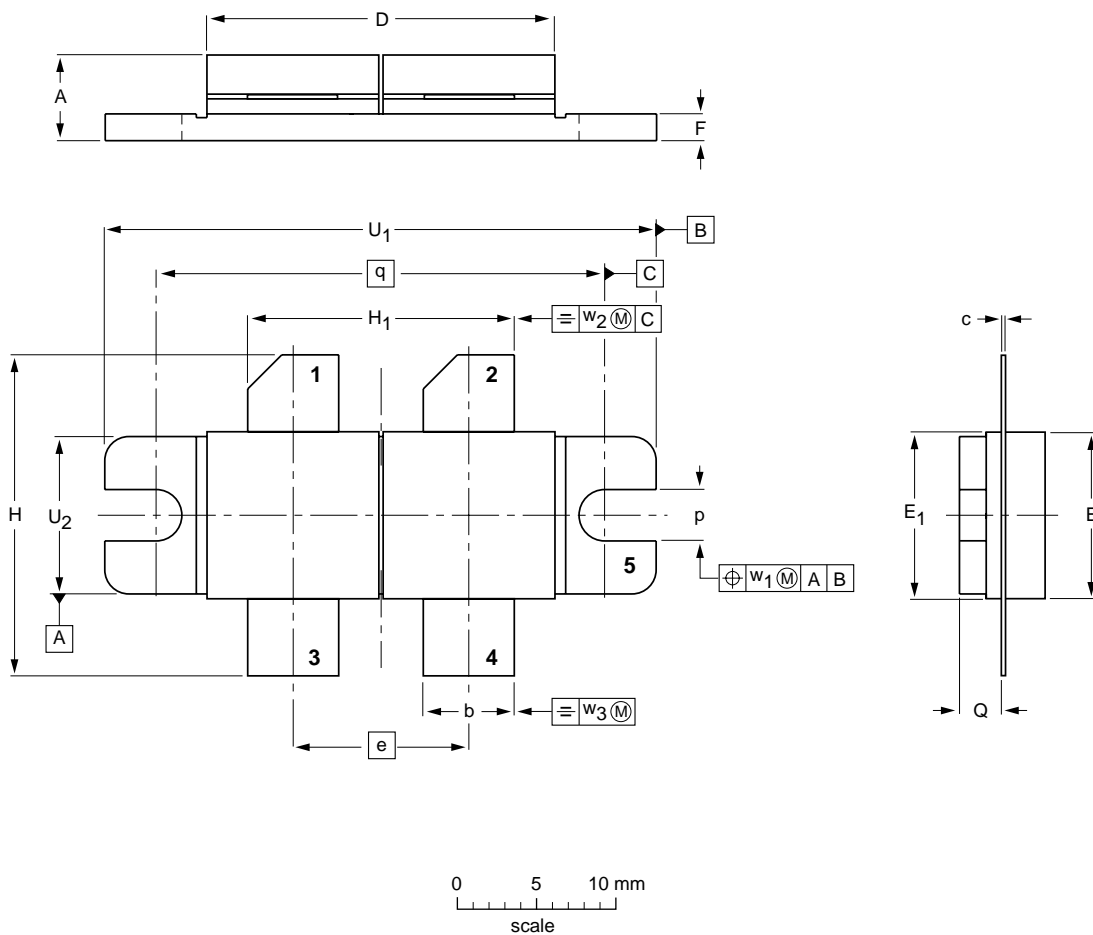
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PACKAGE OUTLINE

Flanged double-ended ceramic package; 2 mounting holes; 4 leads

SOT262A2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	e	E	E ₁	F	H	H ₁	p	Q	q	U ₁	U ₂	w ₁	w ₂	w ₃
mm	5.39 4.62	5.85 5.58	0.16 0.10	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	20.58 20.06	17.02 16.51	3.28 3.02	2.47 2.20	27.94	34.17 33.90	9.91 9.65	0.51	1.02	0.25
inches	0.212 0.182	0.230 0.220	0.006 0.004	0.865 0.855	0.435	0.404 0.395	0.405 0.396	0.070 0.060	0.81 0.79	0.67 0.65	0.129 0.119	0.097 0.087	1.100	1.345 1.335	0.390 0.380	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262A2						97-06-28

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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