

DATA SHEET

BLV194 UHF power transistor

Product specification

January 1993

UHF power transistor

BLV194

FEATURES

- Emitter-ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

DESCRIPTION

NPN silicon planar epitaxial transistor intended for common emitter class-AB operation in the 900 MHz communications band.

The transistor has a SOT171 flange envelope with a ceramic cap.

All leads are isolated from the mounting base.

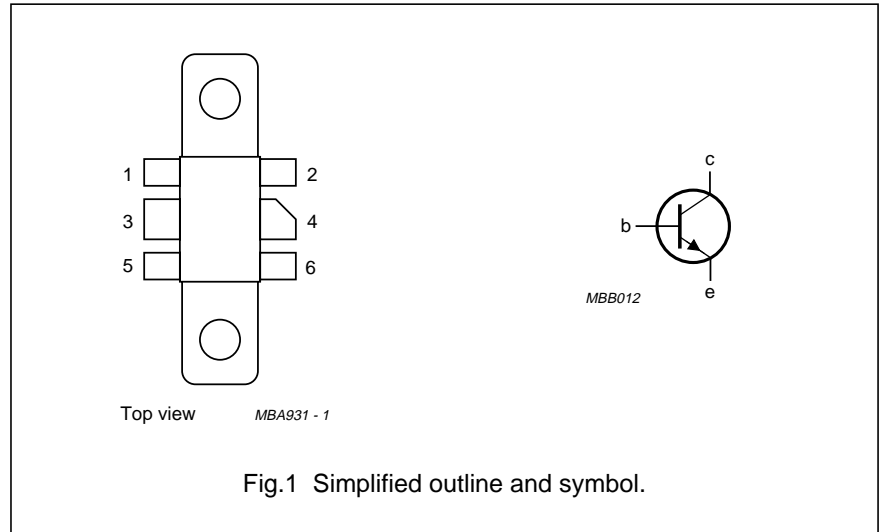
PINNING - SOT171

PIN	DESCRIPTION
1	emitter
2	emitter
3	base
4	collector
5	emitter
6	emitter

QUICK REFERENCE DATA

RF performance at $T_h = 25\text{ }^\circ\text{C}$ in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_c (%)
CW, class-AB	900	12.5	16	≥ 7	≥ 50



WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

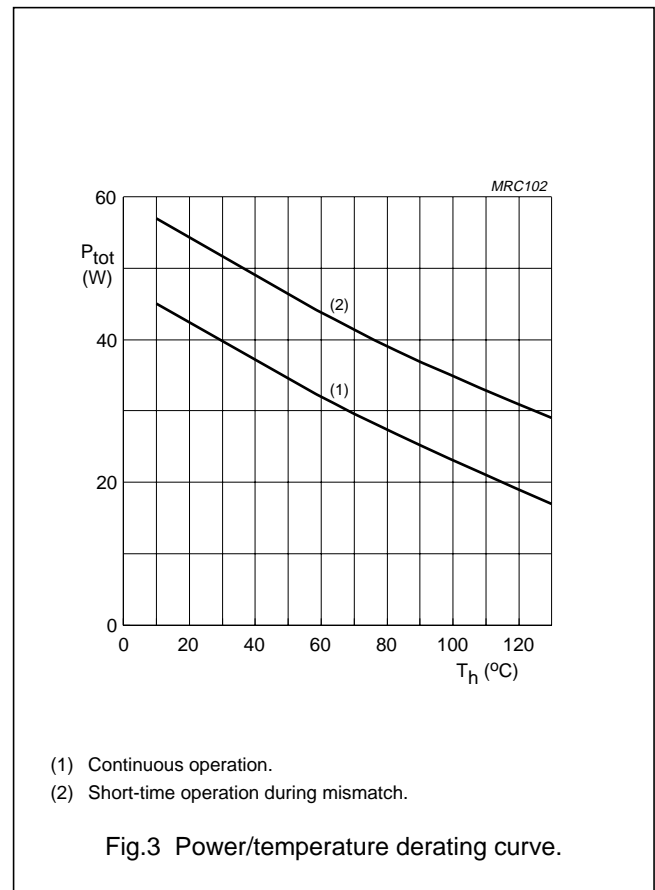
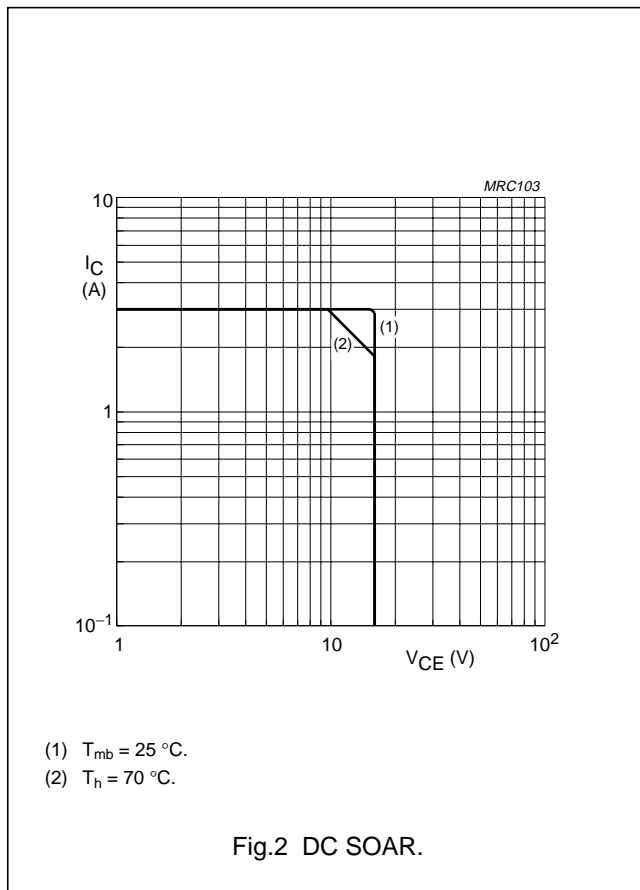
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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CEO}	collector-emitter voltage	open base	–	16	V
V_{CES}	collector-emitter voltage	base short-circuited	–	32	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	DC collector current		–	3	A
$I_{C(AV)}$	average collector current		–	3	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	–	46	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C



THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	$P_{dis} = 46\text{ W}; T_{mb} = 25\text{ °C}$	3.8 K/W
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink		0.4 K/W

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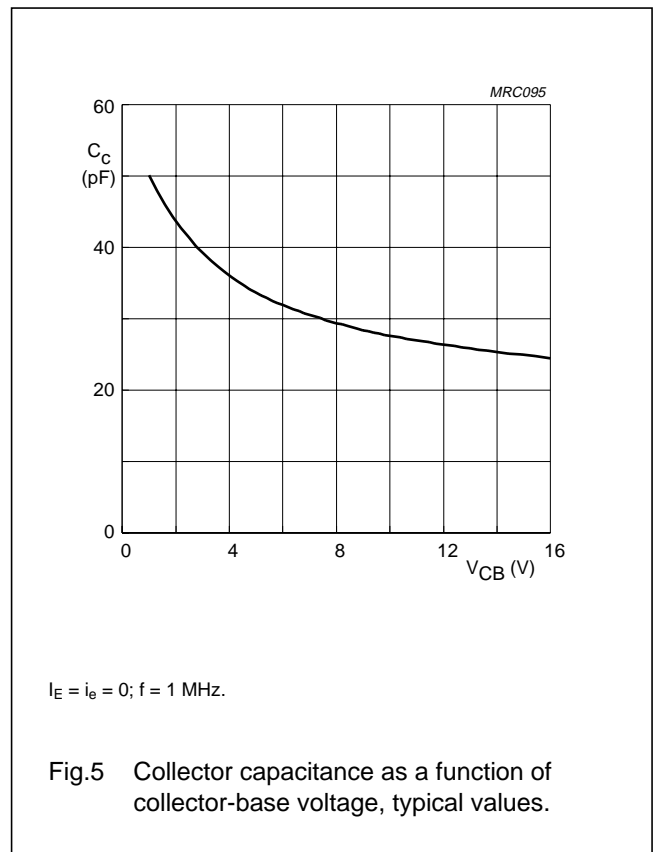
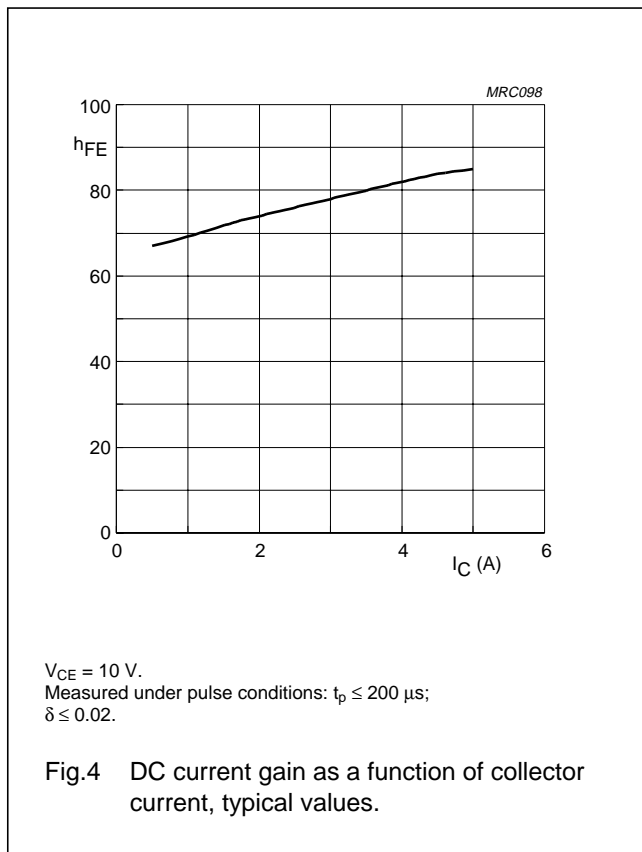
CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_B = 0; I_C = 40\text{ mA}$	16	–	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	$I_C = 20\text{ mA}; V_{BE} = 0$	32	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	$I_C = 0; I_E = 5\text{ mA}$	3	–	–	V
I_{CER}	collector leakage current	$R_{BE} = 700\ \Omega; V_{CE} = 16\text{ V}$	–	–	1	mA
h_{FE}	DC current gain	$I_C = 1.2\text{ A}; V_{CE} = 10\text{ V}$ (note 1)	25	70	–	
C_c	collector capacitance	$I_E = i_e = 0; V_{CB} = 12.5\text{ V}; f = 1\text{ MHz}$	–	26	–	pF
C_{re}	feedback capacitance	$I_C = 0; V_{CB} = 12.5\text{ V}; f = 1\text{ MHz}$	–	19	–	pF
C_{c-mb}	collector-mounting base capacitance		–	2	–	pF

Note

1. Measured under pulse conditions: $t_p \leq 200\ \mu\text{s}; \delta \leq 0.02$.



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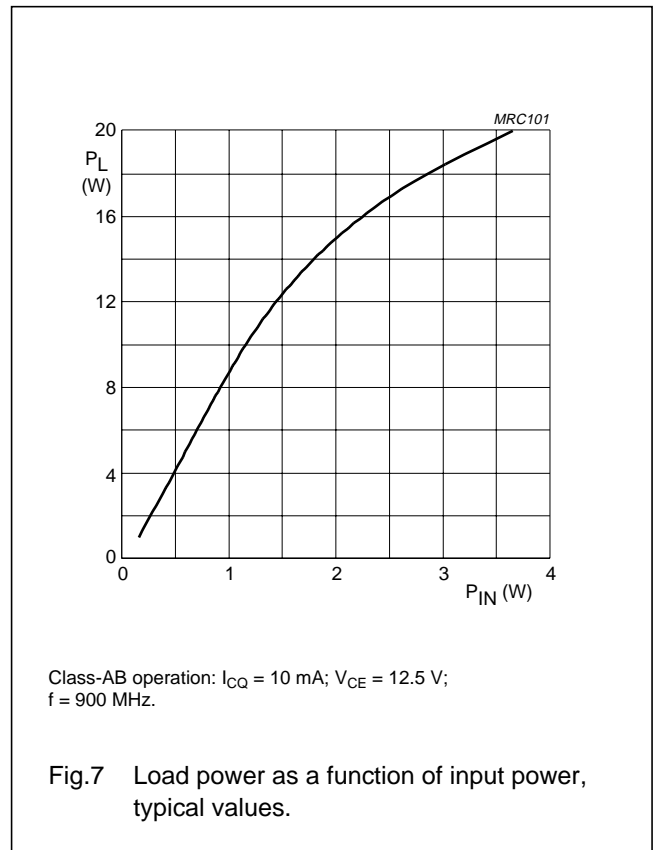
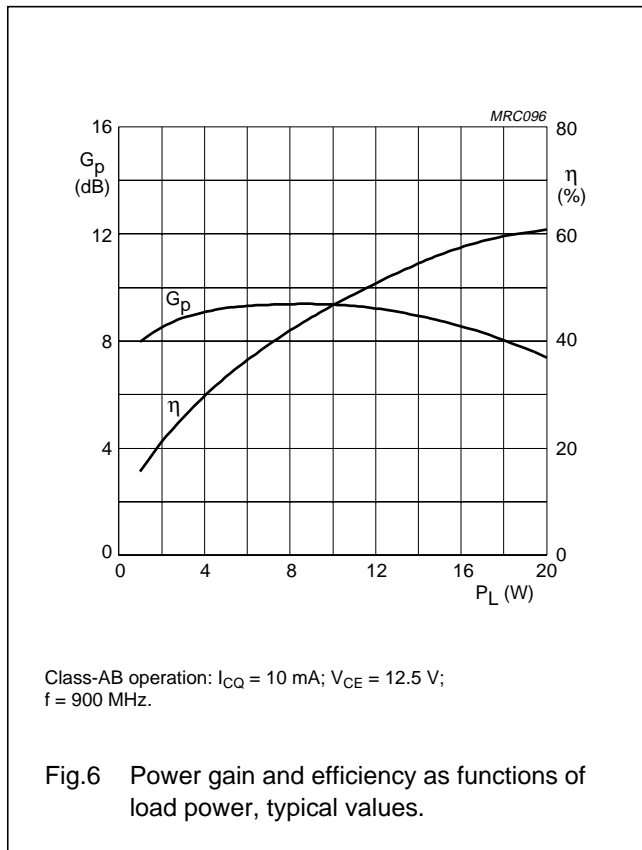
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APPLICATION INFORMATION

RF performance at $T_h = 25\text{ }^\circ\text{C}$ in a common emitter test circuit.

$R_{th\ j-mb} = 0.4\text{ K/W}$.

MODE OF OPERATION	f (MHz)	V _{CE} (V)	I _{CQ} (mA)	P _L (W)	G _p (dB)	η_c (%)
CW, class-AB	900	12.5	10	16	≥ 7 typ. 8.5	≥ 50 typ. 57



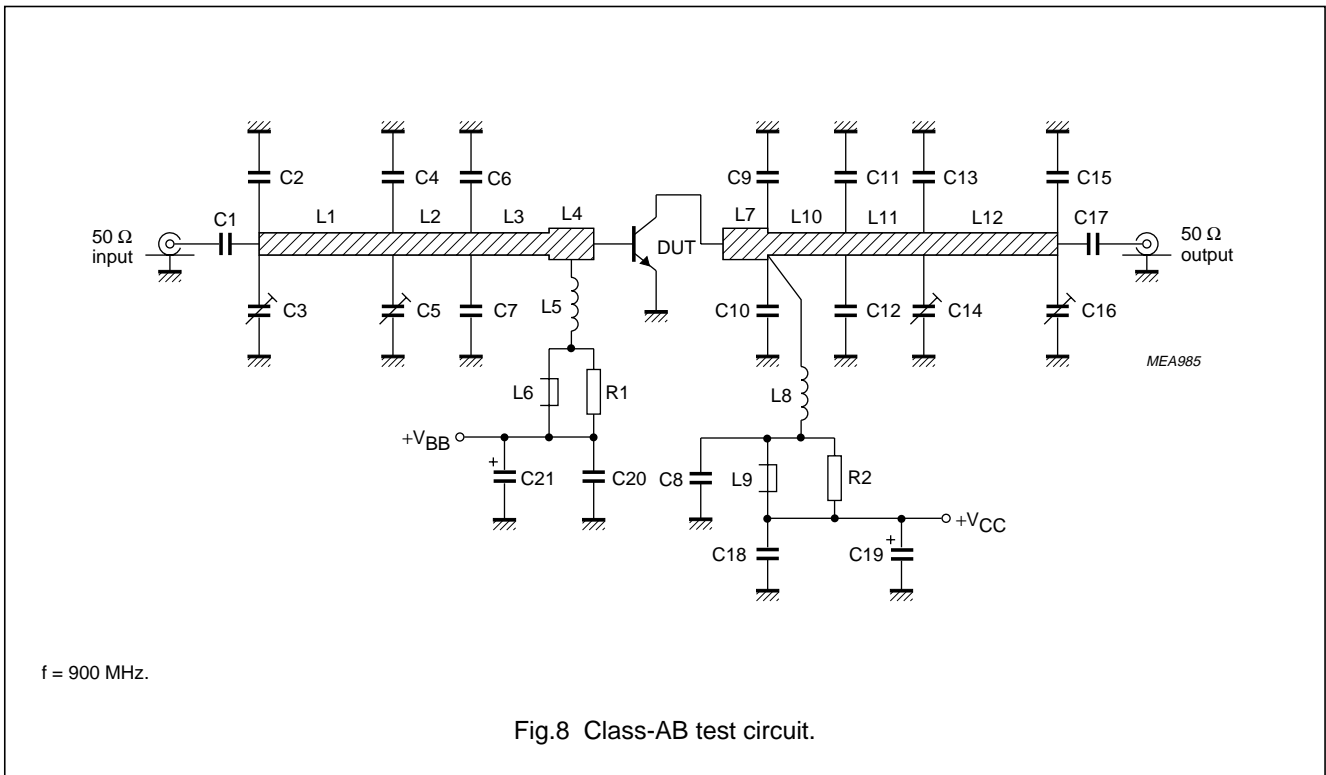
Ruggedness in class-AB operation

The BLV194 is capable of withstanding a load mismatch corresponding to $VSWR = 20:1$ through all phases at rated output power under the following conditions:

$V_{CE} = 15.5\text{ V}$; $T_h = 25\text{ }^\circ\text{C}$; $R_{th\ j-mb} = 0.4\text{ K/W}$; $f = 900\text{ MHz}$.

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List of components (see test circuit)

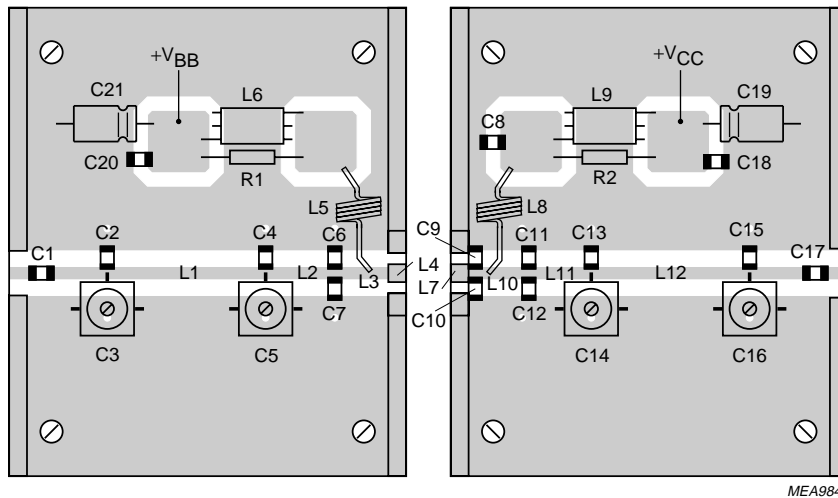
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C8, C17	multilayer ceramic chip capacitor (note 1)	330 pF		
C3, C5, C14, C16	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
C2, C6, C7	multilayer ceramic chip capacitor (note 1)	4.3 pF		
C4	multilayer ceramic chip capacitor (note 1)	3.9 pF		
C13, C15	multilayer ceramic chip capacitor (note 1)	4.7 pF		
C9, C10	multilayer ceramic chip capacitor (note 3)	5.6 pF		
C11, C12	multilayer ceramic chip capacitor (note 1)	5.6 pF		
C18	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C19, C21	electrolytic capacitor	10 μ F, 63 V		2222 030 37688
L1, L12	stripline (note 3)	50 Ω	length 24 mm width 2.4 mm	
L2, L11	stripline (note 3)	50 Ω	length 10 mm width 2.4 mm	
L3	stripline (note 3)	50 Ω	length 8 mm width 2.4 mm	
L4, L7	stripline (note 3)	41 Ω	length 3 mm width 3.2 mm	
L5, L8	4 turns enamelled 1 mm copper wire	45 nH	int. dia. 4 mm leads 2 \times 5 mm	
L6, L9	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L10	stripline (note 3)	50 Ω	length 7 mm width 2.4 mm	
R1, R2	0.25 W metal film resistor	10 Ω		

Notes

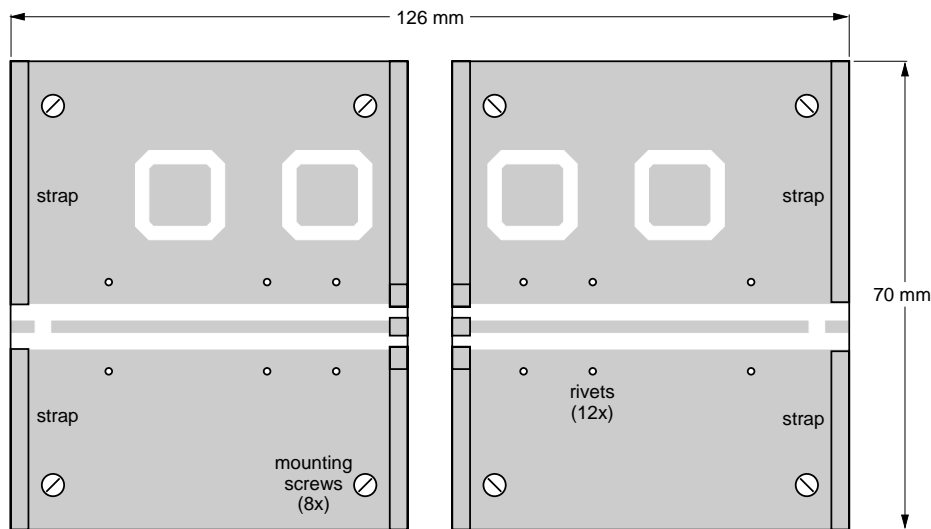
- American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
- American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
- The striplines are on a double copper-clad printed- circuit board, with PTFE fibre-glass dielectric ($\epsilon_r = 2.2$), thickness $\frac{1}{32}$ inch.

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MEA984



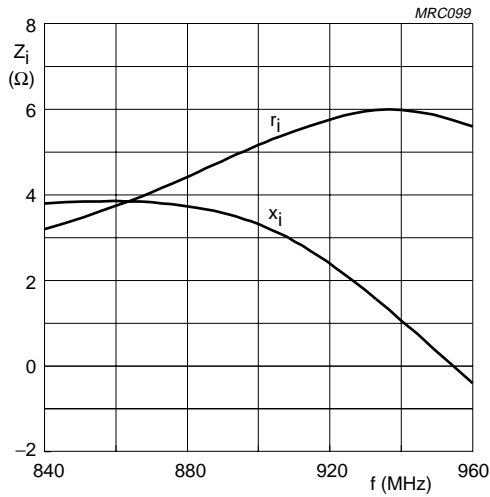
MEA983

The components are mounted on one side of a copper-clad PTFE fibre-glass board; the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by fixing screws and copper straps under the emitter leads.

Fig.9 Component layout for 900 MHz class-AB test circuit.

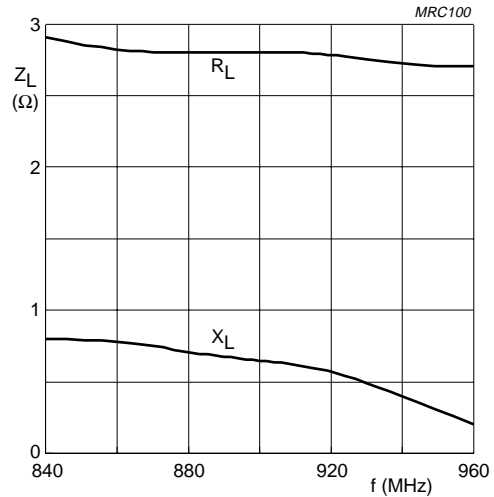
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Class-AB operation: $I_{CQ} = 10 \text{ mA}$; $V_{CE} = 12.5 \text{ V}$;
 $T_h = 25 \text{ }^\circ\text{C}$; $P_L = 16 \text{ W}$.

Fig.10 Input impedance as a function of frequency (series components), typical values.



Class-AB operation: $I_{CQ} = 10 \text{ mA}$; $V_{CE} = 12.5 \text{ V}$;
 $T_h = 25 \text{ }^\circ\text{C}$; $P_L = 16 \text{ W}$.

Fig.11 Load impedance as a function of frequency (series components), typical values.

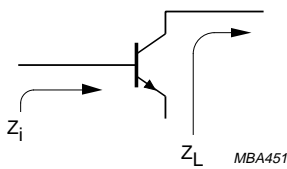
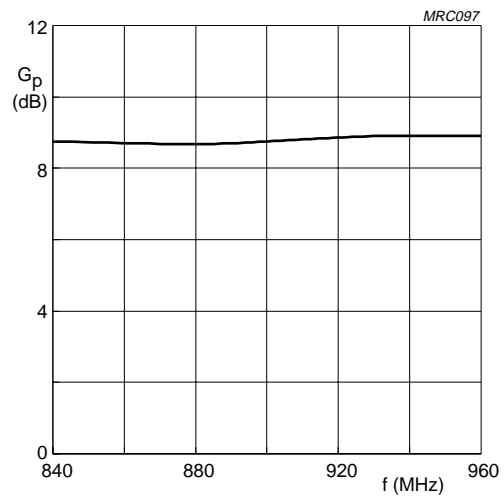


Fig.12 Definition of transistor impedance.



Class-AB operation: $I_{CQ} = 10 \text{ mA}$; $V_{CE} = 12.5 \text{ V}$;
 $T_h = 25 \text{ }^\circ\text{C}$; $P_L = 16 \text{ W}$.

Fig.13 Power gain as a function of frequency, typical values.

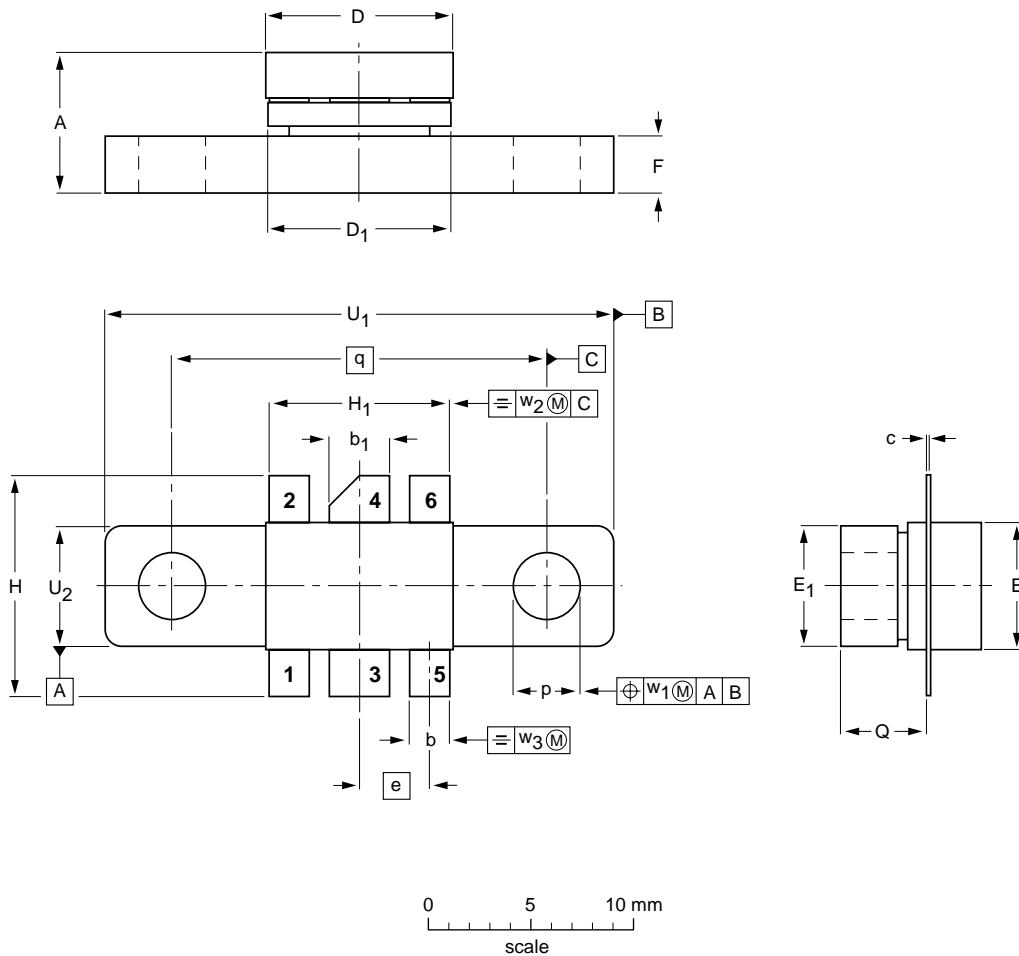
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PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 6 leads

SOT171A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b ₁	c	D	D ₁	E	E ₁	e	F	H	H ₁	p	Q	q	U ₁	U ₂	w ₁	w ₂	w ₃
mm	6.81 6.07	2.15 1.85	3.20 2.89	0.16 0.07	9.25 9.04	9.30 8.99	5.95 5.74	6.00 5.70	3.58	3.05 2.54	11.31 10.54	9.27 9.01	3.43 3.17	4.32 4.11	18.42	24.90 24.63	6.00 5.70	0.51	1.02	0.26
inches	0.268 0.239	0.085 0.073	0.126 0.114	0.006 0.003	0.364 0.356	0.366 0.354	0.234 0.226	0.236 0.224	0.140	0.120 0.100	0.445 0.415	0.365 0.355	0.135 0.125	0.170 0.162	0.725	0.980 0.970	0.236 0.224	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT171A					97-06-28

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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