

DATA SHEET

BLV859

**UHF linear push-pull power
transistor**

Product specification
Supersedes data of 1995 Oct 04

1996 Jul 26

UHF linear push-pull power transistor

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FEATURES

- Double internal input and output matching for an optimum wideband capability and high gain
- Polysilicon emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATION

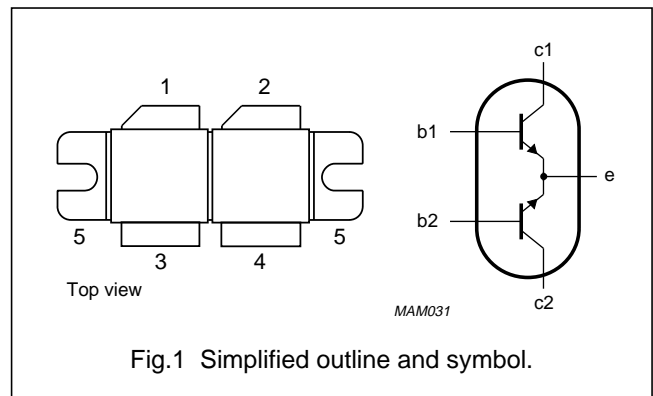
- Common emitter class-A operation in linear transposers/transmitters (television) in the 470 to 860 MHz frequency band.

DESCRIPTION

NPN silicon planar transistor with two sections in push-pull configuration. The device is encapsulated in a SOT262B 4-lead rectangular flange package, with two ceramic caps. It delivers a $P_{o\ sync} = 20\text{ W}$ in class-A operation at 860 MHz and a supply voltage of 25 V.

PINNING SOT262B

PIN	SYMBOL	DESCRIPTION
1	c1	collector 1
2	c2	collector 2
3	b1	base 1
4	b2	base 2
5	e	emitter



QUICK REFERENCE DATA

RF performance at $T_h = 25\text{ °C}$ in a common emitter push-pull test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{o\ sync}$ (W)	G_p (dB)
CW class-A	860	25	2×2.25	$\geq 20^{(1)}$	$\geq 10^{(1)}$

Note

1. Three-tone test signal (-8, -16 and -10 dB); $d_{im} = -54\text{ dB}$.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

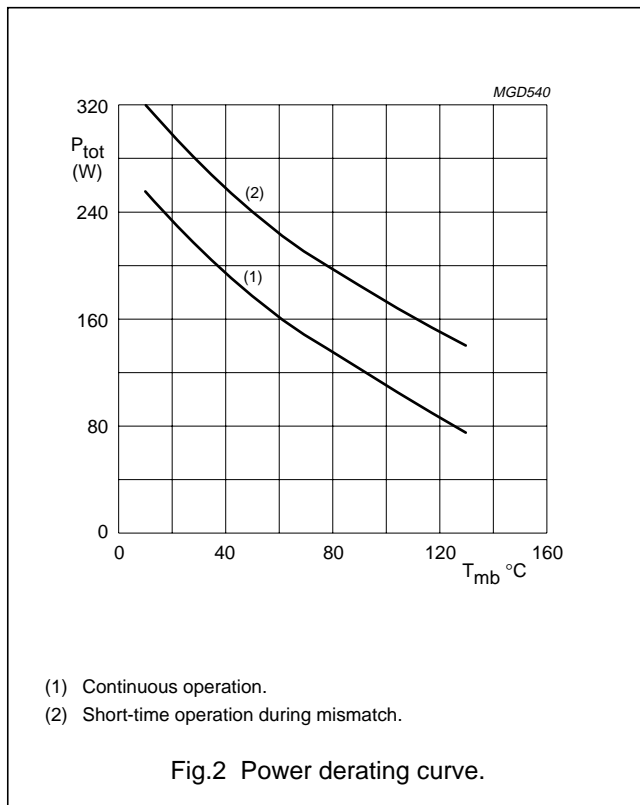
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	28	V
V_{EBO}	emitter-base voltage	open collector	–	2.5	V
I_C	collector current (DC)		–	15	A
$I_{C(AV)}$	average collector current		–	15	A
P_{tot}	total power dissipation	$T_{mb} = 70\text{ °C}$; note 1	–	145	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-mb}$	thermal resistance from junction to mounting-base	$P_{tot} = 145\text{ W}$; $T_{mb} = 70\text{ °C}$ note 1	0.9	K/W
$R_{th\ mb-h}$	thermal resistance from mounting-base to heatsink	note 1	0.15	K/W

Note to Limiting values and Thermal characteristics

1. Total device; both sections equally loaded.



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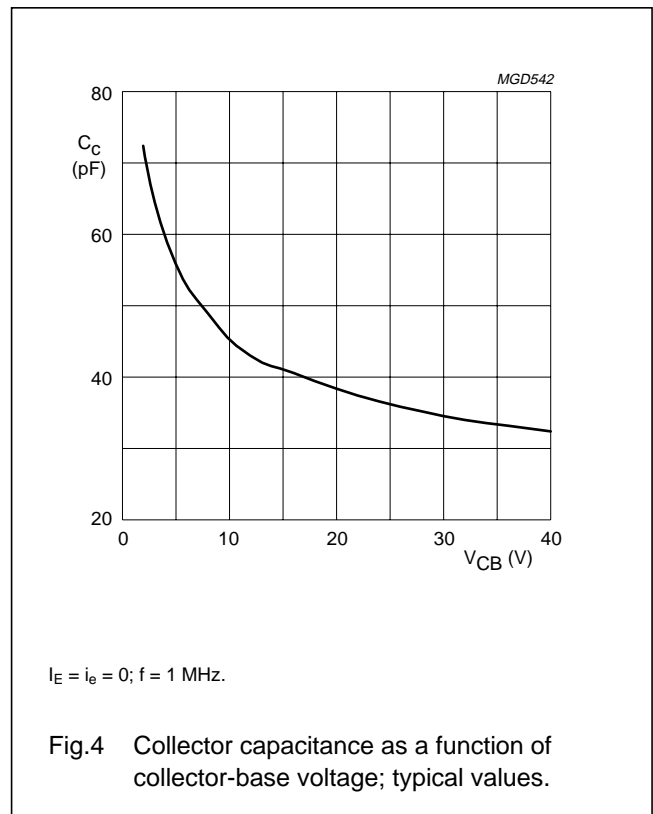
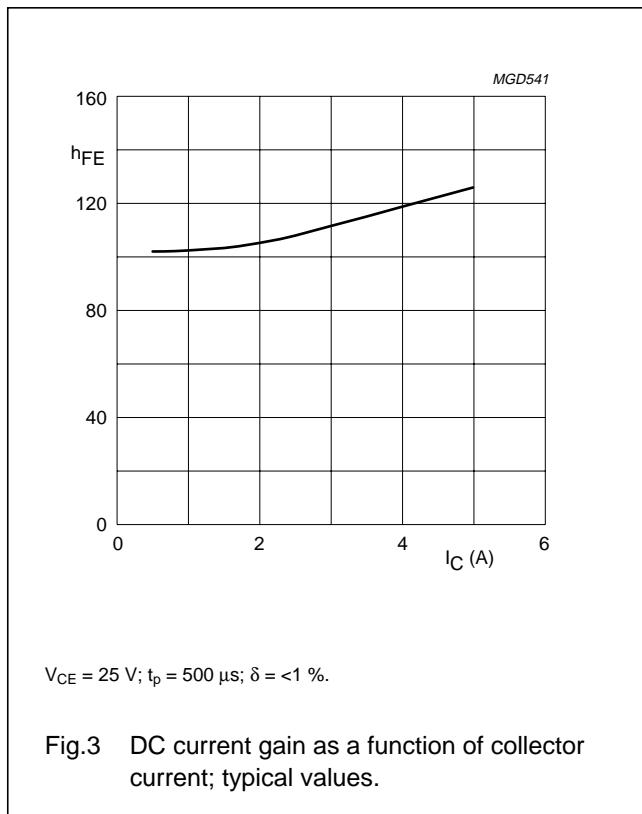
CHARACTERISTICS

Values apply to either transistor section; $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 30\text{ mA}; I_E = 0$	60	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 60\text{ mA}; I_B = 0$	28	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	$I_E = 1.2\text{ mA}; I_C = 0$	2.5	–	–	V
I_{CBO}	collector-base leakage current	$V_{CB} = 27\text{ V}; V_{BE} = 0$	–	–	3	mA
I_{CEO}	collector-emitter leakage current	$V_{CE} = 20\text{ V}$	–	–	6	mA
h_{FE}	DC current gain	$V_{CE} = 25\text{ V}; I_C = 2.25\text{ A}$	30	–	140	
C_c	collector capacitance	$V_{CB} = 25\text{ V}; I_E = i_e = 0;$ $f = 1\text{ MHz}$	–	36 ⁽¹⁾	–	pF
C_{re}	feedback capacitance	$V_{CE} = 25\text{ V}; I_B = 0; f = 1\text{ MHz}$	–	22	–	pF

Note

1. The value of C_c is that of the die only; it is not measurable, because of the internal matching network.



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APPLICATION INFORMATION

RF performance at $T_h = 25\text{ °C}$ in a common emitter push-pull class-A test circuit.

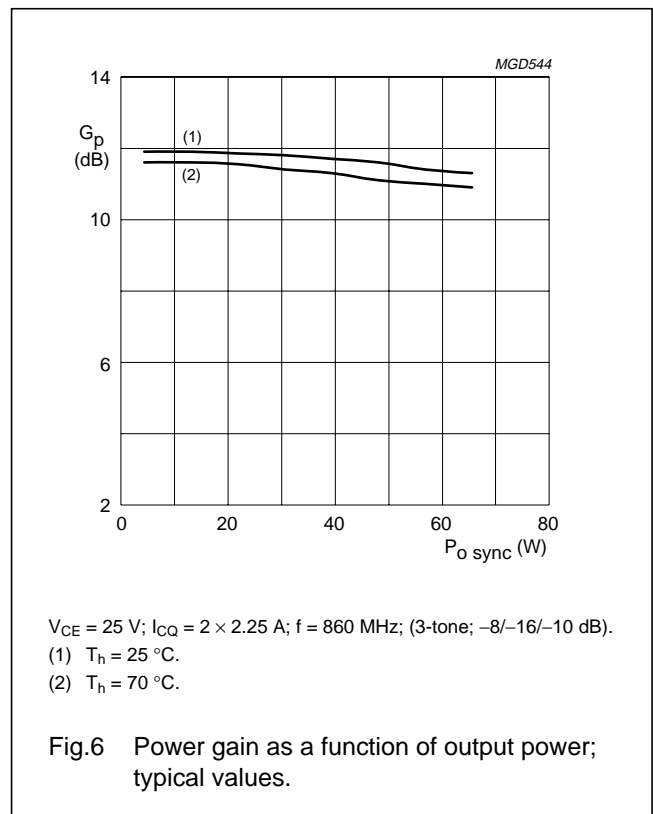
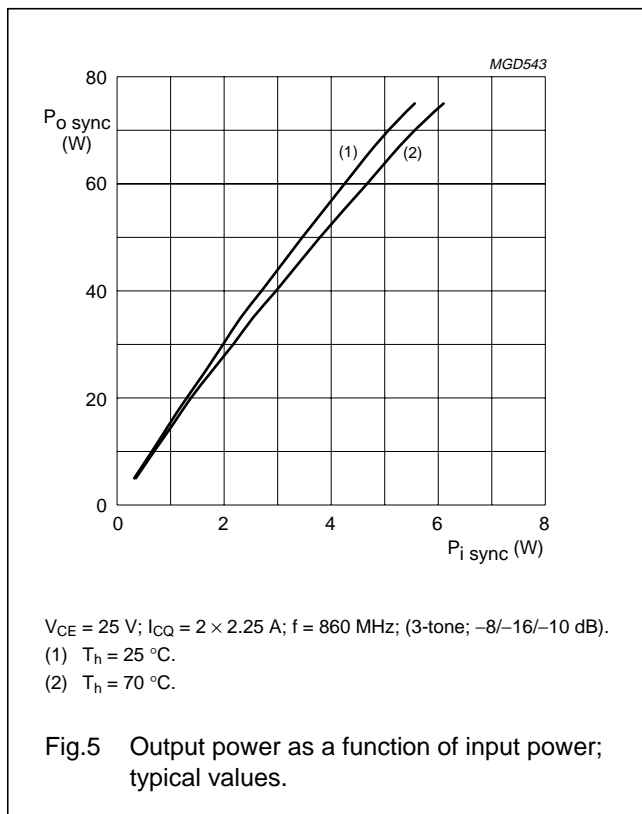
MODE OF OPERATION	f (MHz)	V _{CE} (V)	I _{CQ} (A)	P _{o sync} (W)	G _p (dB)	d _{im} (dB)
CW class-A	860	25	2 × 2.25	≥20 ⁽¹⁾	≥10 ⁽¹⁾	≤-54 ⁽¹⁾
CW class-A	860	25	2 × 2.25	≥20 ⁽²⁾	≥10 ⁽²⁾	≤-51 ⁽²⁾

Notes

- Three-tone test method (vision carrier -8 dB, sound carrier -10 dB, sideband signal -16 dB), 0 dB corresponds to peak sync level.
- Three-tone test method (vision carrier -8 dB, sound carrier -7 dB, sideband signal -16 dB), 0 dB corresponds to peak sync level.

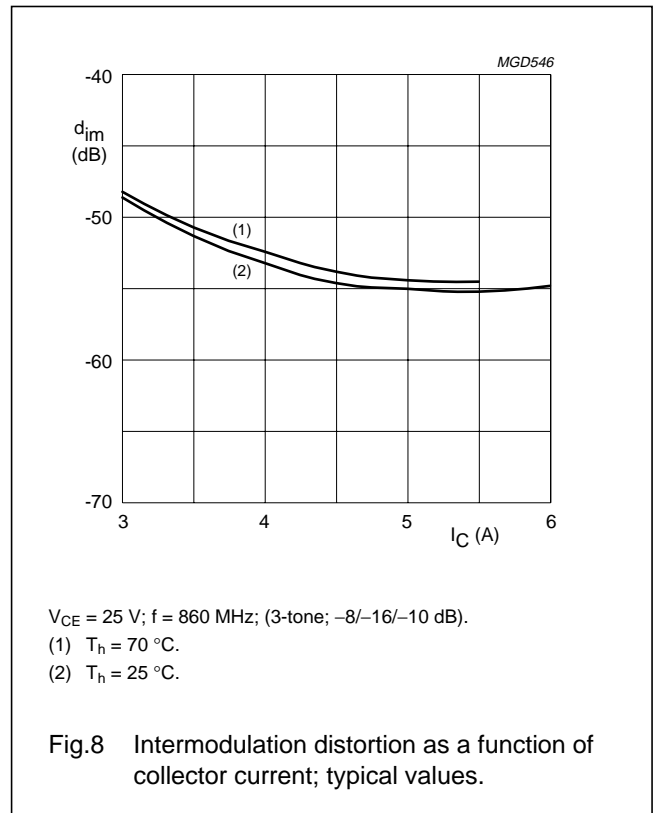
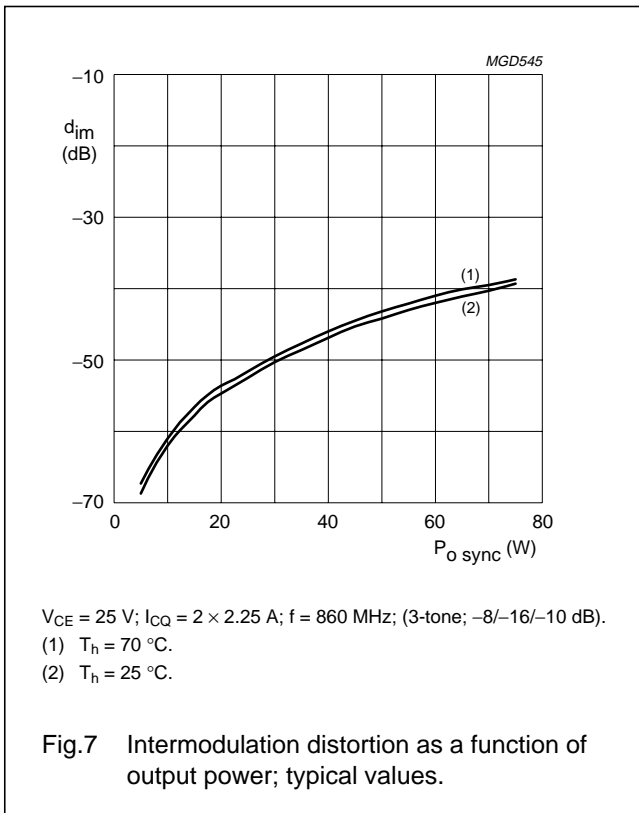
Ruggedness in class-A operation

The BLV859 is capable of withstanding a load mismatch corresponding to VSWR = 50 : 1 through all phases under the conditions: V_{CE} = 25 V; I_{CQ} = 2 × 2.25 A; f = 860 MHz; T_h = 25 °C; P_{o sync} = 20 W.



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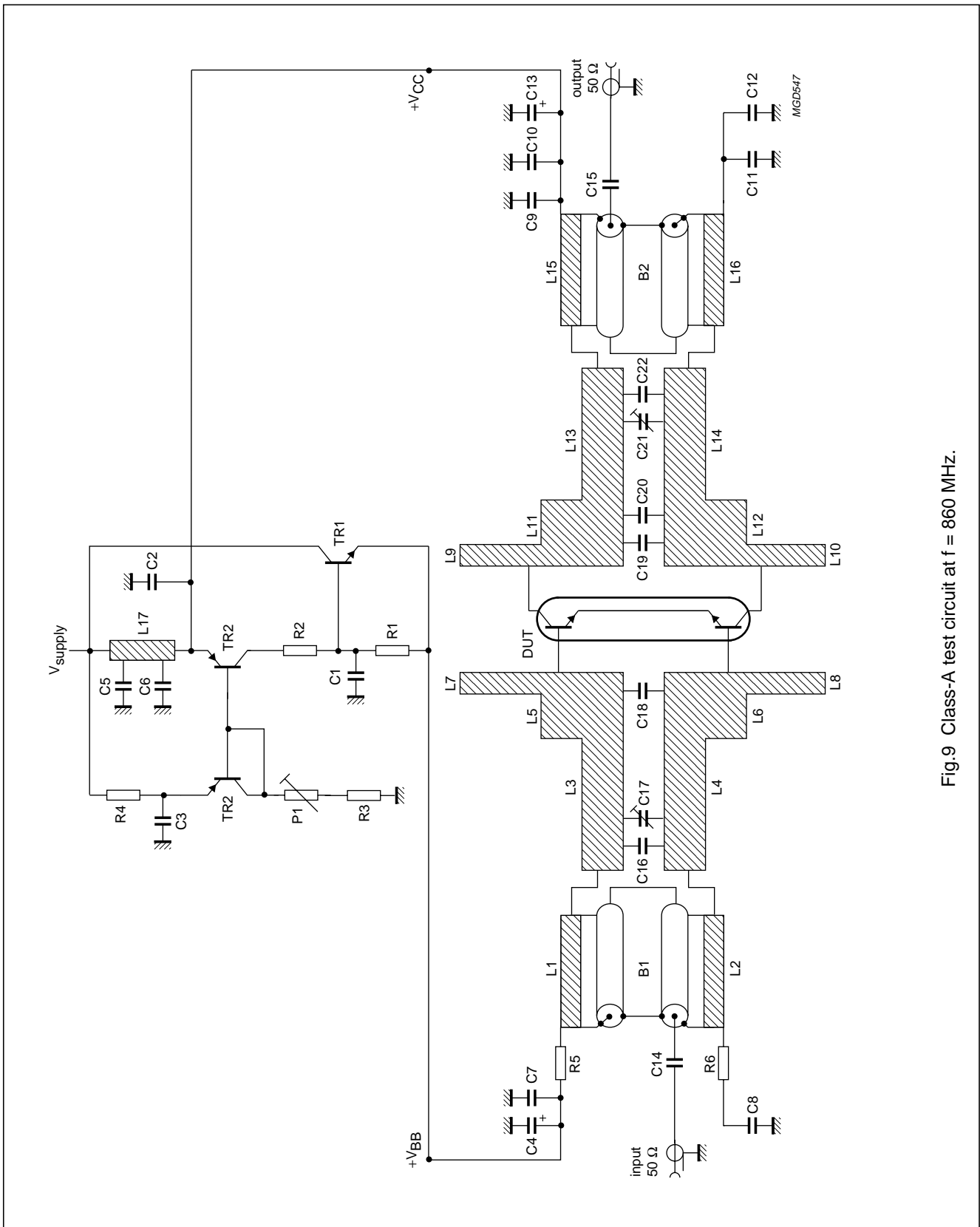
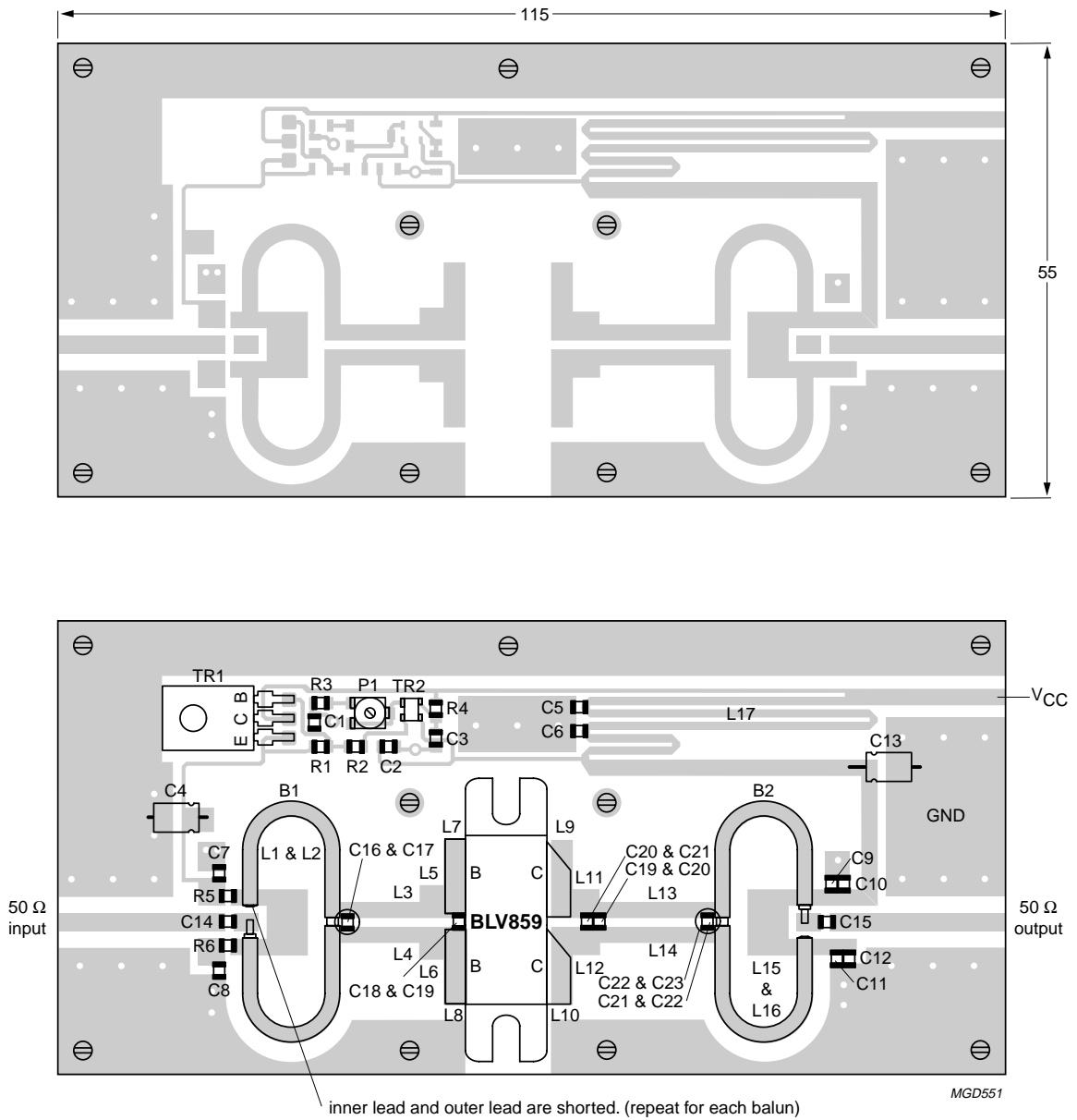


Fig.9 Class-A test circuit at f = 860 MHz.

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Dimensions in mm.

Fig.10 Printed-circuit board and component lay-out for 860 MHz class-A test circuit.

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List of components

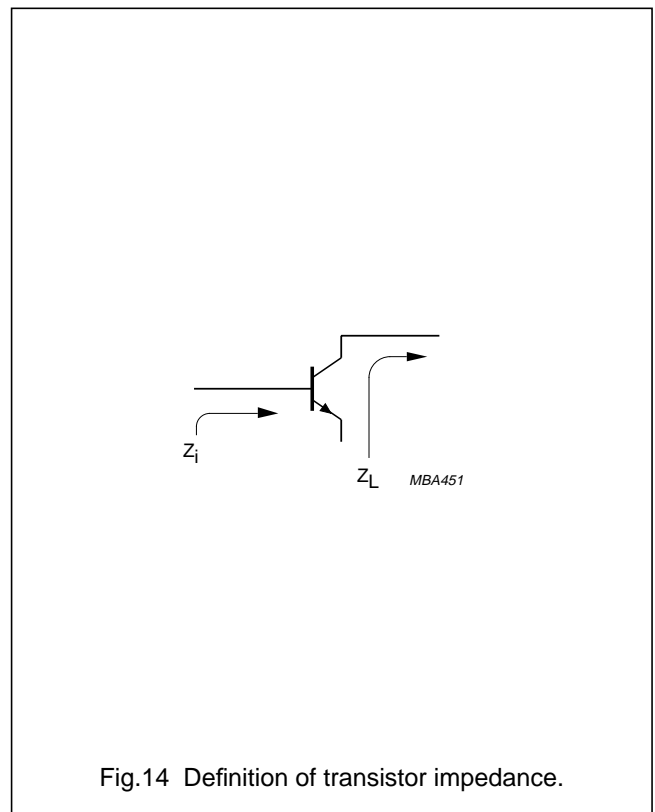
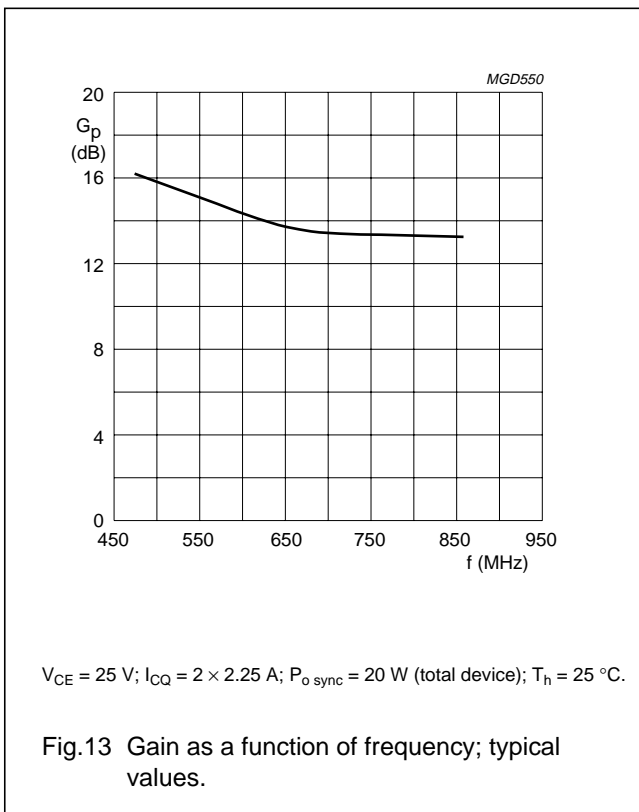
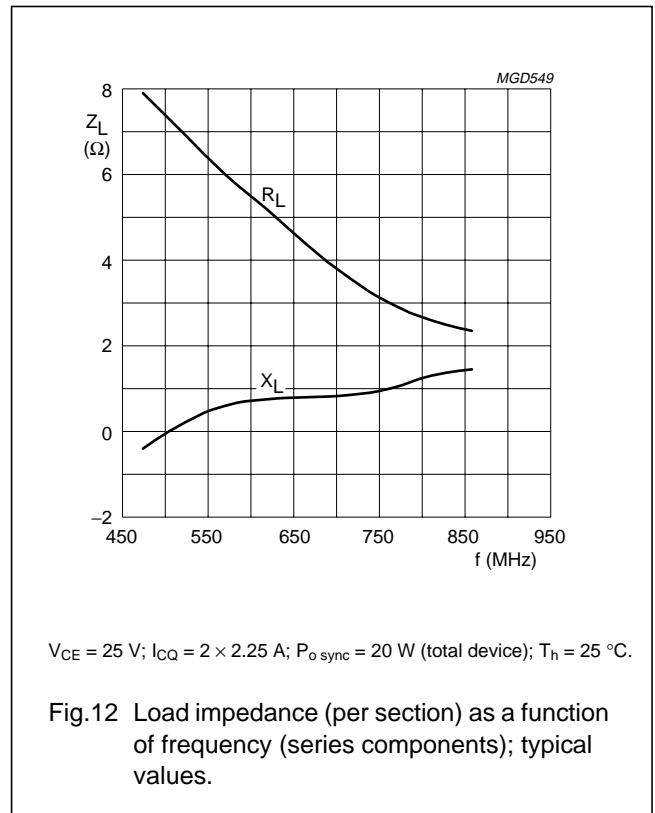
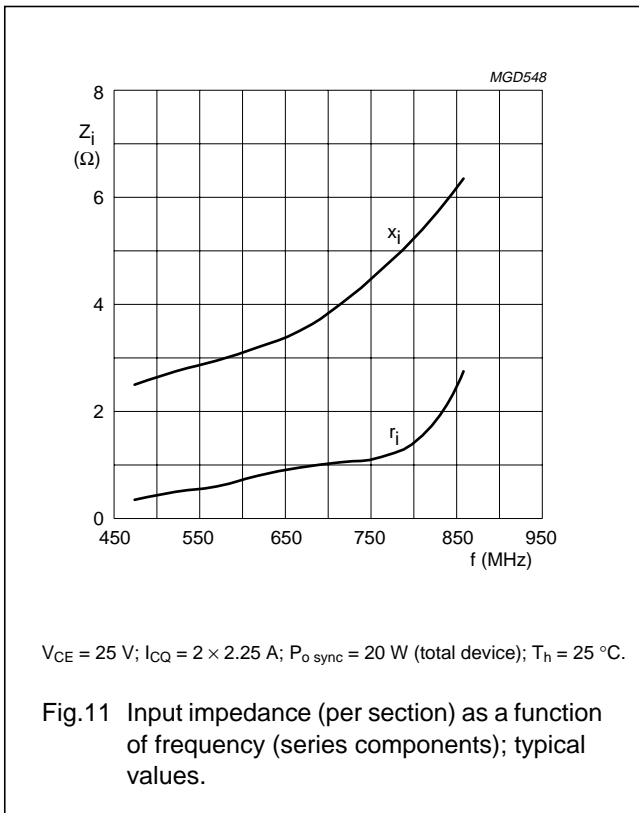
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2, C3, C5, C6	multilayer ceramic chip capacitor;	15 nF	805	2222 590 16629
C4	solid aluminium capacitor	47 μ F; 25 V		2222 030 36479
C7, C8	multilayer ceramic chip capacitor	10 nF	805	2222 590 16627
C9, C10, C11, C12	multilayer ceramic chip capacitor	100 nF	1206	2222 591 16641
C13	solid aluminium capacitor	10 μ F; 63 V		2222 030 381109
C14, C15	multilayer ceramic chip capacitor; note 1	47 pF		
C16	multilayer ceramic chip capacitor; note 1	8.2 pF		
C17, C21	Tekelec Giga trim 37271	0.6 to 4.5 pF		
C18	multilayer ceramic chip capacitor; note 1	13 pF		
C19	multilayer ceramic chip capacitor; note 1	3.9 pF		
C20	multilayer ceramic chip capacitor; note 1	12 pF		
C22	multilayer ceramic chip capacitor; note 1	9.1 pF		
L1, L2, L15, L16	stripline; note 2	50 Ω	2 \times 30.6 mm	
L3, L4	stripline; note 2	50 Ω	2 \times 9.5 mm	
L5, L6	stripline; note 2	32.4 Ω	4 \times 3 mm	
L7, L8, L9, L10	stripline; note 2	16.2 Ω	9.5 \times 2.6 mm	
L11, L12	stripline; note 2	37.5 Ω	3.5 \times 3.4 mm	
L13, L14	stripline; note 2	50 Ω	2 \times 13.9 mm	
L17	stripline; note 2	77.7 Ω	1 \times 120 mm	
B1, B2	Semi rigid coax balun UT70-25	Z = 25 Ω , \pm 1.5 Ω	70 mm	
R1	SMD resistor	220 Ω	805	2322 734 22201
R2	SMD resistor	1.8 Ω	805	2322 734 21808
R3	SMD resistor	2.7 k Ω	805	2322 734 22702
R4	SMD resistor	33 Ω	805	2322 734 23309
R7, R8	SMD resistor	3.3 Ω	805	2322 734 23308
P1	Murata potentiometer RG4M08-102VM-TG	1 k Ω		
TR1	NPN transistor	BD139		9330 912 20112
TR2	double PNP transistor	BVC62		5332 130 60505

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on a double copper-clad PCB: Rogers ULTRALAM 200 (B0300M1046QB) ($\epsilon_r = 2.55$); thickness 0.76 mm.

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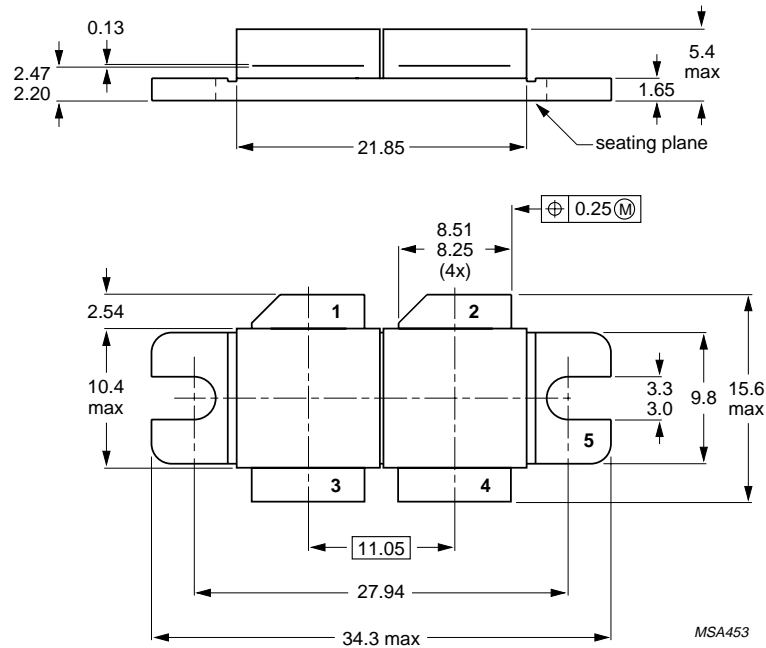
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PACKAGE OUTLINE



Dimensions in mm.
 Torque on screw: min. 0.6 Nm; max. 0.75 Nm.
 Recommended screw: cheese-head 4-40 UNC/2A.
 Heatsink compound must be applied sparingly and evenly distributed.

Fig.15 SOT262B.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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NOTES

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 615 800, Fax. +358 615 80920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. +30 1 4894 339/911, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
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Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
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Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
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2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

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04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

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Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
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United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
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United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
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Printed in The Netherlands

127041/1200/02/pp16

Date of release: 1996 Jul 26

Document order number: 9397 750 00987

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邮编：518033 E-mail:szss20@163.com QQ: 195847376

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