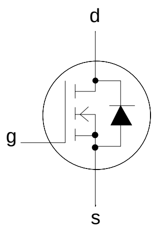
N-channel enhancement mode MOS transistor

BSH107

FEATURES

- Very low threshold voltage
- Fast switching
- Logic level compatible
- Subminiature surface mount package

SYMBOL



QUICK REFERENCE DATA

V_{DS} = 20 V

I_D = 1.75 A

$R_{DS(ON)} \leq 90$ mΩ (V_{GS} = 2.5 V)

$V_{GS(TO)} \geq 0.4$ V

GENERAL DESCRIPTION

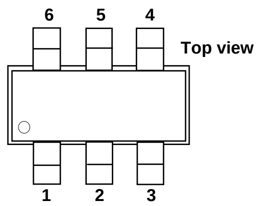
N-channel, enhancement mode, logic level, field-effect power transistor. This device has very low threshold voltage and extremely fast switching making it ideal for battery powered applications and high speed digital interfacing.

The BSH107 is supplied in the SOT457 subminiature surface mounting package.

PINNING

PIN	DESCRIPTION
1,2,5,6	drain
3	gate
4	source

SOT457



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	20	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	20	V
V_{GS}	Gate-source voltage		-	± 8	V
I_D	Drain current (DC)	T_a = 25 ˚C	-	1.75	A
		T_a = 100 ˚C	-	1.1	A
I_{DM}	Drain current (pulse peak value)	T_a = 25 ˚C	-	7	A
P_{tot}	Total power dissipation	T_a = 25 ˚C	-	0.417	W
		T_a = 100 ˚C	-	0.17	W
T_{stg}, T_j	Storage & operating temperature		- 55	150	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-a}$	Thermal resistance junction to ambient	FR4 board, minimum footprint	300	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 10 µA	20	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.4	0.57	-	V
		T_j = 150˚C	0.1	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1.2 A	-	55	75	mΩ
		V_{GS} = 2.5 V; I_D = 1.2 A	-	66	90	mΩ
		V_{GS} = 1.8 V; I_D = 0.6 A	-	81	110	mΩ
		V_{GS} = 2.5 V; I_D = 1.2 A; T_j = 150˚C	-	104	135	mΩ
g_{fs}	Forward transconductance	V_{DS} = 16 V; I_D = 0.6 A	0.5	2.2	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±8 V; V_{DS} = 0 V	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 16 V; V_{GS} = 0 V;	-	50	100	nA
		T_j = 150˚C	-	4.1	10	µA
$Q_{g(tot)}$	Total gate charge	I_D = 1 A; V_{DD} = 20 V; V_{GS} = 4.5 V	-	8	-	nC
Q_{gs}	Gate-source charge		-	0.5	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	1.3	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 20 V; I_D = 1 A;	-	2	-	ns
t_r	Turn-on rise time	V_{GS} = 8 V; R_G = 6 Ω	-	4.5	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	45	-	ns
t_f	Turn-off fall time		-	20	-	ns
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 16 V; f = 1 MHz	-	391	-	pF
C_{oss}	Output capacitance		-	184	-	pF
C_{rss}	Feedback capacitance		-	56	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_a = 25 ˚C	-	-	1.75	A
I_{DRM}	Pulsed reverse drain current		-	-	7	A
V_{SD}	Diode forward voltage	I_F = 0.8 A; V_{GS} = 0 V	-	0.68	1	V
t_{rr}	Reverse recovery time	I_F = 0.5 A; -dI_F/dt = 100 A/µs;	-	59	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 16 V	-	48	-	nC

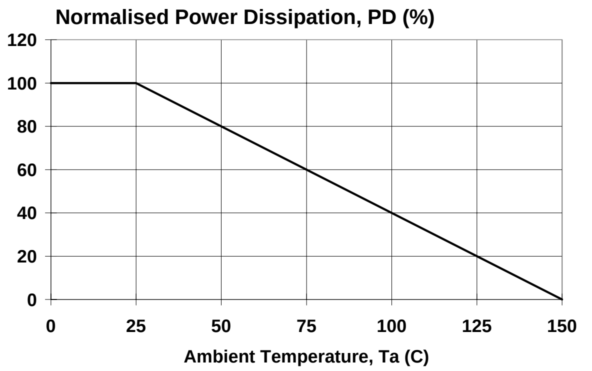


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D/P_{D\ 25\ ^\circ C} = f(T_a)$

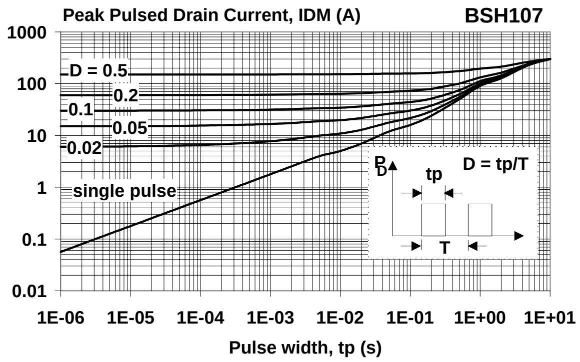


Fig.4. Transient thermal impedance.
$Z_{th\ j-a} = f(t)$; parameter $D = t_p/T$

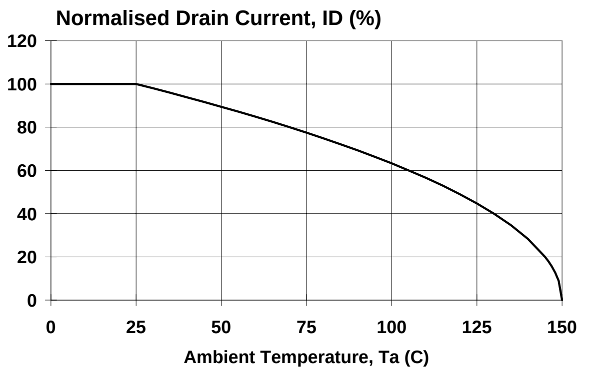


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D/I_{D\ 25\ ^\circ C} = f(T_a)$; conditions: $V_{GS} \geq 4.5$ V

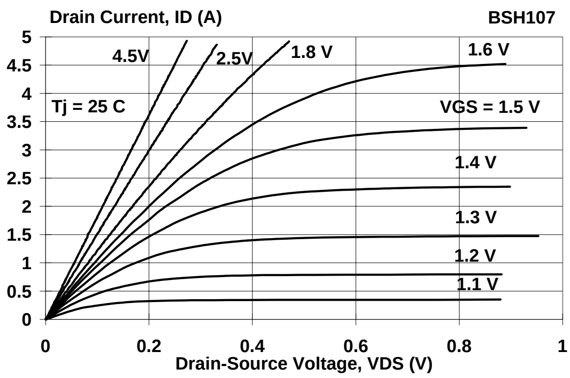


Fig.5. Typical output characteristics, $T_j = 25\ ^\circ C$.
$I_D = f(V_{DS})$; parameter V_{GS}

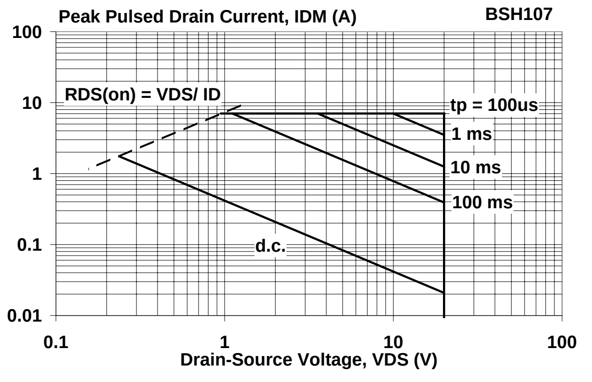


Fig.3. Safe operating area. $T_a = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

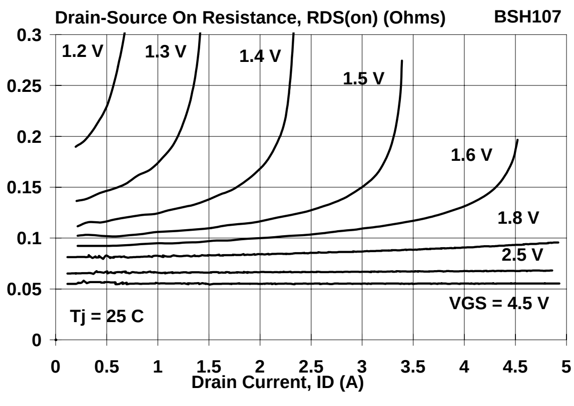


Fig.6. Typical on-state resistance, $T_j = 25\ ^\circ C$.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

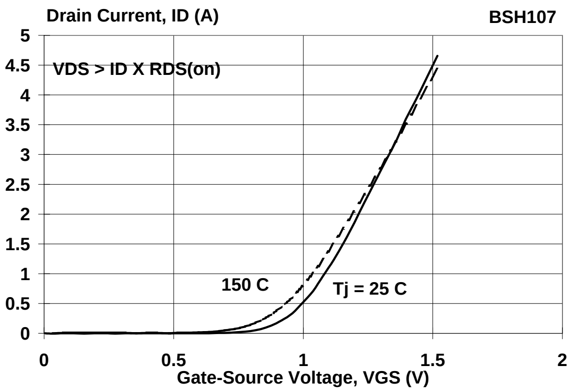


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$

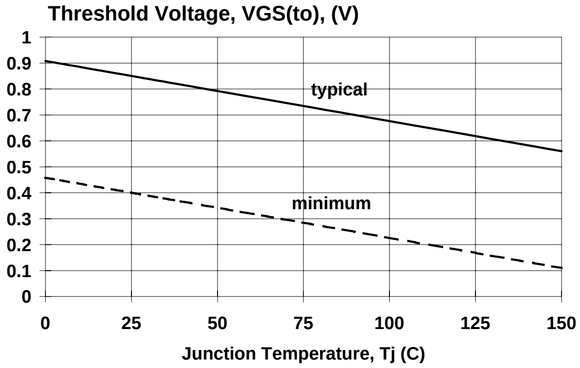


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

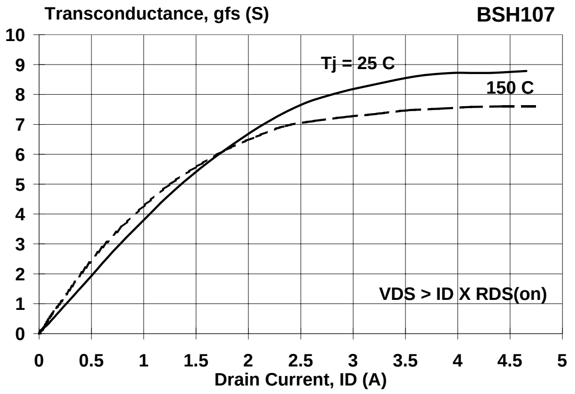


Fig.8. Typical transconductance, $T_j = 25$ ˚C.
$g_{fs} = f(I_D)$

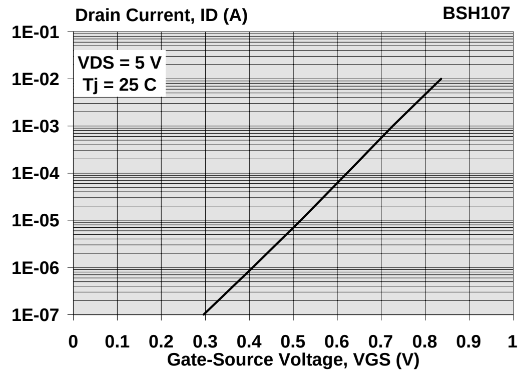


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ ˚C

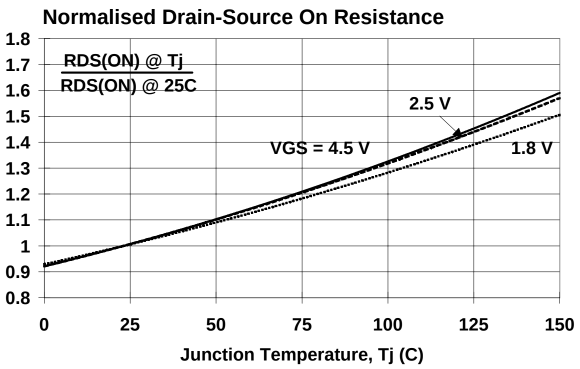


Fig.9. Normalised drain-source on-state resistance.
$R_{DS(ON)}/R_{DS(ON)25\,^\circ C} = f(T_j)$

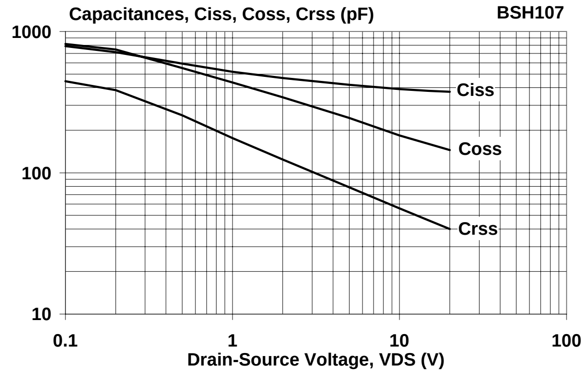


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

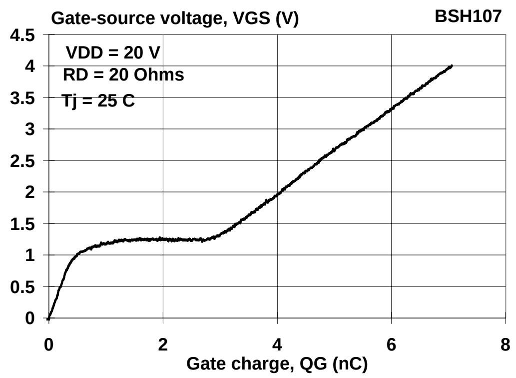


Fig.13. Typical turn-on gate-charge characteristics. *$V_{GS} = f(Q_G)$*

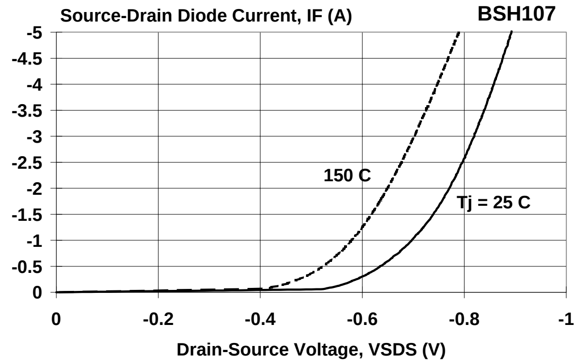
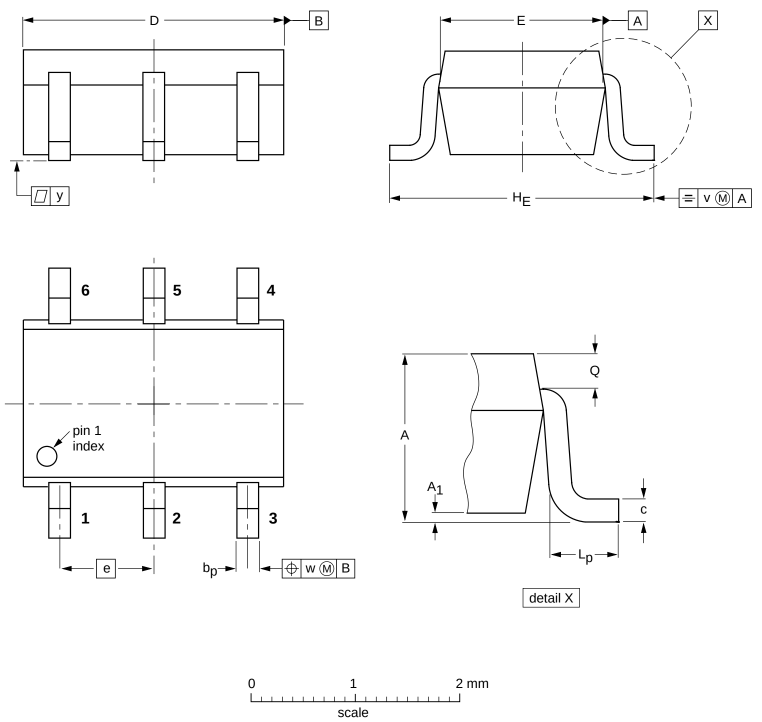


Fig.14. Typical reverse diode current. *$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j*

MECHANICAL DATA

Plastic surface mounted package; 6 leads **SOT457**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			97-02-28

Fig.15. SOT457 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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