

# DATA SHEET

## **BSS123**

N-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

# N-channel enhancement mode vertical D-MOS transistor

**BSS123**

**FEATURES**

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

**DESCRIPTION**

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

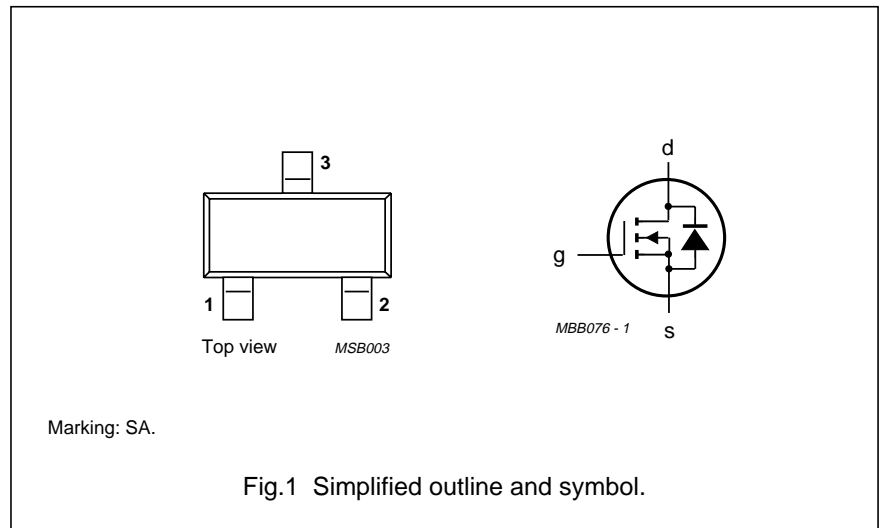
**PINNING - SOT23**

PIN	DESCRIPTION
1	gate
2	source
3	drain

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$V_{DS}$	drain-source voltage		100	V
$I_D$	drain current	DC value	150	mA
$R_{DS(on)}$	drain-source on-resistance	$I_D = 120\text{ mA}$ $V_{GS} = 10\text{ V}$	6	$\Omega$
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$ $V_{GS} = V_{DS}$	2.8	V

**PIN CONFIGURATION**



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### LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	100	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$I_D$	drain current	DC value	–	150	mA
$I_{DM}$	drain current	peak value	–	600	mA
$P_{tot}$	total power dissipation	up to $T_{amb} = 25\text{ }^\circ\text{C}$	–	250	mW
$T_{stg}$	storage temperature range		–65	150	$^\circ\text{C}$
$T_j$	junction temperature		–	150	$^\circ\text{C}$

### THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient (note 1)	500	K/W

### Note

1. Device mounted on a FR4 printboard.

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### CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\ \mu\text{A}$ $V_{GS} = 0$	100	–	–	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 60\ \text{V}$ $V_{GS} = 0$	–	–	10	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 20\ \text{V}$ $V_{DS} = 0$	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$ $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 120\ \text{mA}$ $V_{GS} = 10\ \text{V}$	–	3	6	$\Omega$
$ Y_{fs} $	transfer admittance	$I_D = 120\ \text{mA}$ $V_{DS} = 25\ \text{V}$	80	140	–	mS
$C_{iss}$	input capacitance	$V_{DS} = 25\ \text{V}$ $V_{GS} = 0$ $f = 1\ \text{MHz}$	–	24	40	pF
$C_{oss}$	output capacitance	$V_{DS} = 25\ \text{V}$ $V_{GS} = 0$ $f = 1\ \text{MHz}$	–	15	25	pF
$C_{rss}$	feedback capacitance	$V_{DS} = 25\ \text{V}$ $V_{GS} = 0$ $f = 1\ \text{MHz}$	–	4	10	pF
<b>Switching times (see Figs 2 and 3)</b>						
$t_{on}$	turn-on time	$I_D = 200\ \text{mA}$ $V_{DD} = 50\ \text{V}$ $V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	4	10	ns
$t_{off}$	turn-off time	$I_D = 250\ \text{mA}$ $V_{DD} = 50\ \text{V}$ $V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	10	20	ns

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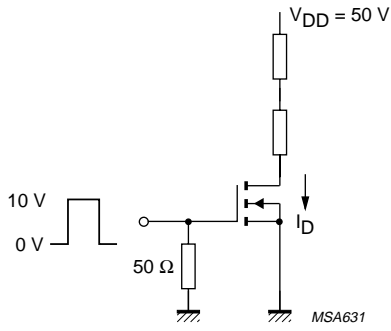


Fig.2 Switching time test circuit.

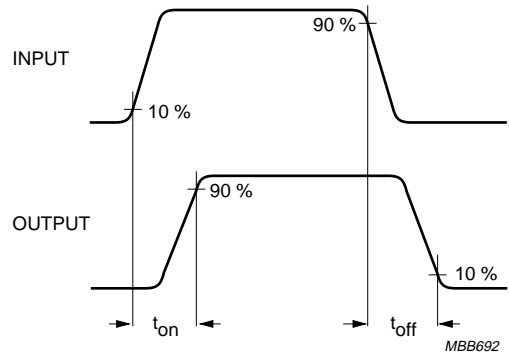


Fig.3 Input and output waveforms.

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## PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max.	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28

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<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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