

TrenchMOS™ transistor Standard level FET

PHB69N03T

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting using 'trench' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in DC-DC converters and general purpose switching applications.

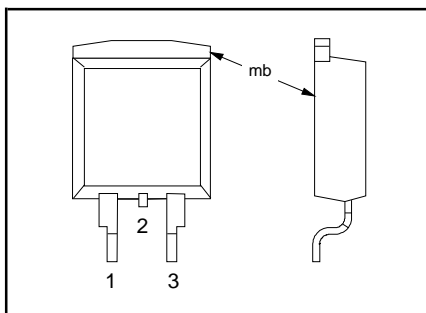
QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | UNIT |
|--------------|---|------|------|
| V_{DS} | Drain-source voltage | 30 | V |
| I_D | Drain current (DC) | 69 | A |
| P_{tot} | Total power dissipation | 125 | W |
| T_j | Junction temperature | 175 | °C |
| $R_{DS(ON)}$ | Drain-source on-state resistance $V_{GS} = 10\text{ V}$ | 14 | mΩ |

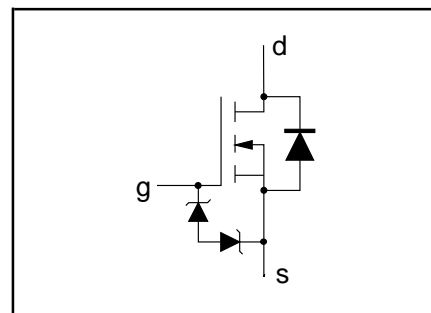
PINNING - SOT404

| PIN | DESCRIPTION |
|-----|-------------|
| 1 | gate |
| 2 | drain |
| 3 | source |
| mb | drain |

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------------|----------------------------------|--------------------------------------|------|------|------|
| V_{DS} | Drain-source voltage | - | - | 30 | V |
| V_{DGR} | Drain-gate voltage | $R_{GS} = 20\text{ k}\Omega$ | - | 30 | V |
| $\pm V_{GS}$ | Gate-source voltage | - | - | 20 | V |
| I_D | Drain current (DC) | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 69 | A |
| I_D | Drain current (DC) | $T_{mb} = 100\text{ }^\circ\text{C}$ | - | 48 | A |
| I_{DM} | Drain current (pulse peak value) | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 240 | A |
| P_{tot} | Total power dissipation | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 125 | W |
| T_{stg}, T_j | Storage & operating temperature | - | - 55 | 175 | °C |

THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | TYP. | MAX. | UNIT |
|----------------|--|------------------------------|------|------|------|
| $R_{th\ j-mb}$ | Thermal resistance junction to mounting base | - | - | 1.2 | K/W |
| $R_{th\ j-a}$ | Thermal resistance junction to ambient | minimum footprint, FR4 board | 50 | - | K/W |

ESD LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|--------|---|-----------------------------------|------|------|------|
| V_C | Electrostatic discharge capacitor voltage, all pins | Human body model (100 pF, 1.5 kΩ) | - | 2 | kV |

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STATIC CHARACTERISTICS

T_j = 25°C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------------|----------------------------------|---|-----------------|---------------|-----------------|----------------|
| V _{(BR)DSS} | Drain-source breakdown voltage | V _{GS} = 0 V; I _D = 0.25 mA; T _j = -55°C | 30 27 | - - | - - | V V |
| V _{GS(TO)} | Gate threshold voltage | V _{DS} = V _{GS} ; I _D = 1 mA T _j = 175°C T _j = -55°C | 2.0 1.0 - | 3.0 - - | 4.0 - 4.4 | V V V |
| I _{DSS} | Zero gate voltage drain current | V _{DS} = 30 V; V _{GS} = 0 V; T _j = 175°C | - | 0.05 | 10 | μA |
| I _{GSS} | Gate source leakage current | V _{GS} = ±10 V; V _{DS} = 0 V T _j = 175°C | - | 0.02 | 500 1 20 | μA μA μA |
| ±V _{(BR)GSS} | Gate-source breakdown voltage | I _G = ±1 mA; | 16 | - | - | V |
| R _{DS(ON)} | Drain-source on-state resistance | V _{GS} = 10 V; I _D = 25 A T _j = 175°C | - - | 12 - | 14 26 | mΩ mΩ |

DYNAMIC CHARACTERISTICS

T_{mb} = 25°C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------------|----------------------------|---|------|------|------|------|
| g _{fs} | Forward transconductance | V _{DS} = 25 V; I _D = 25 A | 9 | 18 | - | S |
| Q _{g(tot)} | Total gate charge | I _D = 69 A; V _{DD} = 24 V; V _{GS} = 10 V | - | 38 | - | nC |
| Q _{gs} | Gate-source charge | | - | 7 | - | nC |
| Q _{gd} | Gate-drain (Miller) charge | | - | 14 | - | nC |
| C _{iss} | Input capacitance | V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz | - | 1500 | 2000 | pF |
| C _{oss} | Output capacitance | | - | 480 | 550 | pF |
| C _{rss} | Feedback capacitance | | - | 220 | 300 | pF |
| t _{d on} | Turn-on delay time | V _{DD} = 25 V; I _D = 25 A; | - | 22 | 35 | ns |
| t _r | Turn-on rise time | V _{GS} = 10 V; R _G = 5 Ω | - | 30 | 60 | ns |
| t _{d off} | Turn-off delay time | Resistive load | - | 40 | 50 | ns |
| t _f | Turn-off fall time | | - | 25 | 38 | ns |
| L _d | Internal drain inductance | Measured from tab to centre of die | - | 3.5 | - | nH |
| L _d | Internal drain inductance | Measured from drain lead solder point to centre of die | - | 4.5 | - | nH |
| L _s | Internal source inductance | Measured from source lead solder point to source bond pad | - | 7.5 | - | nH |

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------|----------------------------------|---|------|------|------|------|
| I _{DR} | Continuous reverse drain current | | - | - | 69 | A |
| I _{DRM} | Pulsed reverse drain current | | - | - | 240 | A |
| V _{SD} | Diode forward voltage | I _F = 25 A; V _{GS} = 0 V | - | 0.95 | 1.2 | V |
| | | I _F = 69 A; V _{GS} = 0 V | - | 1.0 | - | V |
| t _{rr} | Reverse recovery time | I _F = 69 A; -dI _F /dt = 100 A/μs; | - | 60 | - | ns |
| Q _{rr} | Reverse recovery charge | V _{GS} = -10 V; V _R = 25 V | - | 0.1 | - | μC |

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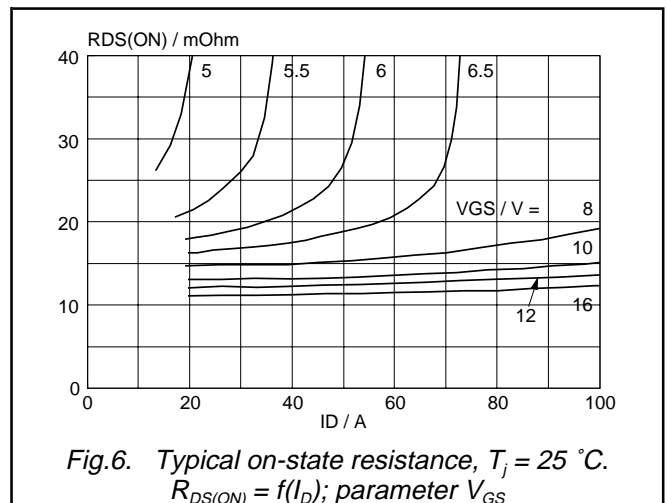
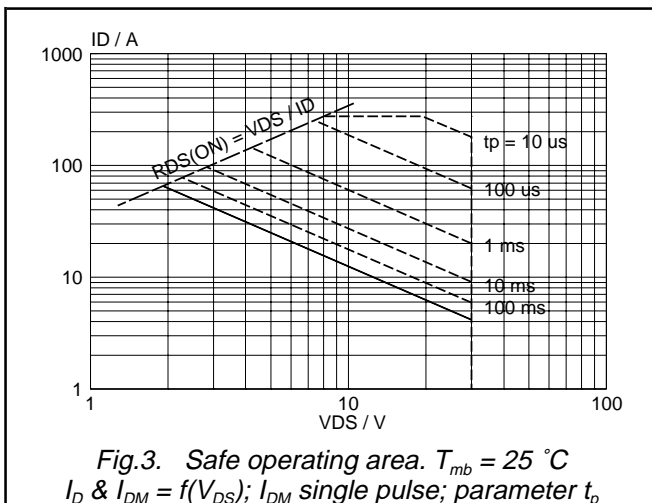
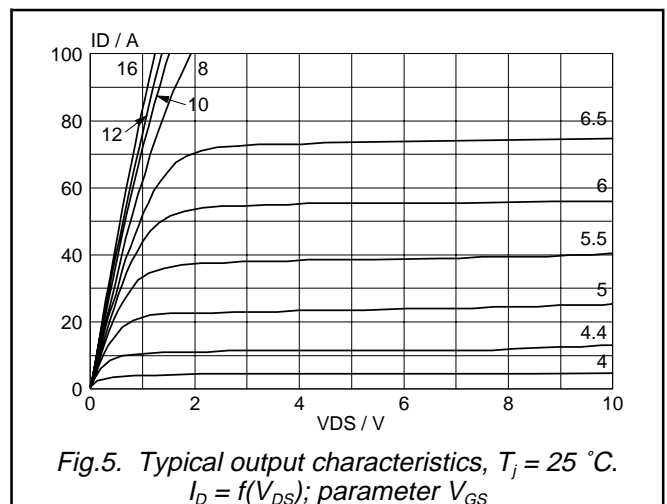
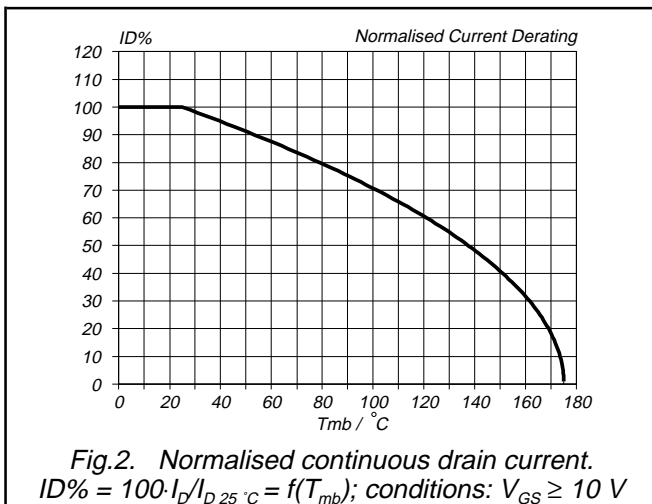
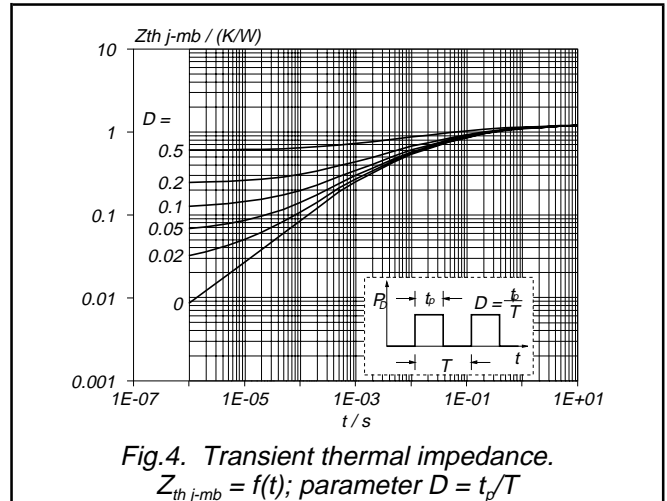
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AVALANCHE LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------|---|--|------|------|------|------|
| W_{DSS} | Drain-source non-repetitive unclamped inductive turn-off energy | $I_D = 36 \text{ A}$; $V_{DD} \leq 15 \text{ V}$; $V_{GS} = 10 \text{ V}$; $R_{GS} = 50 \text{ } \Omega$; $T_{mb} = 25 \text{ } ^\circ\text{C}$ | - | - | 125 | mJ |

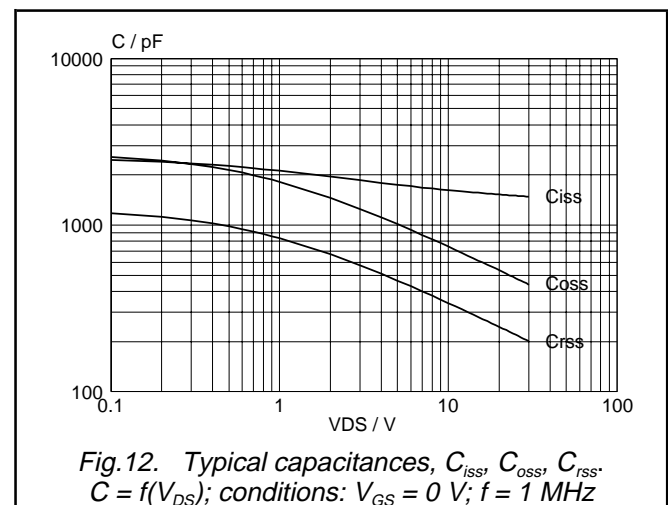
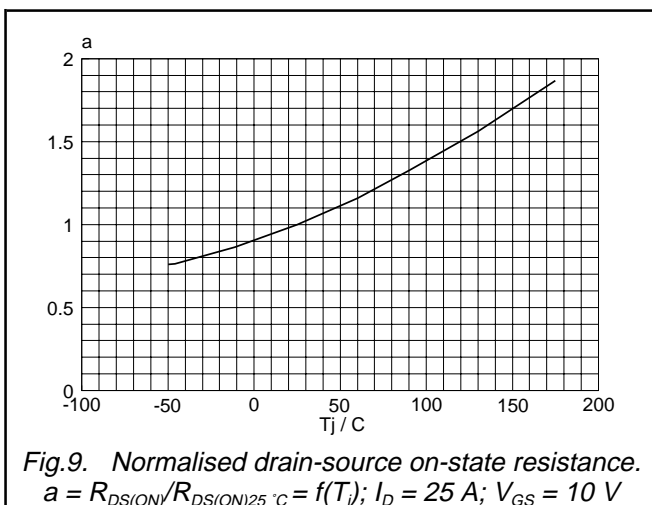
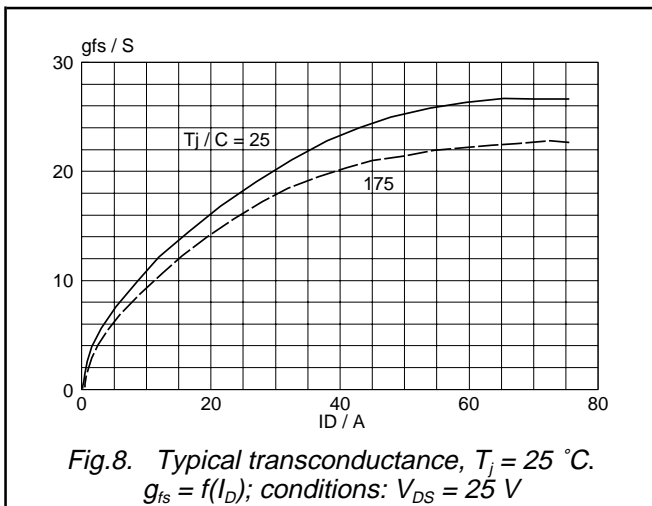
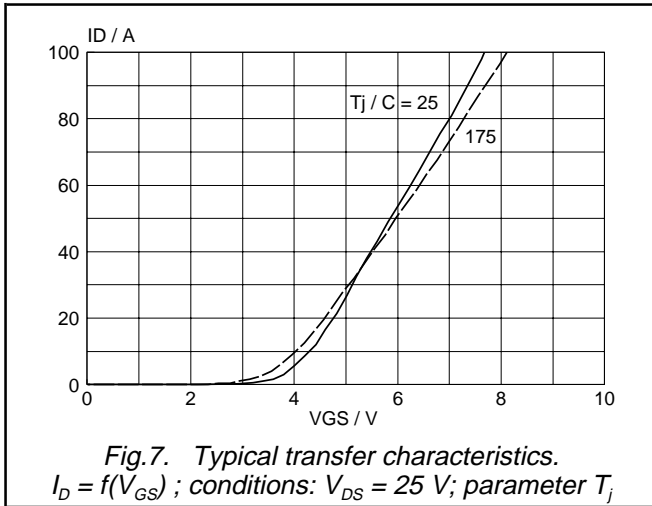
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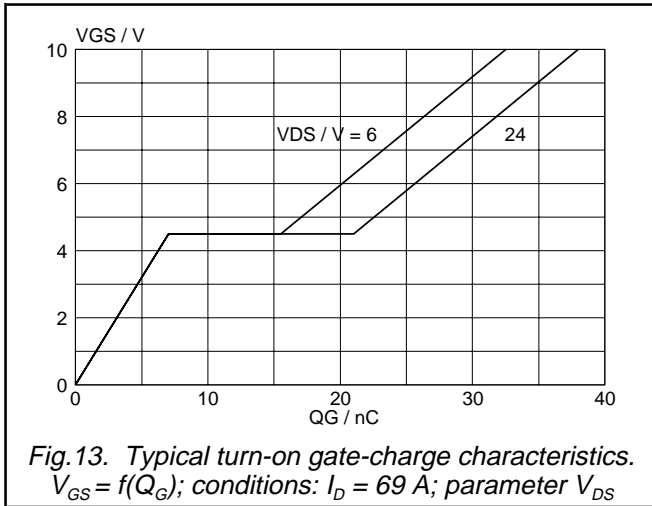


Fig. 13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 69\text{ A}$; parameter V_{DS}

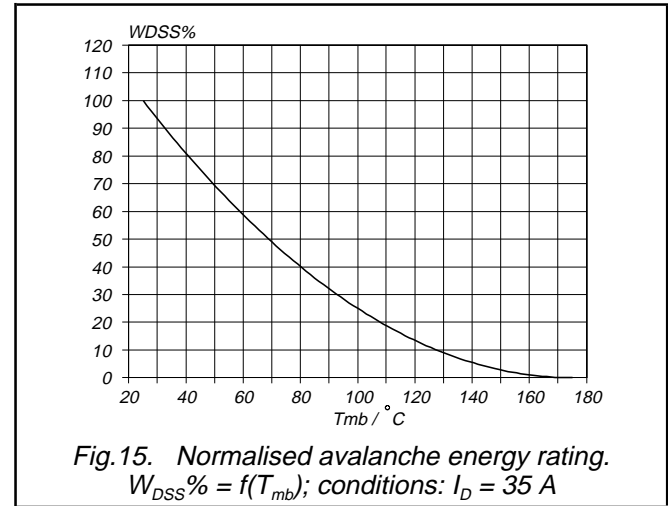


Fig. 15. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 35\text{ A}$

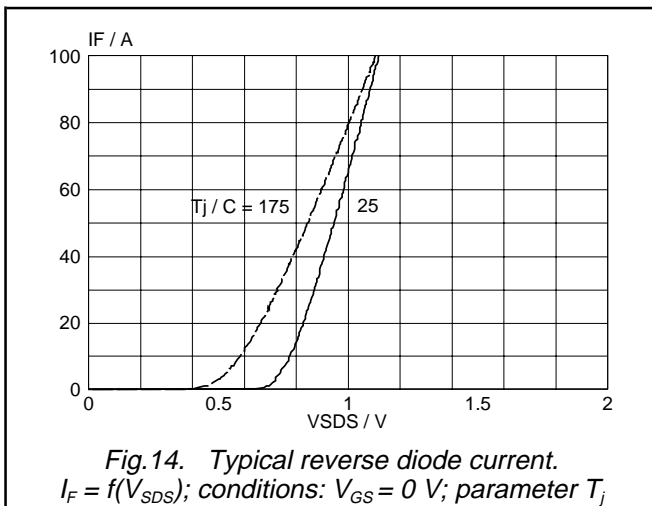


Fig. 14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0\text{ V}$; parameter T_j



Fig. 16. Avalanche energy test circuit.
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

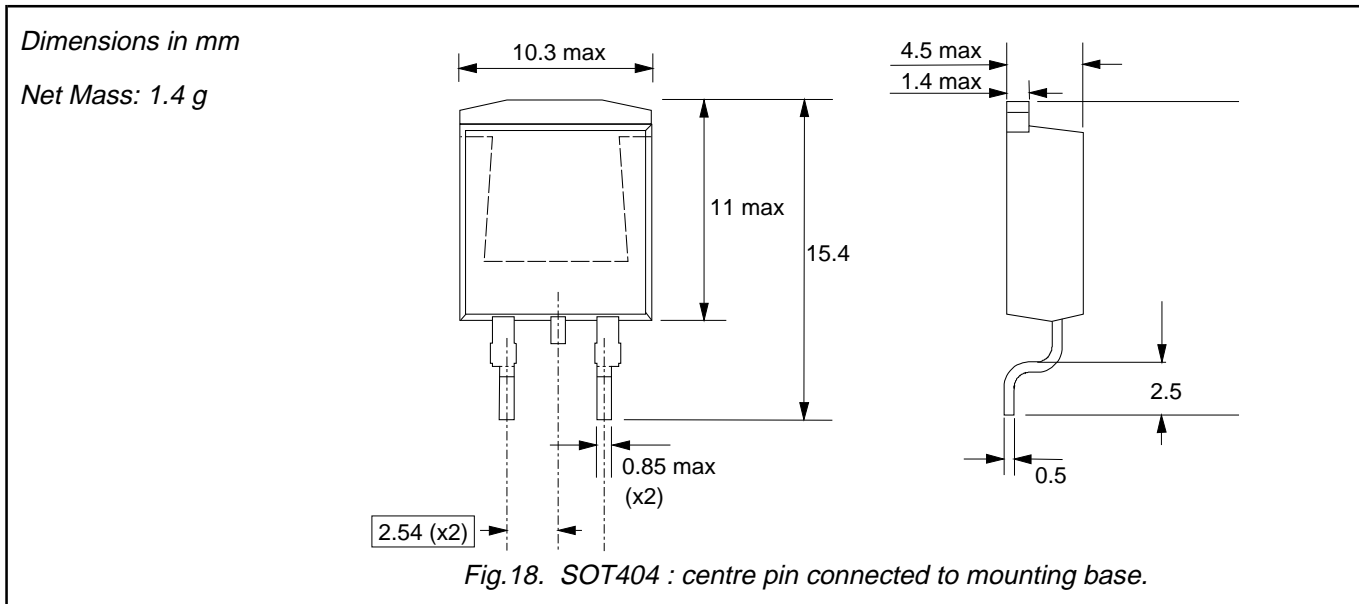


Fig. 17. Switching test circuit.

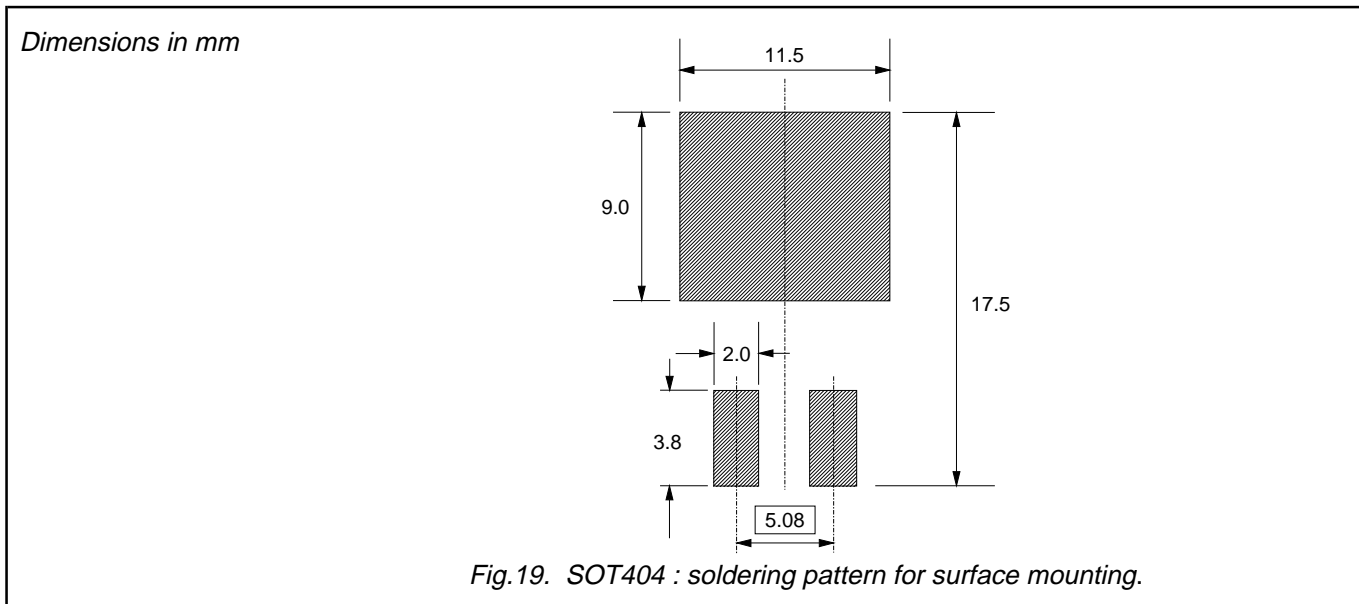
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MECHANICAL DATA



MOUNTING INSTRUCTIONS



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

| | |
|--|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
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