

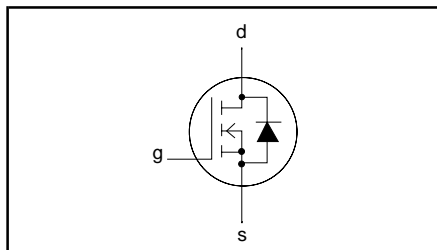
TrenchMOS™ transistor Logic level FET

PHP45N03LT, PHB45N03LT, PHD45N03LT

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 30\text{ V}$
$I_D = 45\text{ A}$
$R_{DS(ON)} \leq 24\text{ m}\Omega (V_{GS} = 5\text{ V})$
$R_{DS(ON)} \leq 21\text{ m}\Omega (V_{GS} = 10\text{ V})$

GENERAL DESCRIPTION

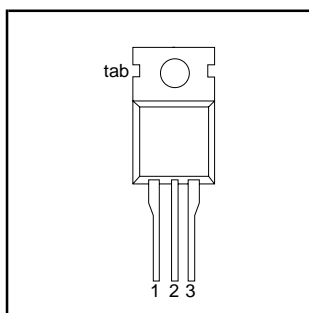
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using 'trench' technology. The combination of very low on-state resistance and low switching losses make this device the optimum choice in high speed computer motherboard d.c. to d.c. converters.

The PHP45N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.
 The PHB45N03LT is supplied in the SOT404 surface mounting package.
 The PHD45N03LT is supplied in the SOT428 surface mounting package.

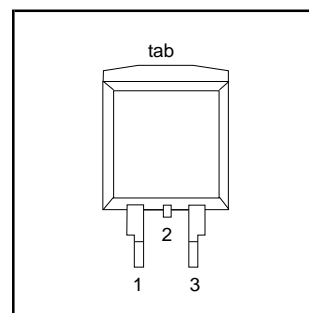
PINNING

PIN	DESCRIPTION
1	gate
2	drain ¹
3	source
tab	drain

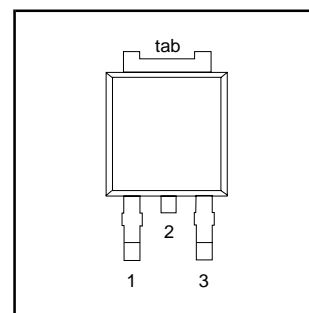
SOT78 (TO220AB)



SOT404



SOT428



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$	-	30	V
V_{DGR}	Drain-gate voltage	$T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	Gate-source voltage		-	± 15	V
V_{GSM}	Pulsed gate-source voltage	$T_j \leq 150\text{ }^\circ\text{C}$	-	± 20	V
I_D	Continuous drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$	-	45	A
		$T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$	-	33	A
I_{DM}	Pulsed drain current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	180	A
P_D	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	86	W
T_j, T_{stg}	Operating junction and storage temperature		-55	175	$^\circ\text{C}$

¹ It is not possible to make connection to pin 2 of the SOT428 or SOT404 packages.

TrenchMOS™ transistor
Logic level FET
PHP45N03LT, PHB45N03LT, PHD45N03LT
THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	1.75	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	SOT78 package, in free air SOT404 and SOT428 packages, pcb mounted, minimum footprint	-	60	-	K/W
			-	50	-	K/W

ELECTRICAL CHARACTERISTICS
 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA};$ $T_j = -55^\circ\text{C}$	30 27	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$ $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	1 0.5 -	1.5 - -	2 - 2.3	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}$ $V_{GS} = 5\text{ V}; I_D = 25\text{ A}$ $V_{GS} = 5\text{ V}; I_D = 25\text{ A}; T_j = 175^\circ\text{C}$	- - -	16 20 -	21 24 45	mΩ mΩ mΩ
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 25\text{ A}$	8	27	-	S
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 30\text{ V}; V_{GS} = 0\text{ V};$ $T_j = 175^\circ\text{C}$	-	0.05	10	μA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 5\text{ V}; V_{DS} = 0\text{ V}$	-	10	500	μA
			-	10	100	nA
$Q_{g(tot)}$	Total gate charge	$I_D = 20\text{ A}; V_{DD} = 24\text{ V}; V_{GS} = 10\text{ V}$	-	40	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	10	-	nC
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 15\text{ V}; I_D = 25\text{ A};$	-	10	20	ns
t_r	Turn-on rise time	$V_{GS} = 10\text{ V}; R_G = 5\ \Omega$	-	50	75	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	50	75	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	1050	-	pF
C_{oss}	Output capacitance		-	270	-	pF
C_{rss}	Feedback capacitance		-	140	-	pF

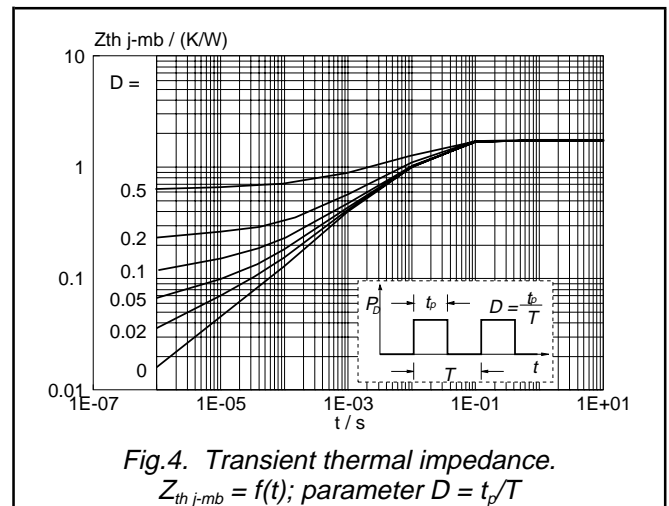
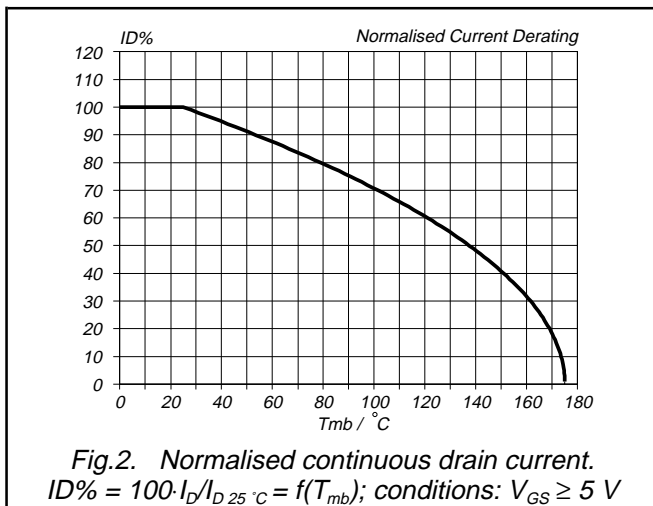
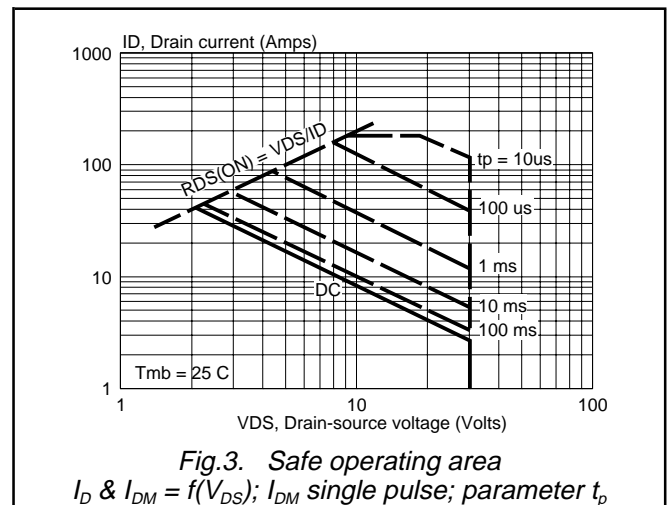
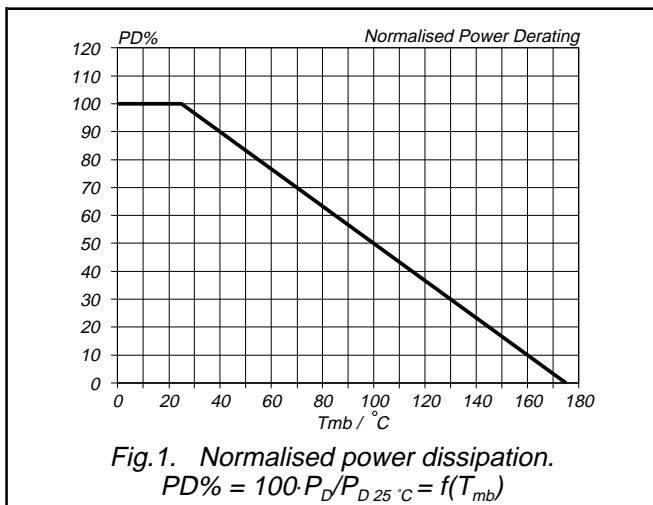
TrenchMOS™ transistor
Logic level FET

PHP45N03LT, PHB45N03LT, PHD45N03LT

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

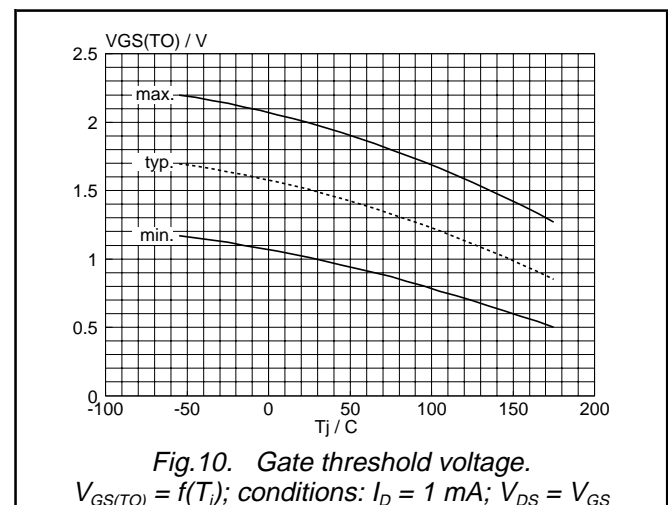
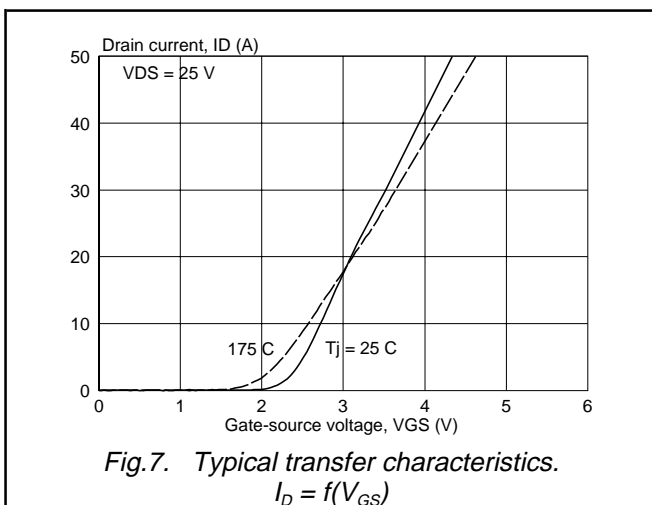
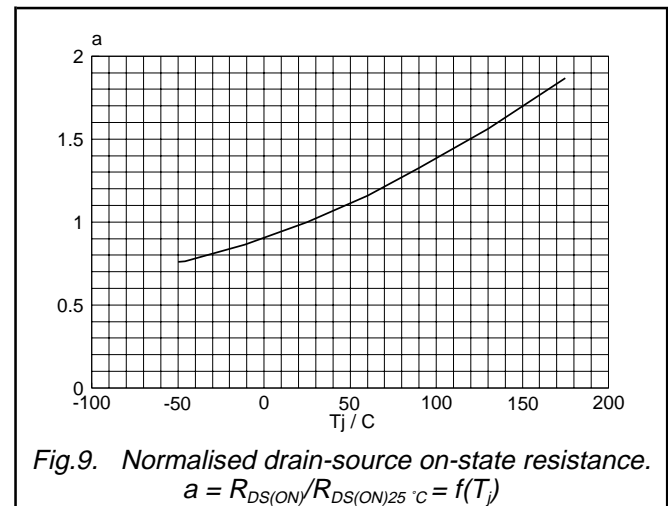
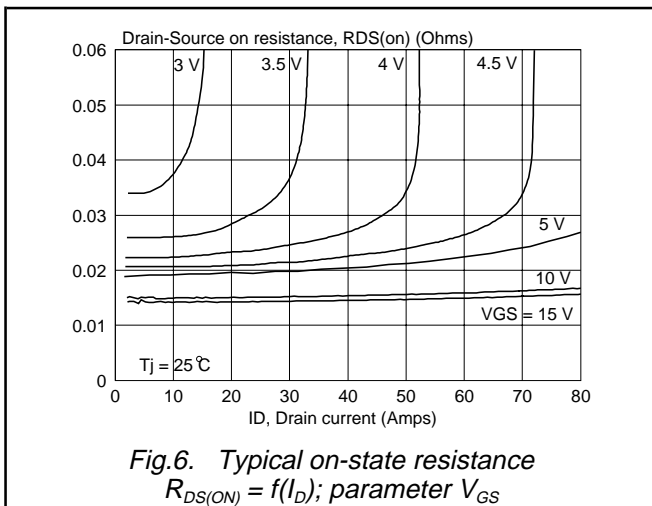
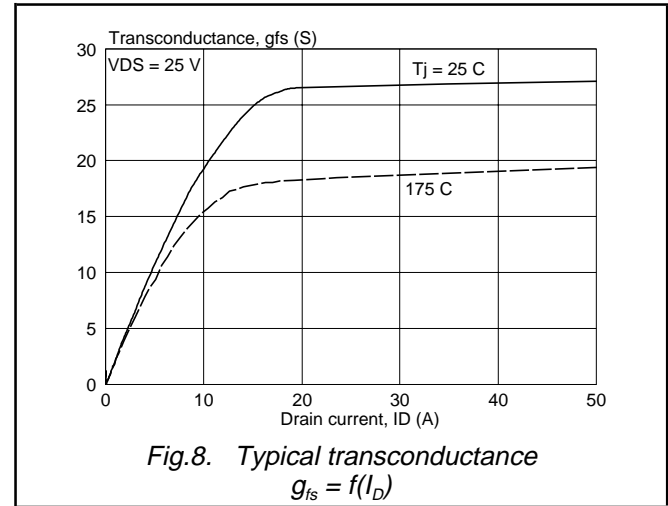
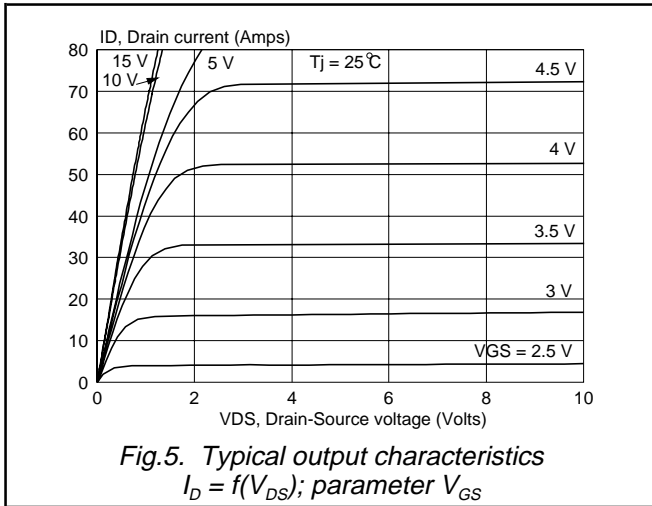
T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _S	Continuous source current (body diode)		-	-	45	A
I _{SM}	Pulsed source current (body diode)		-	-	180	A
V _{SD}	Diode forward voltage	I _F = 25 A; V _{GS} = 0 V I _F = 40 A; V _{GS} = 0 V	-	0.95 1.0	1.2 -	V
t _{rr}	Reverse recovery time	I _F = 40 A; -di _F /dt = 100 A/μs; V _{GS} = -10 V; V _R = 25 V	-	52	-	ns
Q _{rr}	Reverse recovery charge		-	0.08	-	μC



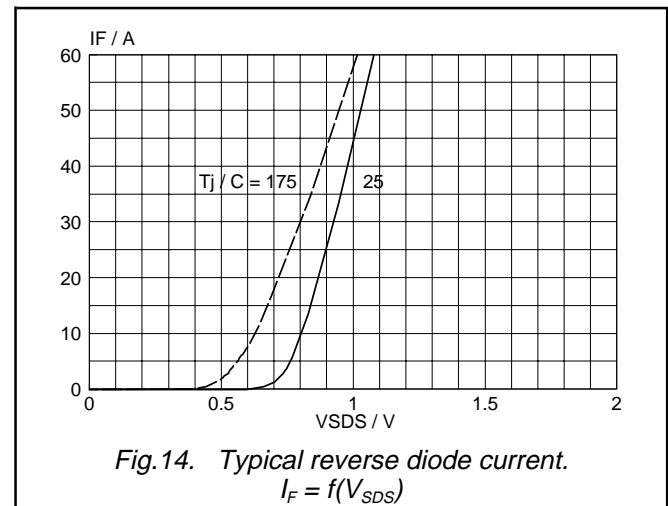
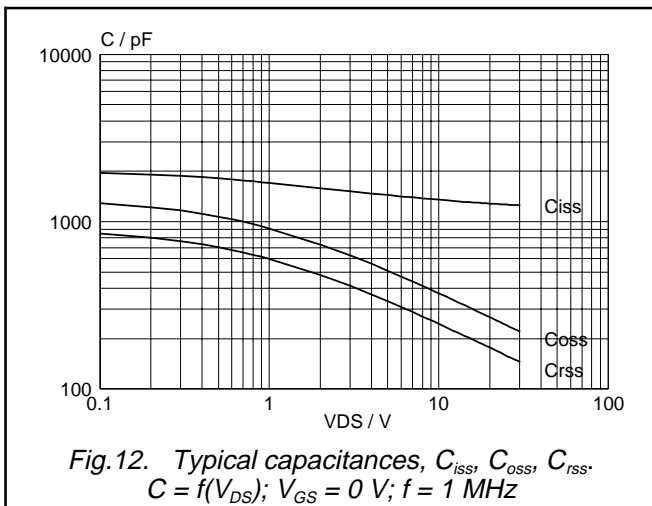
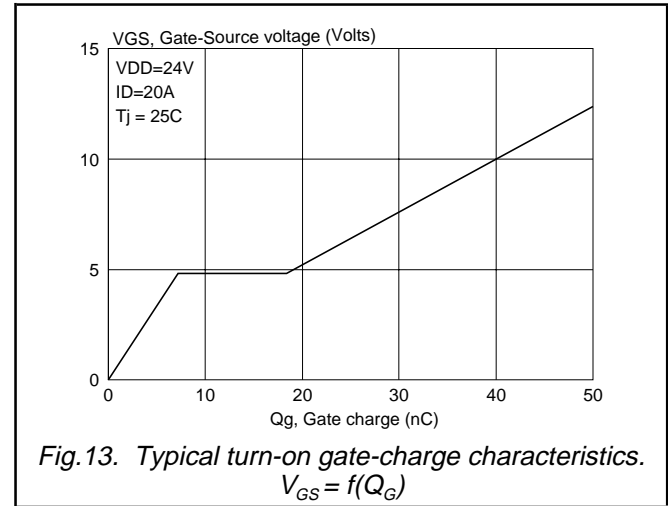
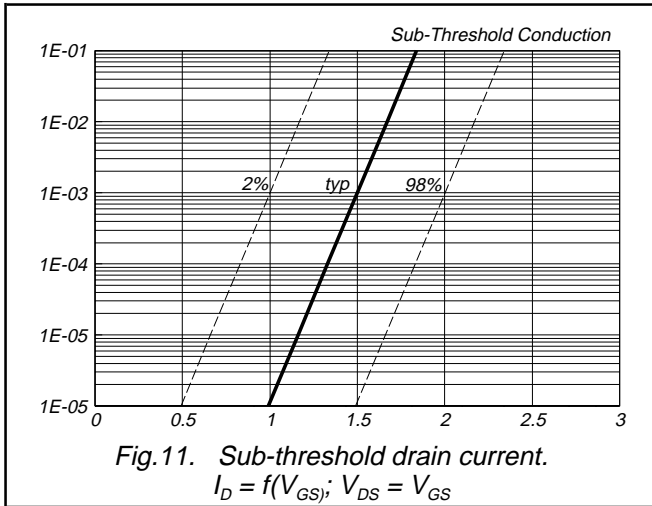
TrenchMOS™ transistor
Logic level FET

PHP45N03LT, PHB45N03LT, PHD45N03LT



TrenchMOS™ transistor
Logic level FET

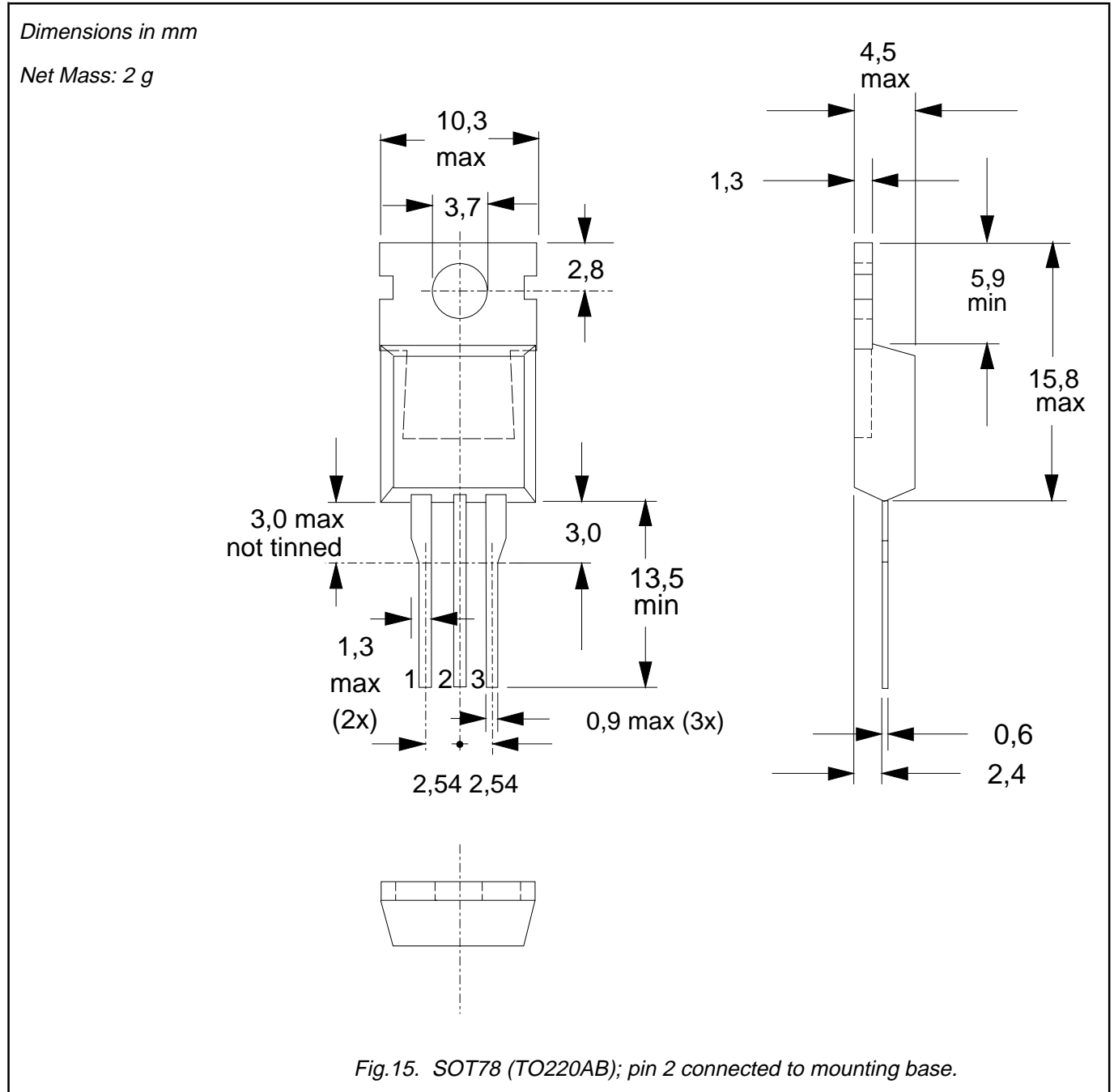
PHP45N03LT, PHB45N03LT, PHD45N03LT



TrenchMOS™ transistor
Logic level FET

PHP45N03LT, PHB45N03LT, PHD45N03LT

MECHANICAL DATA



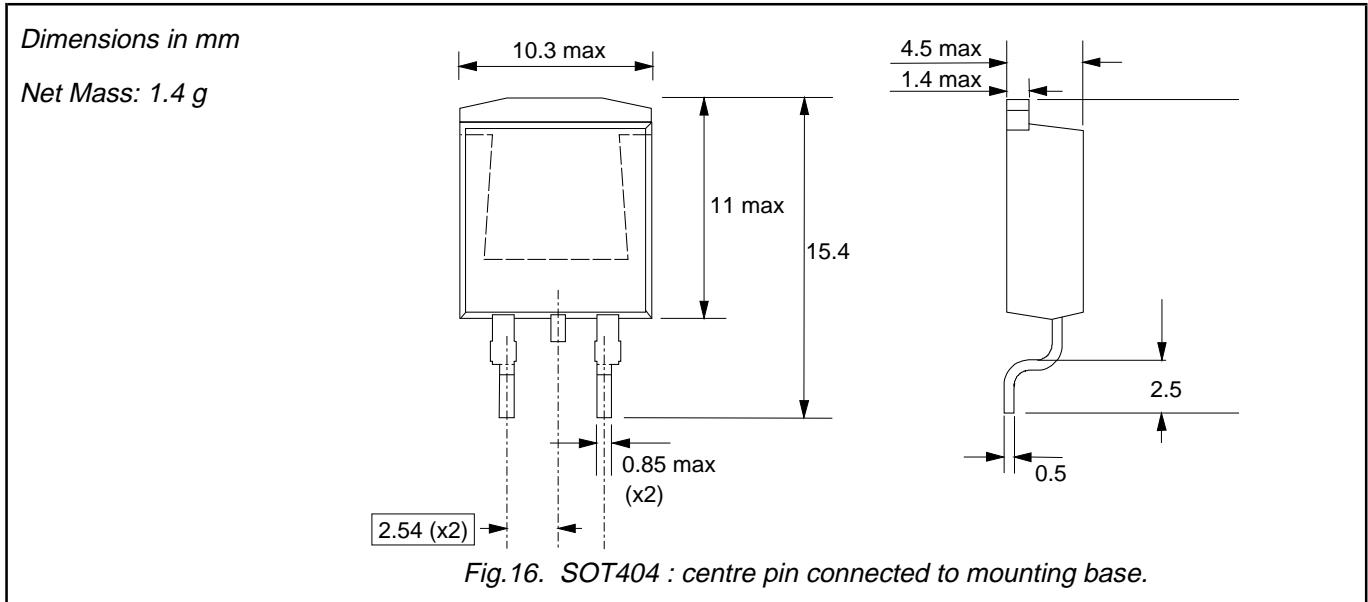
Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

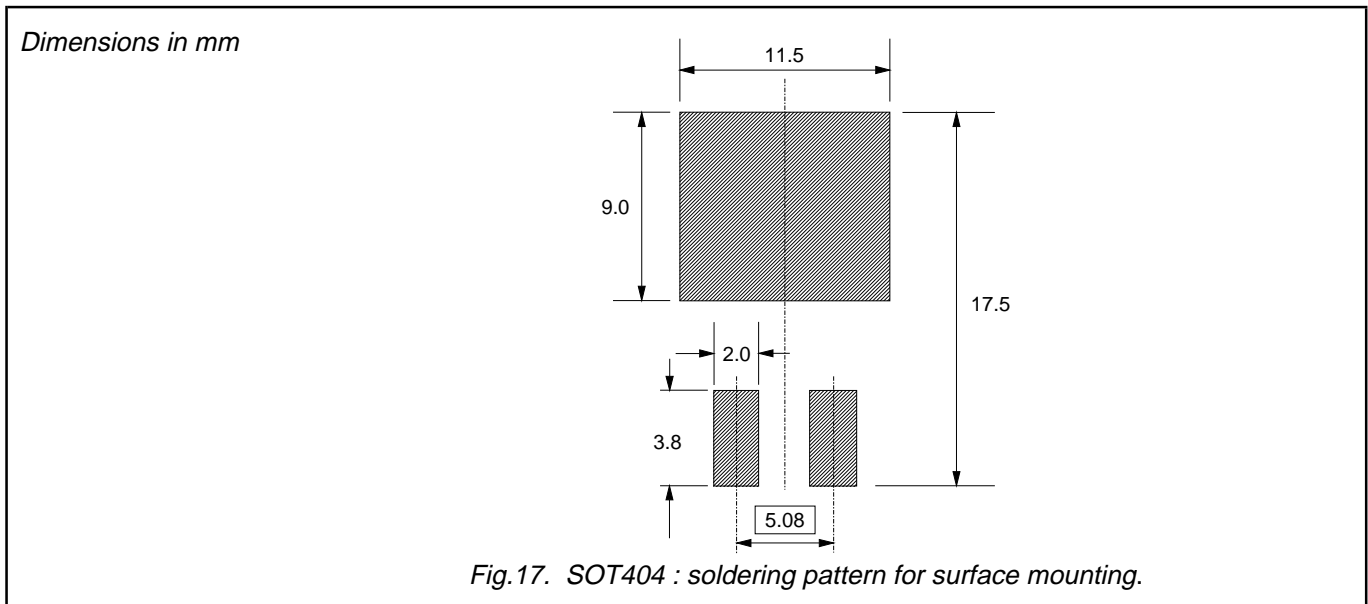
TrenchMOS™ transistor
Logic level FET

PHP45N03LT, PHB45N03LT, PHD45N03LT

MECHANICAL DATA



MOUNTING INSTRUCTIONS



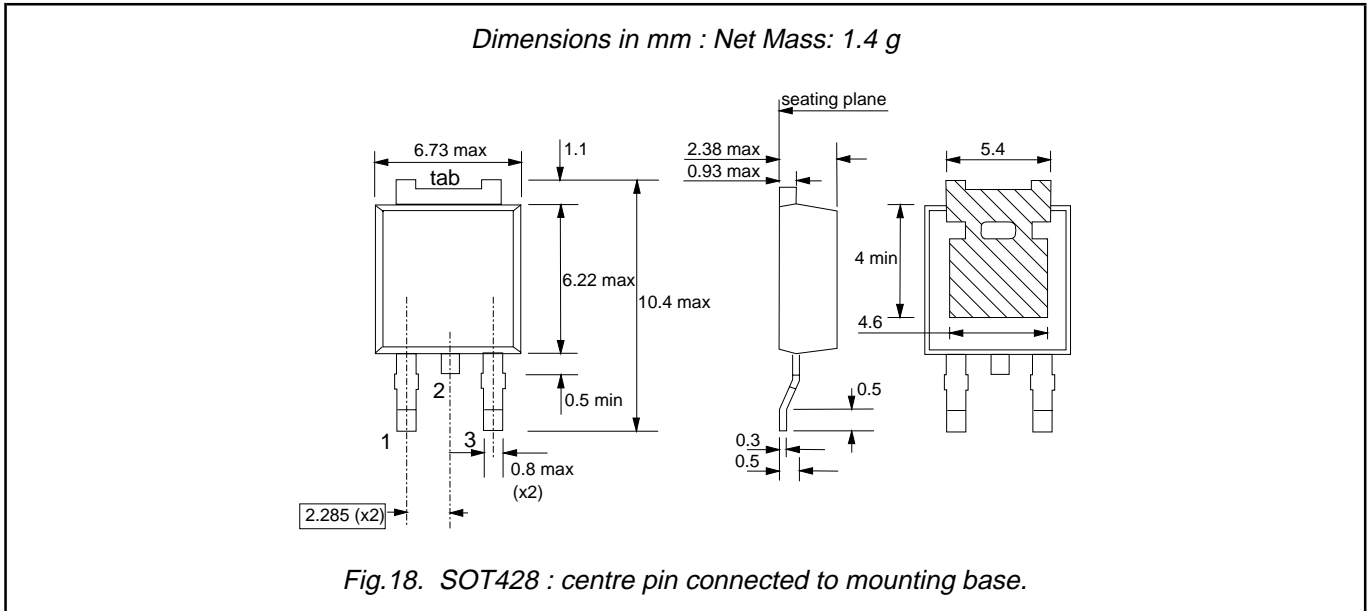
Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

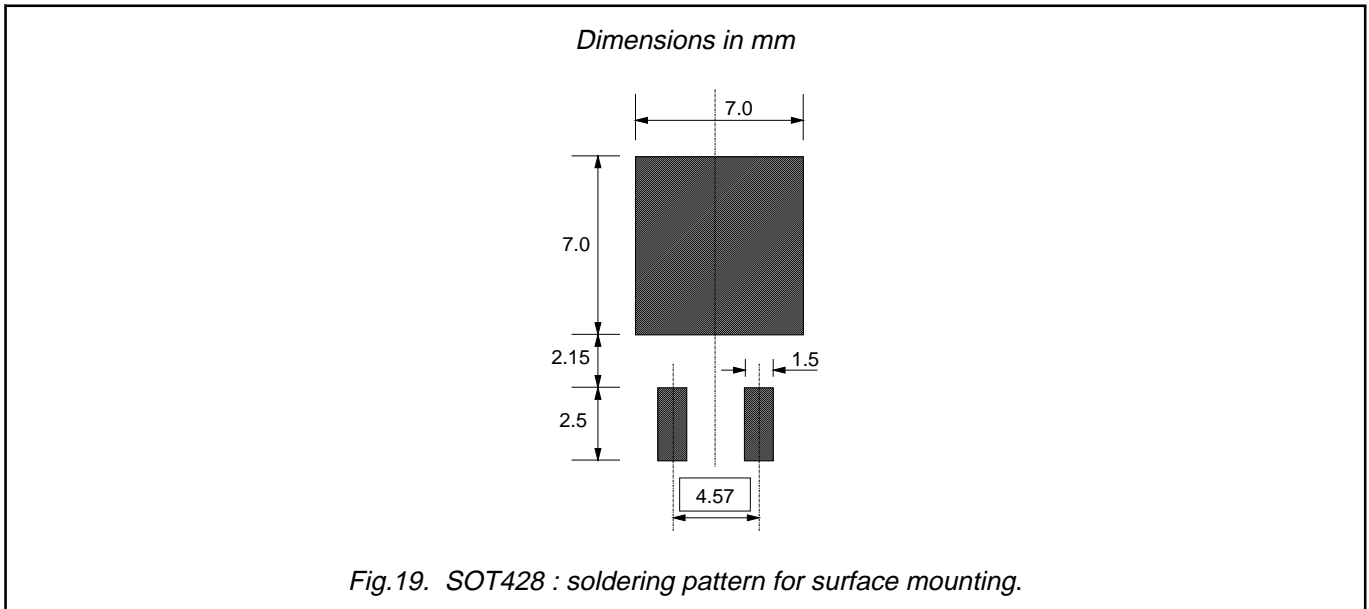
TrenchMOS™ transistor
Logic level FET

PHP45N03LT, PHB45N03LT, PHD45N03LT

MECHANICAL DATA



MOUNTING INSTRUCTIONS



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

TrenchMOS™ transistor
Logic level FET

PHP45N03LT, PHB45N03LT, PHD45N03LT

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
© Philips Electronics N.V. 1998	
All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.	
The information presented in this document does not form part of any quotation or contract, it is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

SUNSTAR 商斯达实业集团是集研发、生产、工程、销售、代理经销、技术咨询、信息服务等为一体的高科技企业，是专业高科技电子产品生产厂家，是具有 10 多年历史的专业电子元器件供应商，是中国最早和最大的仓储式连锁规模经营大型综合电子零部件代理分销商之一，是一家专业代理和分销世界各大品牌 IC 芯片和电子元器件的连锁经营综合性国际公司，专业经营进口、国产名厂名牌电子元件，型号、种类齐全。在香港、北京、深圳、上海、西安、成都等全国主要电子市场设有直属分公司和产品展示展销窗口门市部专卖店及代理分销商，已在全国范围内建成强大统一的供货和代理分销网络。我们专业代理经销、开发生产电子元器件、集成电路、传感器、微波光电元器件、工控机/DOC/DOM 电子盘、专用电路、单片机开发、MCU/DSP/ARM/FPGA 软件硬件、二极管、三极管、模块等，是您可靠的一站式现货配套供应商、方案提供商、部件功能模块开发配套商。商斯达实业公司拥有庞大的资料库，有数位毕业于著名高校——有中国电子工业摇篮之称的西安电子科技大学（西军电）并长期从事国防尖端科技研究的高级工程师为您精挑细选、量身订做各种高科技电子元器件，并解决各种技术问题。

微波光电部专业代理经销高频、微波、光纤、光电元器件、组件、部件、模块、整机；电磁兼容元器件、材料、设备；微波 CAD、EDA 软件、开发测试仿真工具；微波、光纤仪器仪表。欢迎国外高科技微波、光纤厂商将优秀产品介绍到中国、共同开拓市场。长期大量现货专业批发高频、微波、卫星、光纤、电视、CATV 器件：晶振、VCO、连接器、PIN 开关、变容二极管、开关二极管、低噪晶体管、功率电阻及电容、放大器、功率管、MMIC、混频器、耦合器、功分器、振荡器、合成器、衰减器、滤波器、隔离器、环行器、移相器、调制解调器；光电子元件和组件：红外发射管、红外接收管、光电开关、光敏管、发光二极管和发光二极管组件、半导体激光二极管和激光器组件、光电探测器和光接收组件、光发射接收模块、光纤激光器和光放大器、光调制器、光开关、DWDM 用光发射和接收器件、用户接入系统光收发器件与模块、光纤连接器、光纤跳线/尾纤、光衰减器、光纤适配器、光隔离器、光耦合器、光环行器、光复用器/转换器；无线收发芯片和模组、蓝牙芯片和模组。

更多产品请看本公司产品专用销售网站：

商斯达中国传感器科技信息网：<http://www.sensor-ic.com/>

商斯达工控安防网：<http://www.pc-ps.net/>

商斯达电子元器件网：<http://www.sunstare.com/>

商斯达微波光电产品网：[HTTP://www.rfoe.net/](http://www.rfoe.net/)

商斯达消费电子产品网：<http://www.icasic.com/>

商斯达实业科技产品网：<http://www.sunstars.cn/> 微波元器件销售热线：

地址：深圳市福田区福华路福庆街鸿图大厦 1602 室

电话：0755-82884100 83397033 83396822 83398585

传真：0755-83376182 (0) 13823648918 MSN: SUNS8888@hotmail.com

邮编：518033 E-mail:szss20@163.com QQ: 195847376

深圳赛格展销部：深圳华强北路赛格电子市场 2583 号 电话：0755-83665529 25059422

技术支持：0755-83394033 13501568376

欢迎索取免费详细资料、设计指南和光盘；产品凡多，未能尽录，欢迎来电查询。

北京分公司：北京海淀区知春路 132 号中发电子大厦 3097 号

TEL: 010-81159046 82615020 13501189838 FAX: 010-62543996

上海分公司：上海市北京东路 668 号上海赛格电子市场 D125 号

TEL: 021-28311762 56703037 13701955389 FAX: 021-56703037

西安分公司：西安高新开发区 20 所(中国电子科技集团导航技术研究所)

西安劳动南路 88 号电子商城二楼 D23 号

TEL: 029-81022619 13072977981 FAX:029-88789382