

DATA SHEET

PMBF107

**N-channel enhancement mode
vertical D-MOS transistor**

Product specification
File under Discrete Semiconductors, SC13b

April 1995

N-channel enhancement mode vertical D-MOS transistor

PMBF107

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

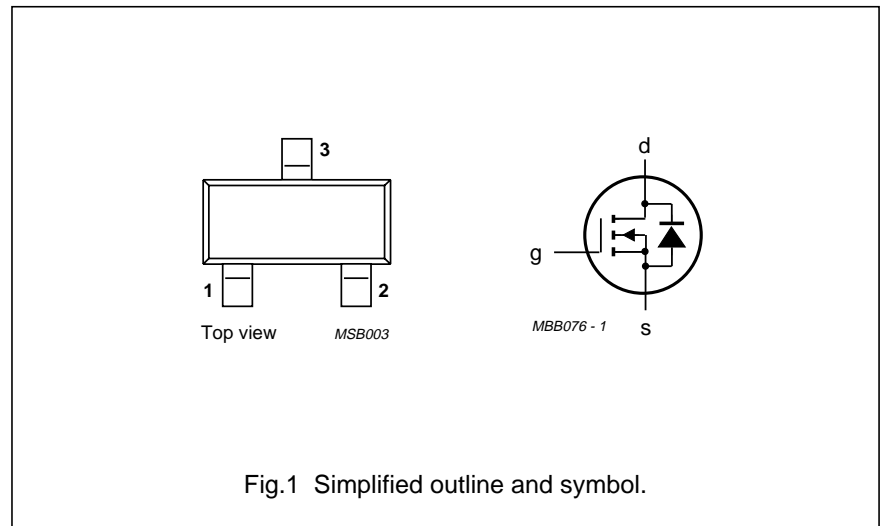
PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		200	V
I_D	drain current	DC value	100	mA
$R_{DS(on)}$	drain-source on-resistance	$I_D = 20 \text{ mA}$ $V_{GS} = 2.6 \text{ V}$	28	Ω
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ $V_{GS} = V_{DS}$	2.4	V

PIN CONFIGURATION



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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	100	mA
I_{DM}	drain current	peak value	–	250	mA
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$ (note 1)	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an FR4 printboard.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient (note 1)	500	K/W

Note

1. Device mounted on an FR4 printboard.

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CHARACTERISTICS $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\ \mu\text{A}$ $V_{GS} = 0$	200	–	–	V
I_{DSS}	drain-source leakage current	$V_{DS} = 130\ \text{V}$ $V_{GS} = 0$	–	–	30	nA
I_{DSX}	drain cut-off current	$V_{DS} = 70\ \text{V}$ $V_{GS} = 0.2\ \text{V}$	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 15\ \text{V}$ $V_{DS} = 0$	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$ $V_{GS} = V_{DS}$	0.8	–	2.4	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 20\ \text{mA}$ $V_{GS} = 2.6\ \text{V}$	–	20	28	Ω
		$I_D = 150\ \text{mA}$ $V_{GS} = 10\ \text{V}$	–	14	–	Ω
$ Y_{fs} $	transfer admittance	$I_D = 250\ \text{mA}$ $V_{DS} = 15\ \text{V}$	90	180	–	mS
C_{iss}	input capacitance	$V_{DS} = 10\ \text{V}$ $V_{GS} = 0$ $f = 1\ \text{MHz}$	–	50	65	pF
C_{oss}	output capacitance	$V_{DS} = 10\ \text{V}$ $V_{GS} = 0$ $f = 1\ \text{MHz}$	–	16	25	pF
C_{rss}	feedback capacitance	$V_{DS} = 10\ \text{V}$ $V_{GS} = 0$ $f = 1\ \text{MHz}$	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$I_D = 250\ \text{mA}$ $V_{DD} = 50\ \text{V}$ $V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	2	10	ns
t_{off}	turn-off time	$I_D = 200\ \text{mA}$ $V_{DD} = 50\ \text{V}$ $V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	5	20	ns

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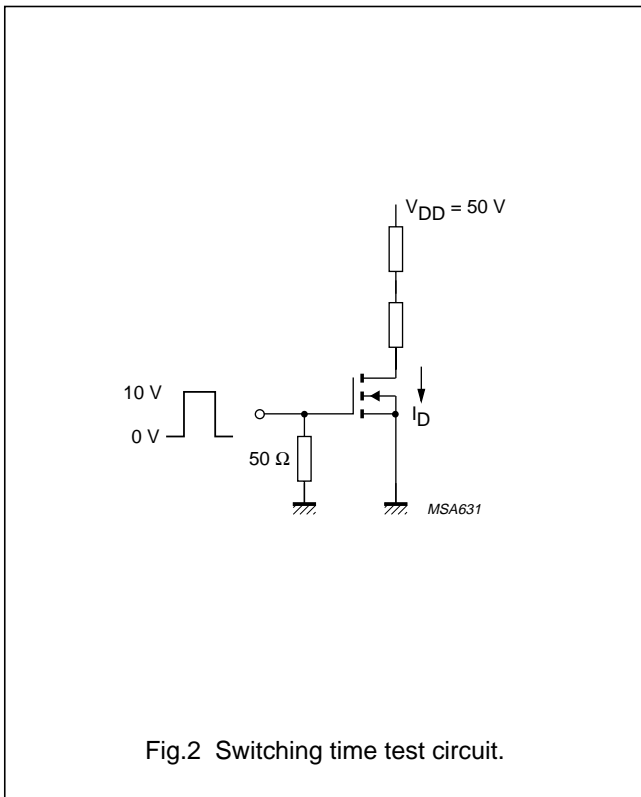


Fig.2 Switching time test circuit.

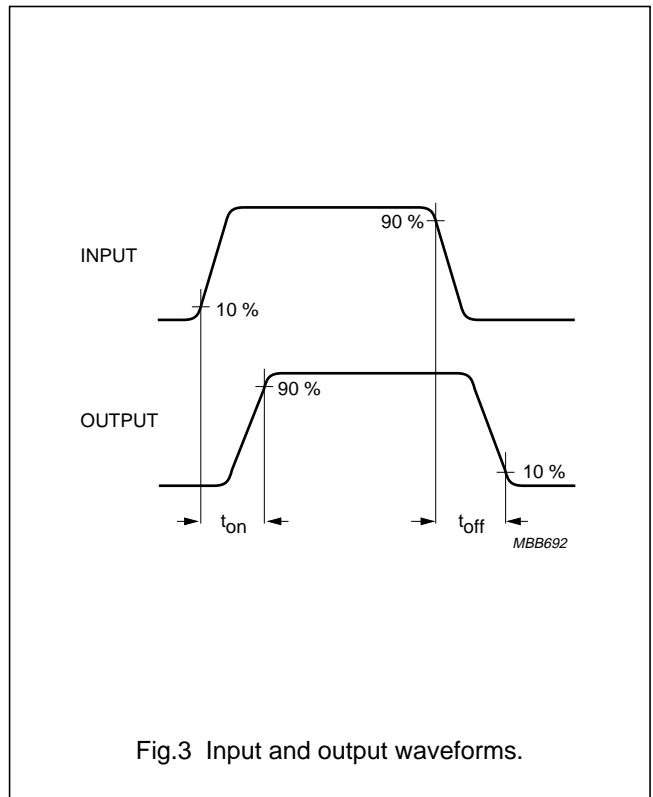


Fig.3 Input and output waveforms.

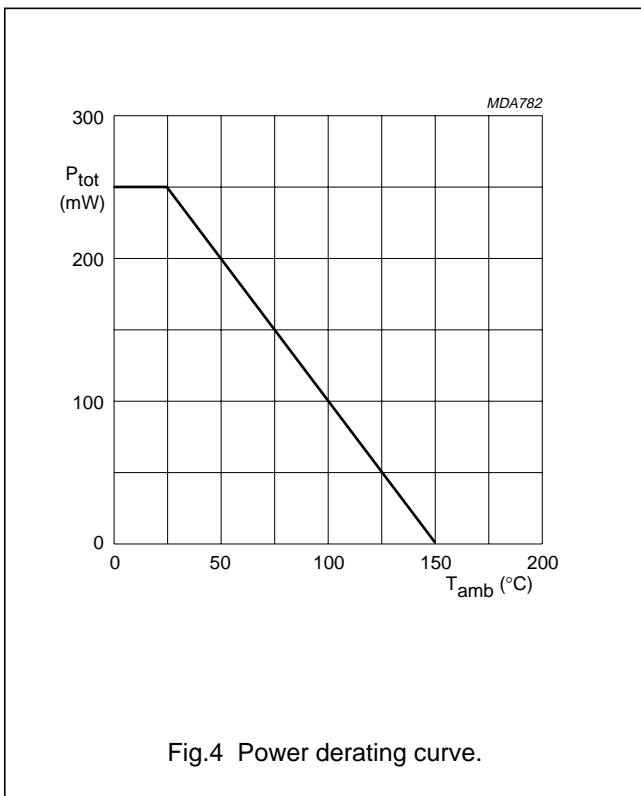


Fig.4 Power derating curve.

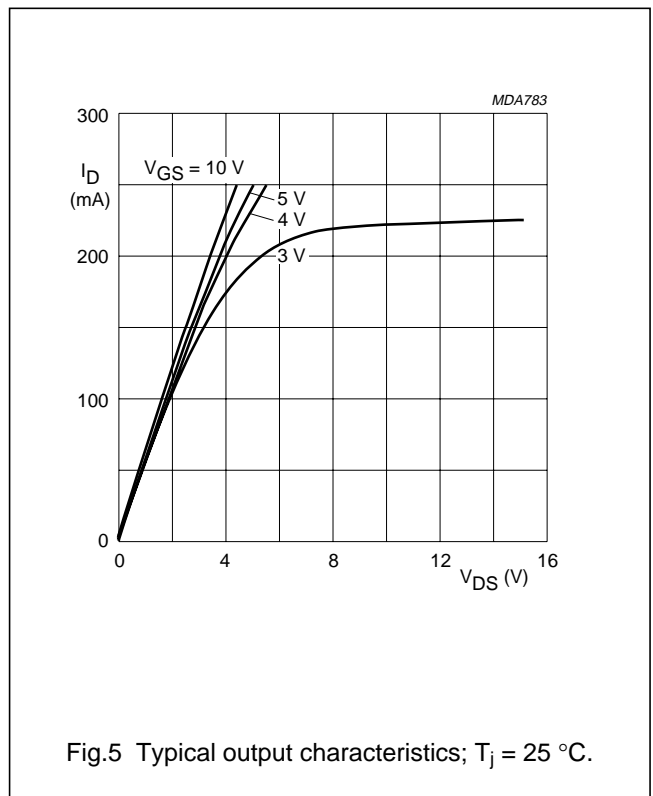
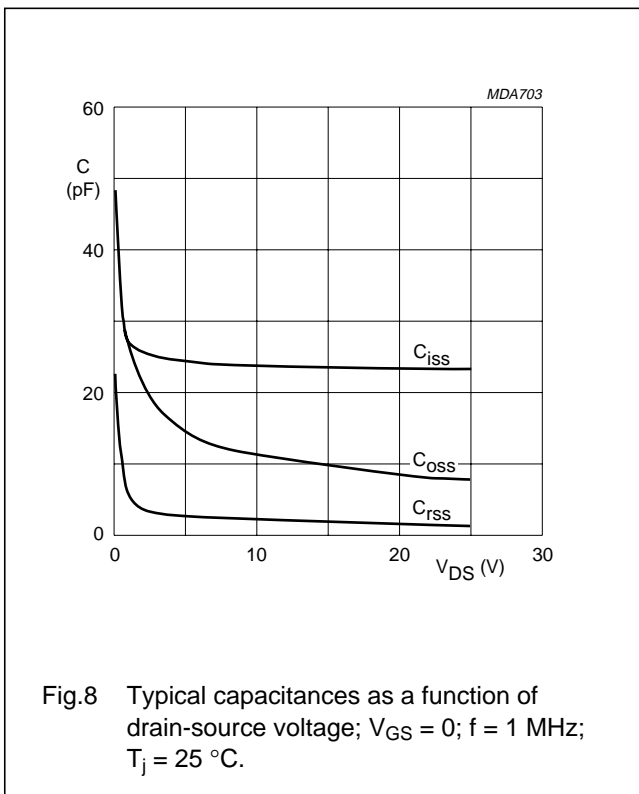
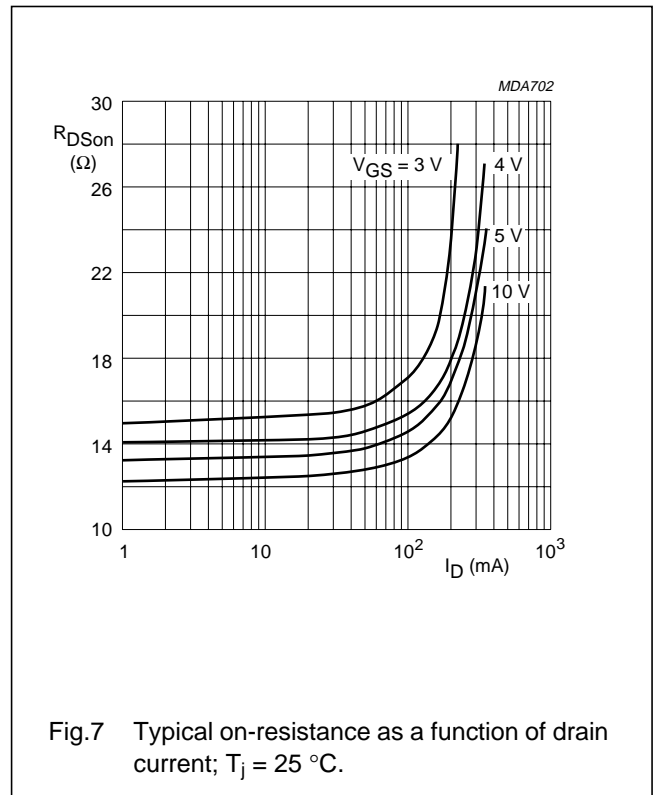
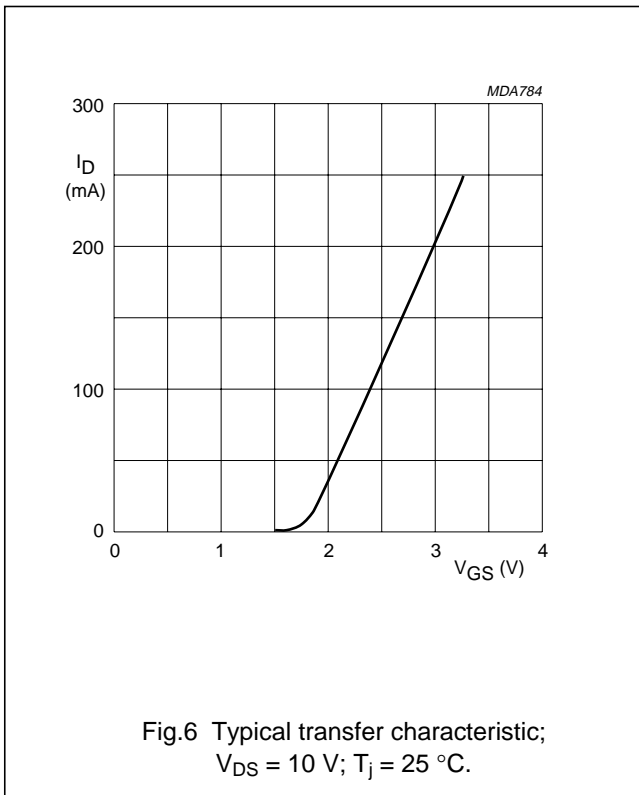


Fig.5 Typical output characteristics; T_j = 25 °C.

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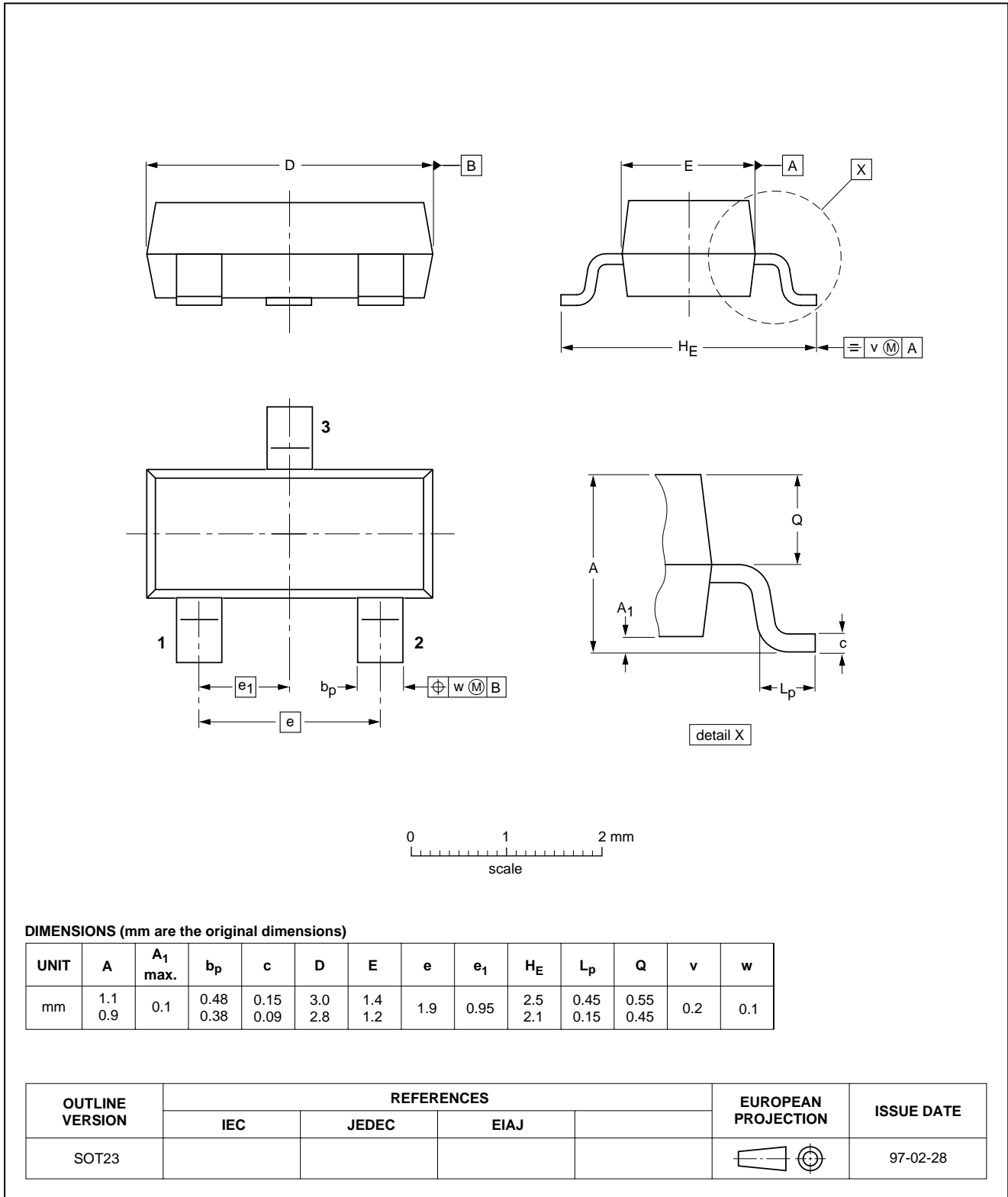
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PACKAGE OUTLINES

Plastic surface mounted package; 3 leads

SOT23



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PMBF107**DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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