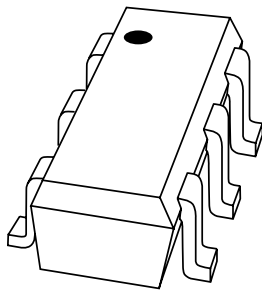


DATA SHEET



PUMB4 PNP resistor-equipped double transistor

Product specification
Supersedes data of 1998 Aug 03

1999 Apr 12

PNP resistor-equipped double transistor

PUMB4

FEATURES

- Transistors with built-in bias resistor R1 (typ. 10 kΩ)
- No mutual interference between the transistors
- Simplification of circuit design
- Reduces number of components and board space.

APPLICATIONS

- Especially suitable for space reduction in interface and driver circuits
- Inverter circuit configurations without use of external resistors.

DESCRIPTION

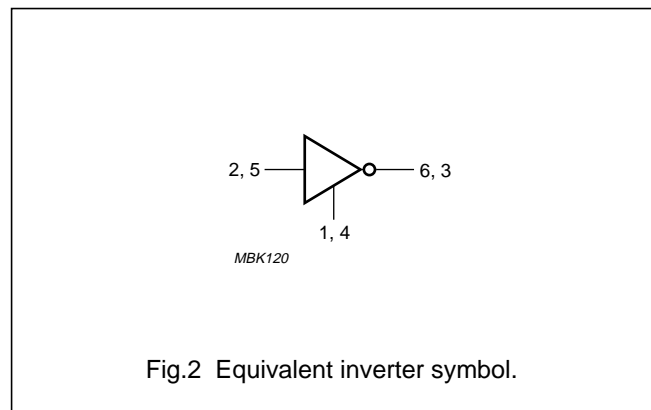
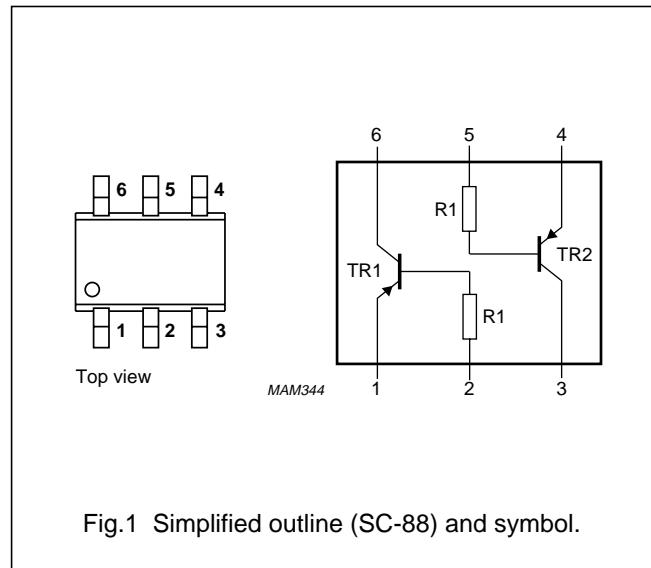
PNP resistor-equipped double transistor in an SC-88 plastic package.

MARKING

TYPE NUMBER	MARKING CODE
PUMB4	Bt4

PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2



PNP resistor-equipped double transistor

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor					
V _{CBO}	collector-base voltage	open emitter	–	–50	V
V _{CEO}	collector-emitter voltage	open base	–	–50	V
V _{EBO}	emitter-base voltage	open collector	–	–5	V
I _O	output current (DC)		–	–100	mA
I _{CM}	peak collector current		–	–100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	300	mW

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	note 1	416	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

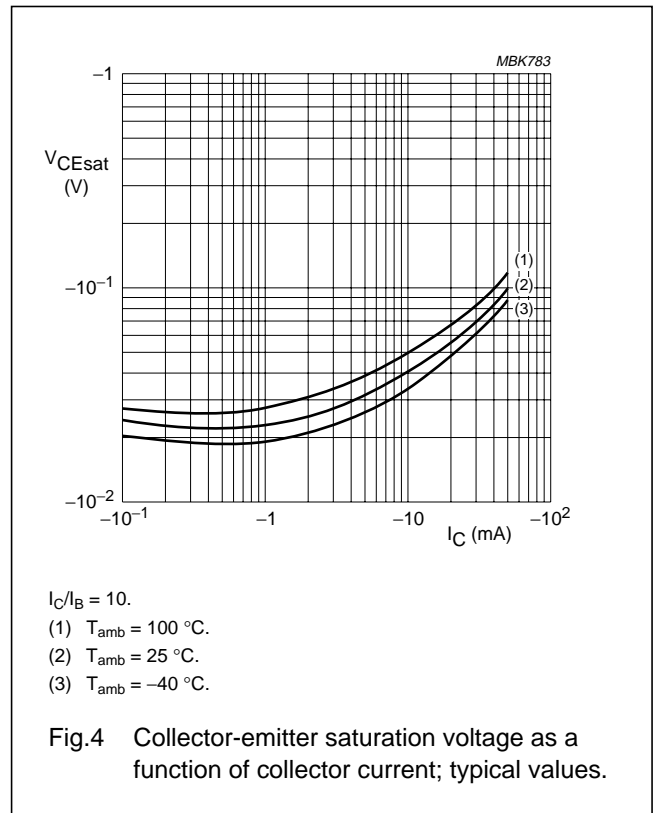
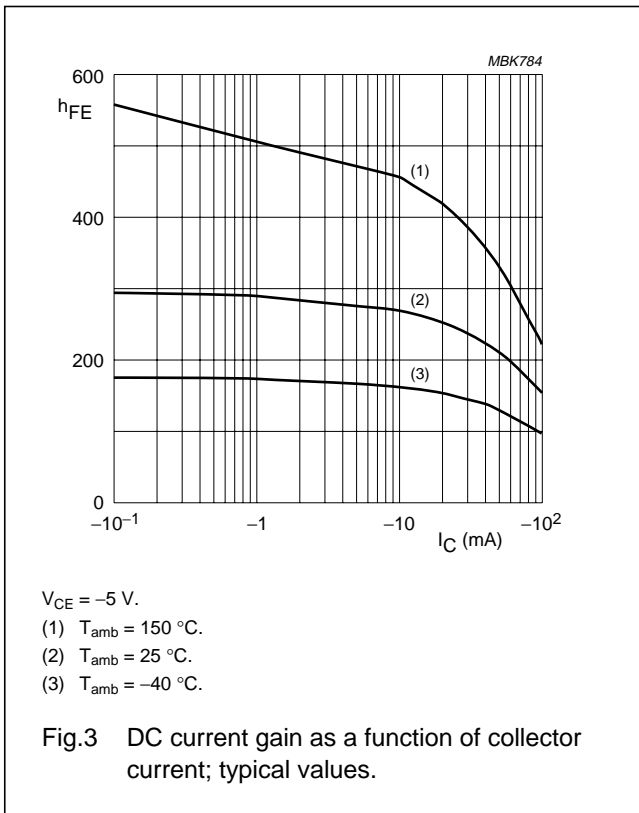
CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor						
I _{CBO}	collector cut-off current	I _E = 0; V _{CB} = –50 V	–	–	–100	nA
I _{CEO}	collector cut-off current	I _B = 0; V _{CE} = –30 V	–	–	–1	μA
		I _B = 0; V _{CE} = –30 V; T _j = 150 °C	–	–	–50	μA
I _{EBO}	emitter cut-off current	I _C = 0; V _{EB} = –5 V	–	–	–100	nA
h _{FE}	DC current gain	I _C = –1 mA; V _{CE} = –5 V	200	–	–	
V _{CEsat}	collector-emitter saturation voltage	I _C = –10 mA; I _B = –0.5 mA	–	–	–150	mV
R1	input resistor		7	10	13	kΩ
C _c	collector capacitance	I _E = i _e = 0; V _{CB} = –10 V; f = 1 MHz	–	–	3	pF

PNP resistor-equipped double transistor

PUMB4



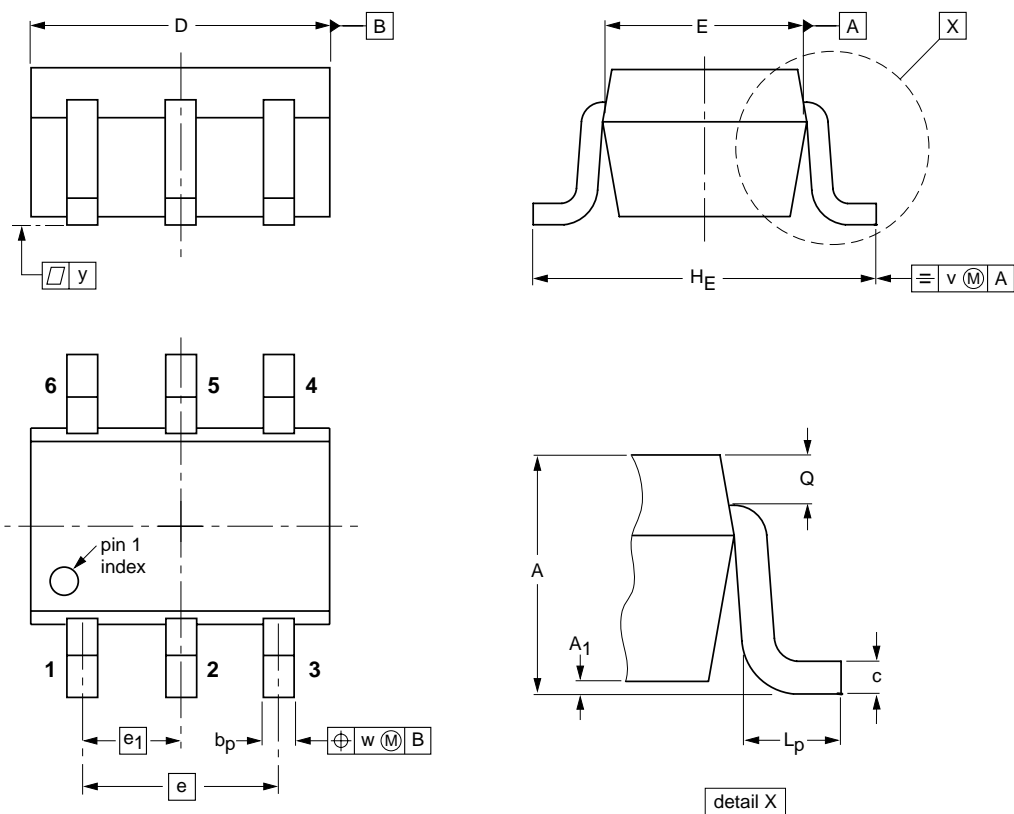
PNP resistor-equipped double transistor

PUMB4

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

PNP resistor-equipped double transistor

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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PNP resistor-equipped double transistor

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