DATA SHEET

SAA5284
Multimedia video data acquisition circuit

Objective specification
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PHILIPS

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1 FEATURES

- High performance multi-standard data slicer
- **Intercast™ (Intel Corporation) compatible**
- Teletext (WST, Chinese teletext) (625 lines)
- Teletext (US teletext, NABTS and MOJI) (525 lines)
- Wide Screen Signalling (WSS), Video Programming Signal (VPS)
- Closed Caption (Europe, US)
- Data broadcast, PDC (packet 30 and 31)
- User programmable data format (programmable framing code)
- 2 kbytes data cache on-chip to avoid data loss and reduce host CPU overhead
- Filtering of packets 30 and 31 WST/NABTS
- Choice of clock frequencies, direct-in clock or crystal oscillator
- Parallel interface, Motorola, Intel and digital video bus
- I²C-bus control
- Data transport by digital video bus
- Choice of programmable interrupt, DMA or polling driven
- Data type selectable video line by video line, with Vertical Blanking Interval and Full Field mode
- Single IC with few external components and small footprint QFP44 package
- Optimized for EMC.

2 GENERAL DESCRIPTION

The SAA5284 is a Vertical Blanking Interval (VBI) and Full Field (FF) video data acquisition device tailored for application on PC add-in cards, PC mother-boards, set-top boxes and as a SAA5250 replacement. The IC in combination with a range of software modules will acquire most existing formats of broadcast VBI and FF data.

These associated software modules are available under licence. Scope is provided for acquiring some as yet unspecified formats. The SAA5284 incorporates all the data slicing, parallel interface, data filtering and control logic. It is controlled either by a parallel interface or I²C-bus. It can output ASCII VBI data as pixels on the digital video bus where no parallel port is available. It is available in a QFP44 package.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	72	95	mA
$V_{sync(p-p)}$	sync voltage (peak-to-peak value)	0.1	0.3	0.6	V
$V_{i(CVBS)(p-p)}$	input voltage on pin CVBS0 and CVBS1 (peak-to-peak value)	0.7	1.0	1.4	V
f_{xtal}	crystal frequency; see note 1	–	12.0	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

Note

1. Selectable: 12, 13.5, 15 or 16 MHz.

4 ORDERING INFORMATION

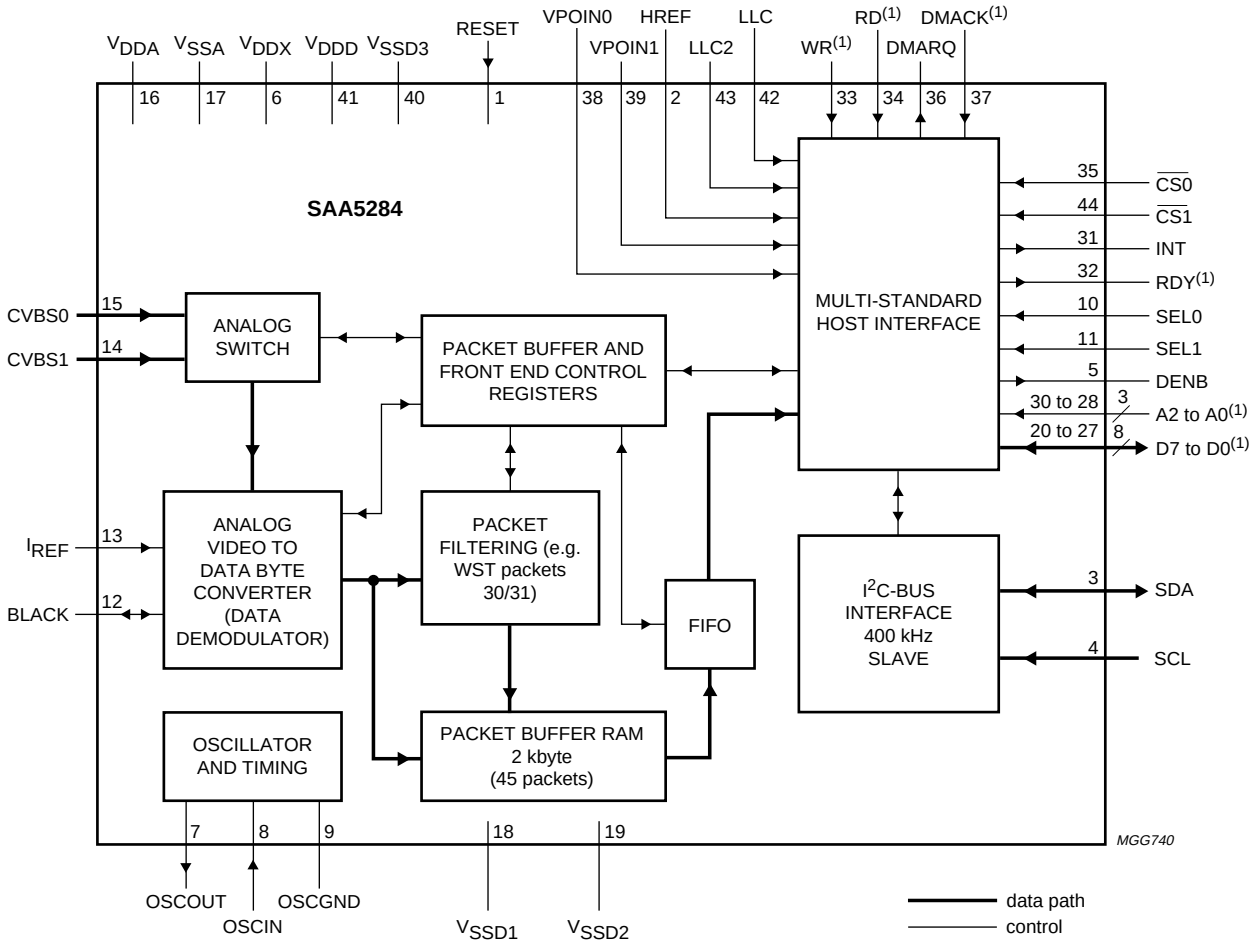
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5284GP	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1

5 MAIN FUNCTIONAL BLOCKS

1. Input clamp and sync separator
2. Analog-to-digital converter
3. Multi-standard data slicer and clock regenerator
4. Packet filtering; (8 and 4) Hamming correction
5. On-chip data cache
6. Line selectable data type
7. 12, 13.5, 15 and 16 MHz clock or oscillator options
8. FIFO access to data
9. Interrupt and DMA support
10. Multi-standard parallel interface
11. I²C-bus interface
12. Power-on reset.

Figure 1 shows a block diagram of the SAA5284.

6 BLOCK DIAGRAM

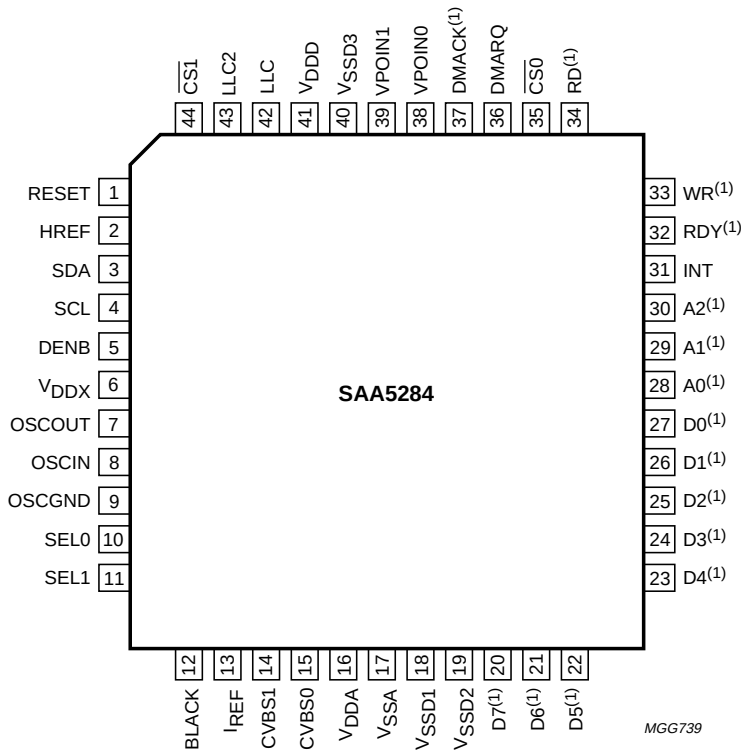


(1) Multi-functional pins, see Chapter 7.

Fig.1 Block diagram.

7 PINNING INFORMATION

7.1 Pinning



(1) Multi-functional pin.

Fig.2 Pin configuration.

7.2 Pin description

Table 1 QFP44 package

The IC has a total of 44 pins; many of these are multi-functional due to the multiple host block modes of operation.

SYMBOL	PIN	I/O	DESCRIPTION
RESET	1	I	reset IC
HREF	2	I	video horizontal reference signal (digital video mode only)
SDA	3	I/O	serial data port for I^2C-bus, open-drain
SCL	4	I	serial clock input for I^2C-bus
DENB	5	O	data enable bar (for external buffers)
V_{DDX}	6	–	+5 V supply
OSCOUT	7	O	oscillator output
OSCIN	8	I	oscillator input

SYMBOL	PIN	I/O	DESCRIPTION
OSCGND	9	–	oscillator ground
SEL0	10	I	parallel interface format select 0
SEL1	11	I	parallel interface format select 1
BLACK	12	I/O	video black level storage; connected to V_{SSA} via 100 nF capacitor
I_{REF}	13	I	reference current input; connected to V_{SSA} via 27 kΩ resistor
CVBS1	14	I	analog composite video input 1
CVBS0	15	I	analog composite video input 0
V_{DDA}	16	–	analog +5 V supply
V_{SSA}	17	–	analog ground supply
V_{SSD1}	18	I	digital ground supply 1
V_{SSD2}	19	I	digital ground supply 2
D7(1)	20	I/O	data bus 7/video data output 7
D6(1)	21	I/O	data bus 6/video data output 6
D5(1)	22	I/O	data bus 5/video data output 5
D4(1)	23	I/O	data bus 4/video data output 4
D3(1)	24	I/O	data bus 3/video data output 3
D2(1)	25	I/O	data bus 2/video data output 2
D1(1)	26	I/O	data bus 1/video data output 1
D0(1)	27	I/O	data bus 0/video data output 0
A0(1)	28	I	address input 0/video data input 7
A1(1)	29	I	address input 1/video data input 6
A2(1)	30	I	address input 2/video data input 5
INT	31	O	interrupt request
RDY(1)	32	O	ready/DTACK (data acknowledge)/VBI, open-drain
WR(1)	33	I	Intel bus Write/Motorola bus R/$\overline{W}$/video data input 4
RD(1)	34	I	Intel bus Read/Motorola bus LDS/video data input 3
$\overline{CS0}$	35	I	chip select 0; active LOW
DMARQ	36	O	DMA request
DMACK(1)	37	I	DMA acknowledge/video data input 2
VPOIN0	38	I	video data input 0
VPOIN1	39	I	video data input 1
V_{SSD3}	40	–	digital ground supply 3
V_{DDD}	41	–	digital +5 V supply
LLC	42	I	full rate digital video clock input
LLC2	43	I	half rate digital video clock input
$\overline{CS1}$	44	I	chip select 1; active LOW

Note

1. These pins have two functions, depending on the interface mode.

8 FUNCTIONAL DESCRIPTION

8.1 Power supply strategy

There are three separate +5 V (V_{DD}) connections to the IC:

1. V_{DDA} supplies the critical noise-sensitive analog front-end sections: ADC and sync separator, to reduce interference from the rest of the front-end
2. V_{DDX} supplies all sections which take standing DC current
3. V_{DDD} supplies the rest of the logic.

8.2 Clocking strategy

The master frequency reference for the IC is a 12, 13.5, 15 or 16 MHz crystal oscillator. The tolerance on the clock frequency is 500×10^{-6} (1.5 kHz). Further specifications of the crystal are given in Table 2.

If preferred, an external 12, 13.5, 15 or 16 MHz (±1.5 kHz) frequency source may be connected to OSCIN instead of the crystal.

8.3 Power-on reset

The RESET pin should be held HIGH for a minimum of two clock cycles. The reset signal is passed through a Schmitt trigger internally.

Direct addressed registers (i.e. those addressed using the A0 to A2 pins) are set to 00H after power-up. All other register bits are assumed to be in random states after power-up.

8.4 Analog switch

Register bit selection between two video sources.

8.5 Analog video-to-data byte converter

This section comprises a line and field sync separator, a video clamp, an ADC and a custom adaptive digital filter with DPLL based timing circuit.

The analog video-to-data byte converter is specifically designed to overcome the most commonly found types of distortion of a broadcast video signal. It is also fully multi-standard. The data type to be demodulated is programmable on a line-by-line basis using 4 register bits per line for lines 2 to 23 (PAL numbering), fields 1 and 2, and 4 further bits for all lines combined.

8.6 Packet filtering

If using a slow (e.g. 80C51) microcontroller, it is necessary to reduce the amount of data acquired by SAA5284 before downloading to the microcontroller to avoid it being swamped by unwanted data. Packet filtering is available for this purpose. A common use of this would be to acquire only packet 8/30 in 625-line WST. The packet filter includes optional (8, 4) Hamming correction.

8.7 Packet buffer

This is a 2 kbyte RAM which acts as a buffer for storing received packets. The first 44 bytes are reserved for control information. The rest of the RAM is divided into 44-byte rows (or packets), each holding the data received on one incoming CVBS line. In the case of a WST packet received, the data stored consists of a Magazine and Row-Address Group (2 bytes), followed by the 40 bytes of packet data. When data in other formats than WST is received, this is stored in the packet buffer in the same way. In each case, the data is preceded by two information bytes which record on which line and field the packet was received, and what the data type is.

8.8 FIFO

FIFO hardware is provided to manage the ‘read’ address for the host processor, i.e. data is read repeatedly from the same 8-bit port, and appears byte-serially in the order of reception. The read address can be reset to the start of the packet buffer (the first 44-byte packet), back to the start of the current packet, or incremented to the start of the next packet.

Table 2 Crystal characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C1	series capacitance	–	18.5	–	fF
C2	parallel capacitance	–	4.9	–	pF
R_r	resonant resistance	–	–	50	Ω
X_a	ageing	–	–	5×10^{-6}	per year
X_j	adjustment tolerance	–	–	25×10^{-6}	–
X_d	drift	–	–	25×10^{-6}	–

8.9 Host interface

The SAA5284 has a multi-standard 8-bit I/O interface. To reduce the amount of host I/O space used, the parallel interface has only 3 address inputs (A0, A1 and A2). An extended addressing (pointer) scheme and the data FIFO are used to allow access to the full set of SAA5284 registers and the full span of the packet buffer.

As well as the 8 data I/O lines and 3 address lines, there are the following control signals: RD (read LOW), WR (write LOW), $\overline{CS0}$ (chip select LOW), $\overline{CS1}$(second chip select LOW), INT (interrupt request), DMARQ (DMA request), DMACK (DMA acknowledge) and RDY (ready).

In order to maintain compatibility with Motorola and Intel type buses, two control signals SEL0 and SEL1 are provided to configure the host interface. These signals allow configuration of the host interface to work with the Motorola or Intel style interfaces.

The host interface has a digital video mode. Digital video mode may be used to allow the SAA5284 to pass decoded VBI data into a system using the digital video bus.

8.10 Interrupt support

The host interface provides comprehensive support for interrupt generation. The interrupt may be programmed to occur when a particular number of packets of VBI data are available in the cache RAM. The interrupts can be further controlled to occur on a specific line in the TV frame. The interrupts can also be self masking if required.

8.11 DMA support

Burst and demand mode DMA are supported. In burst mode, the number of packets to transfer can be defined. An interrupt can be generated when DMA is finished. This can be self masking.

8.12 I^2C-bus interface

The I^2C-bus interface functions as a slave receiver or transmitter at up to 400 kHz. The I^2C-bus address is selectable as 20H or 22H. All functionality is available using the I^2C-bus although with a slower data transfer speed. It is possible to use the I^2C-bus in all modes.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	–0.3	+6.5	V
$V_{I(max)}$	input voltage (any input)	–0.3	V_{DD} + 0.5	V
$V_{O(max)}$	output voltage (any output)	–0.3	V_{DD} + 0.5	V
$\Delta V_{DDD–DDA–DDX}$	supply voltage difference between V_{DDD}, V_{DDA} and V_{DDX}	–	0.25	V
I_{IOK}	DC input or output diode current	–	20	mA
$I_{O(max)}$	output current (any output)	–	10	mA
T_{stg}	storage temperature	–55	+125	°C
T_{amb}	operating ambient temperature	–20	+70	°C

10 QUALITY & RELIABILITY

In accordance with *“SNW-FQ-611-E”*.

11 CHARACTERISTICS

T_{amb} = −20 to +70 °C; V_{DD} = 4.5 to 5.5 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supply						
V_{DDn}	supply voltage		4.5	5.0	5.5	V
$I_{DD(tot)}$	total supply current		–	72	95	mA
I_{DDD}	digital supply current		–	32	42	mA
I_{DDA}	analog supply current		–	40	53	mA
Inputs CVBS0 and CVBS1						
$V_{sync(p-p)}$	sync voltage (peak-to-peak value)		0.1	0.3	0.6	V
$V_{burst(p-p)}$	colour burst voltage (peak-to-peak value)		0	0.3	0.4	V
$V_{i(vid)(p-p)}$	video input voltage (peak-to-peak value)		0.7	1.0	1.4	V
$V_{i(data)(p-p)}$	teletext data input voltage (peak-to-peak value)		0.29	0.46	0.71	V
Z_{source}	source impedance		–	–	250	Ω
$V_{i(sw)}$	input switching level of sync separator		1.5	1.8	2.1	V
Z_i	input impedance		2.5	5.0	–	kΩ
C_i	input capacitance		–	–	10	pF
Input I_{REF}						
R_{IREF}	external resistor to V_{SSA}		–	27	–	kΩ
Inputs RESET, HREF, SEL0, SEL1, A0, A1, A2, WR, RD, $\overline{CS0}$, $\overline{CS1}$, DMACK, VPOIN1, VPOIN0, LLC and LLC2						
V_{IL}	LOW-level input voltage		−0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_i = 0 to V_{DD}	−10	–	+10	µA
C_i	input capacitance		–	–	10	pF
Input SCL						
V_{IL}	LOW-level input voltage		−0.5	–	+1.5	V
V_{IH}	HIGH-level input voltage		3.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_i = 0 to V_{DD}	−10	–	+10	µA
C_i	input capacitance			–	10	pF
$t_{i(r)}$	input rise time	$V_{IL(min)}$ to $V_{IH(max)}$; $f_{i(SCL)}$ = 100 kHz	50	–	1000	ns
		$V_{IL(min)}$ to $V_{IH(max)}$; $f_{i(SCL)}$ = 400 kHz	50	–	300	ns
$t_{i(f)}$	input fall time	$V_{IL(max)}$ to $V_{IH(min)}$; $f_{i(SCL)}$ = 100 kHz	50	–	300	ns
		$V_{IL(max)}$ to $V_{IH(min)}$; $f_{i(SCL)}$ = 400 kHz	50	–	300	ns
$f_{i(SCL)}$	input clock frequency		0	–	400	kHz
C_L	load capacitance		–	–	400	pF

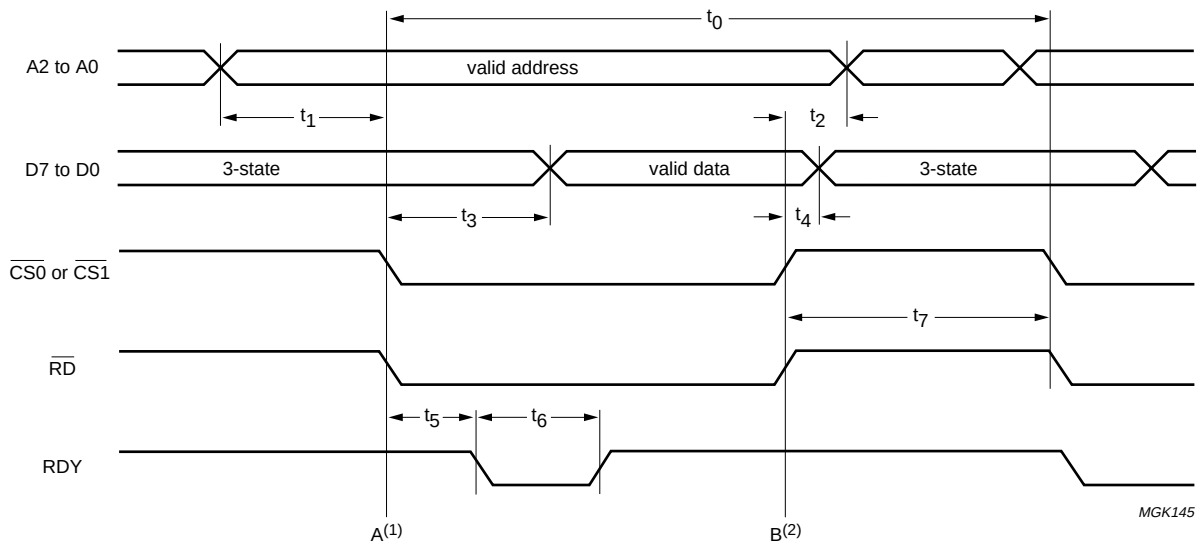
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input/output SDA (open-drain)						
V_{IL}	LOW-level input voltage		–0.5	–	+1.5	V
V_{IH}	HIGH-level input voltage		3.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_i	input capacitance			–	10	pF
$t_{i(r)}$	input rise time	$V_{IL(min)}$ to $V_{IH(max)}$; $f_{i(SCL)}$ = 100 kHz	50	–	1000	ns
		$V_{IL(min)}$ to $V_{IH(max)}$; $f_{i(SCL)}$ = 400 kHz	50	–	300	ns
$t_{i(f)}$	input fall time	$V_{IL(max)}$ to $V_{IH(min)}$; $f_{i(SCL)}$ = 100 kHz	50	–	300	ns
		$V_{IL(max)}$ to $V_{IH(min)}$; $f_{i(SCL)}$ = 400 kHz	50	–	300	ns
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	0	–	0.4	V
		I_{OL} = 6 mA	0	–	0.6	V
$t_{o(f)}$	output fall time	between 3 and 1.5 V; I_{OL} = 3 mA	50	–	250	ns
C_L	load capacitance		–	–	400	pF
Input/output BLACK						
C_{BLACK}	storage capacitance to V_{SSA}		–	100	–	nF
Inputs/outputs D7 to D0						
V_{IL}	LOW-level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	V_{IN} = 0 to V_{DD}	–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW-level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	tbf	pF
$t_{o(r)}$	output rise time into C_L	0.6 to 2.2 V	–	–	tbf	ns
$t_{o(f)}$	output fall time into C_L	2.2 to 0.6 V	–	–	tbf	ns
Outputs INT, DENB and DMARQ						
V_{OL}	LOW-level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –0.2 mA	2.4	–	V_{DD}	V
C_L	load capacitance		–	–	tbf	pF
$t_{o(r)}$	output rise time into C_L	0.6 to 2.2 V	–	–	tbf	ns
$t_{o(f)}$	output fall time into C_L	2.2 to 0.6 V	–	–	tbf	ns
RDY (open-drain); note 1						
V_{OL}	LOW-level output voltage	I_{OL} = +1.6 mA	0	–	0.4	V
C_L	load capacitance		–	–	tbf	pF
$t_{o(r)}$	output rise time into C_L	0.6 to 2.2 V	–	–	tbf	ns
$t_{o(f)}$	output fall time into C_L	2.2 to 0.6 V	–	–	tbf	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2C-bus timings (see note 2 and Fig.8)						
$f_{i(SCL)}$	SCL input clock frequency	$f_{i(SCL)}$ = 100 kHz	0	–	100	kHz
		$f_{i(SCL)}$ = 400 kHz	0	–	400	kHz
t_{LOW}	SCL LOW time	$f_{i(SCL)}$ = 100 kHz	4.7	–	–	µs
		$f_{i(SCL)}$ = 400 kHz	1.3	–	–	µs
t_{HIGH}	SCL HIGH time	$f_{i(SCL)}$ = 100 kHz	4.0	–	–	µs
		$f_{i(SCL)}$ = 400 kHz	0.6	–	–	µs
$t_{SU;DAT}$	data set-up time	$f_{i(SCL)}$ = 100 kHz	250	–	–	ns
		$f_{i(SCL)}$ = 400 kHz	100	–	–	ns
$t_{HD;DAT}$	data hold time	$f_{i(SCL)}$ = 100 kHz	0	–	–	µs
		$f_{i(SCL)}$ = 400 kHz	0	–	–	µs
$t_{SU;STO}$	set-up time STOP condition	$f_{i(SCL)}$ = 100 kHz	4.7	–	–	µs
		$f_{i(SCL)}$ = 400 kHz	0.6	–	–	µs
t_{BUF}	bus free time	$f_{i(SCL)}$ = 100 kHz	4.7	–	–	µs
		$f_{i(SCL)}$ = 400 kHz	1.3	–	–	µs
$t_{HD;STA}$	hold time START condition	$f_{i(SCL)}$ = 100 kHz	4.0	–	–	µs
		$f_{i(SCL)}$ = 400 kHz	0.6	–	–	µs
$t_{SU;STA}$	set-up time repeated START	$f_{i(SCL)}$ = 100 kHz	4.7	–	–	µs
		$f_{i(SCL)}$ = 400 kHz	0.6	–	–	µs
t_r	rise time (SDA and SCL)	$f_{i(SCL)}$ = 100 kHz	–	–	1000	ns
		$f_{i(SCL)}$ = 400 kHz	–	–	300	ns
t_f	fall time (SDA and SCL)	$f_{i(SCL)}$ = 100 kHz	–	–	300	ns
		$f_{i(SCL)}$ = 400 kHz	–	–	300	ns

Notes

1. ESD protection of this pin falls below the Philips General Quality Specification (GQS). Therefore it is recommended that a diode is connected from pin RDY to V_{DDD}.
2. The I^2C-bus interface pins SDA and SCL may pull the data and clock lines below 3 V while the digital power supply V_{DDD} is in the range 0.4 to 0.8 V.

12 TIMING

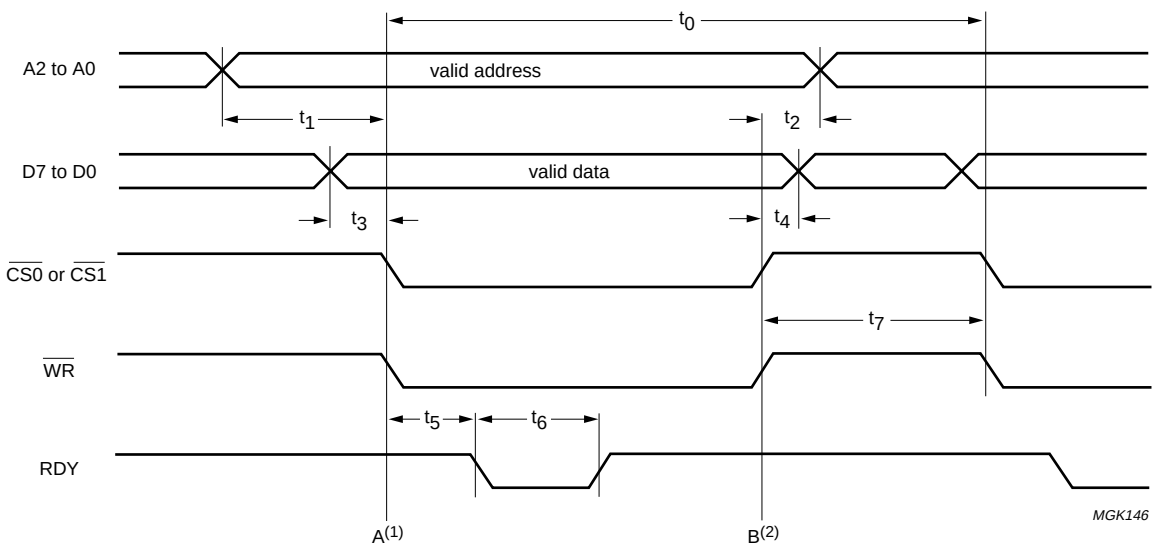


(1) Event A occurs when $\overline{RD} + \overline{CS0} + \overline{CS1} = 0$ (boolean).
(2) Event B occurs when $\overline{RD} + \overline{CS0} + \overline{CS1} = 1$ (boolean).

Fig.3 Intel mode interface read cycle timing.

Table 3 Intel-mode interface read cycle timing (12 MHz clock)

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
t_0	minimum cycle time	333	833	ns
t_1	address set-up time before event A	0	–	ns
t_2	address hold time after event B	0	–	ns
t_3	data settling time	88	712	ns
t_4	data hold time after event B	0	–	ns
t_5	time from event A until RDY goes LOW	83	170	ns
t_6	RDY LOW time	83	530	ns
t_7	event B to next event A time	83	–	ns



(1) Event A occurs when $\overline{WR}$ + $\overline{CS0}$ + $\overline{CS1}$ = 0 (boolean).
(2) Event B occurs when $\overline{WR}$ + $\overline{CS0}$ + $\overline{CS1}$ = 1 (boolean).

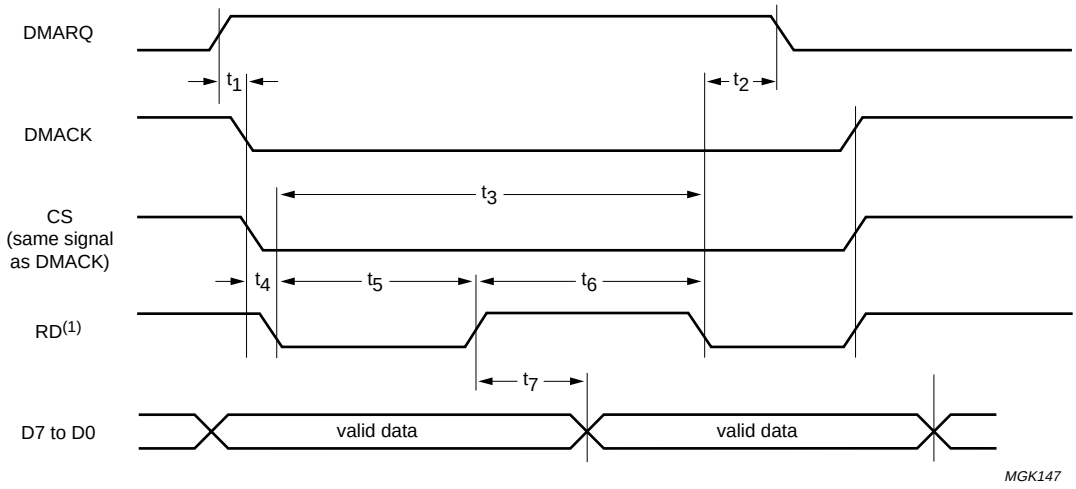
Fig.4 Intel mode interface write cycle timing.

Table 4 Intel-mode interface write cycle timing (12 MHz clock)

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
t_0	minimum cycle time	333	833	ns
t_1	address set-up time	0	–	ns
t_2	address hold time	0	–	ns
t_3	data set-up time, note 1	0	–	ns
t_4	data hold time	0	–	ns
t_5	RDY set-up time	83	170	ns
t_6	RDY LOW time	83	530	ns
t_7	event B to next event A time	83	–	ns

Note

1. Legacy AT bus PCs may not satisfy this requirement as they are not ISA compatible. An application fix is available in the *"SAA5284 Users Guide"*.



(1) Read data pipelined, so no RD LOW to data valid set-up time.

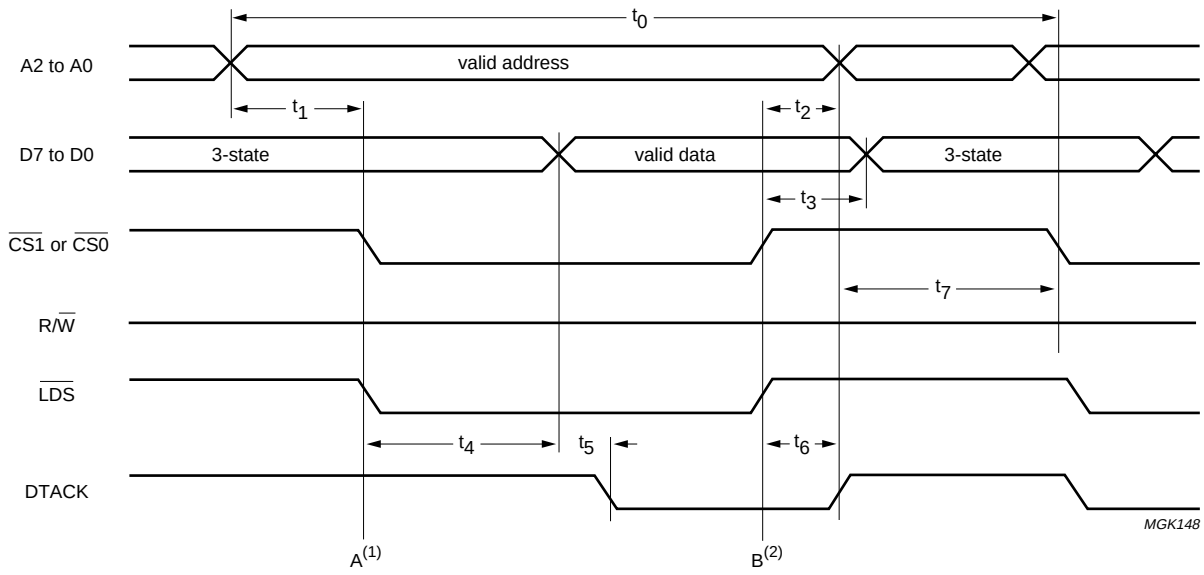
Fig.5 Intel mode interface DMA cycle timing.

Table 5 Intel-mode interface DMA cycle timing (12 MHz clock)

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
t_1	DMARQ to DMACK	0	–	ns
t_2	RD LOW to DMARQ LOW	0	212	ns
t_3	cycle time	252	–	ns
t_4	DMACK to RD active	–	0	ns
t_5	data set-up time	0	90(1)	ns
t_6	data hold time	83	–	ns
t_7	data hold from DMACK HIGH	0	83	ns

Note

1. This timing will be up to 3 clock cycles for the first read in DMA transfer.

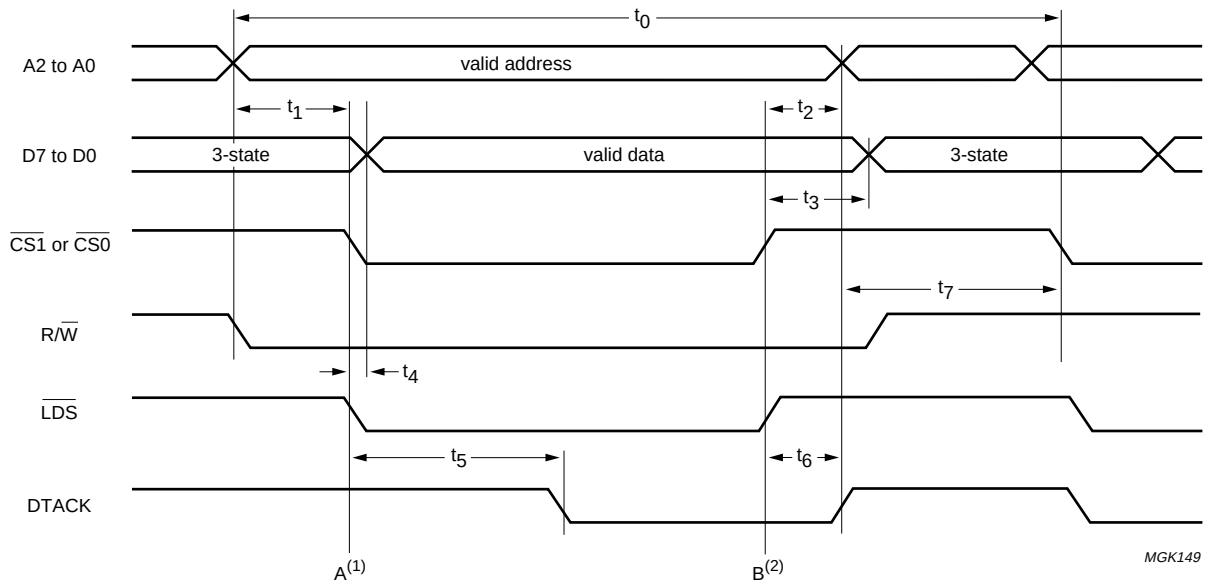


(1) Event A occurs when $\overline{LDS} + \overline{CS0} + \overline{CS1} = 0$ (boolean).
(2) Event B occurs when $\overline{LDS} + \overline{CS0} + \overline{CS1} = 1$ (boolean).

Fig.6 Motorola mode interface read cycle timing.

Table 6 Motorola-mode interface read cycle timing (12 MHz clock)

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
t_0	minimum cycle time	333	833	ns
t_1	address set-up time before event A	0	–	ns
t_2	address hold time after event B	0	–	ns
t_3	data hold time from event B	0	–	ns
t_4	data settling time	88	712	ns
t_5	data valid to DTACK LOW	83	170	ns
t_6	$\overline{LDS}$ HIGH to DTACK HIGH	83	212	ns
t_7	delay between cycles	83	–	ns



(1) Event A occurs when $\overline{LDS} + \overline{CS0} + \overline{CS1} = 0$ (boolean).
(2) Event B occurs when $\overline{LDS} + \overline{CS0} + \overline{CS1} = 1$ (boolean).

Fig.7 Motorola mode interface write cycle timing.

Table 7 Motorola-mode interface write cycle timing (12 MHz clock)

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
t_0	minimum cycle time	333	417	ns
t_1	address set-up time before event A	0	–	ns
t_2	address hold time after event B	0	–	ns
t_3	data hold time from event B	0	–	ns
t_4	data set-up time	0	–	ns
t_5	DTACK set-up time	–	212	ns
t_6	$\overline{LDS}$ HIGH to DTACK HIGH	83	212	ns
t_7	delay between cycles	83	–	ns

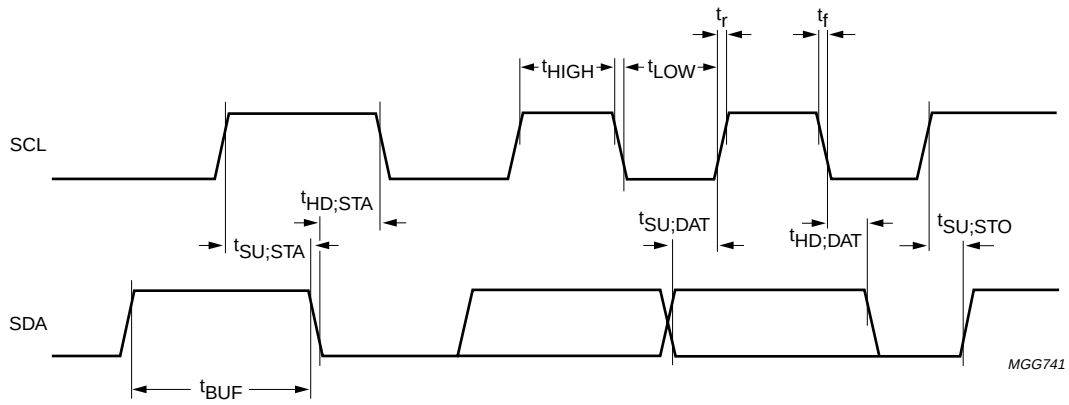


Fig.8 I^2C-bus timing diagram.

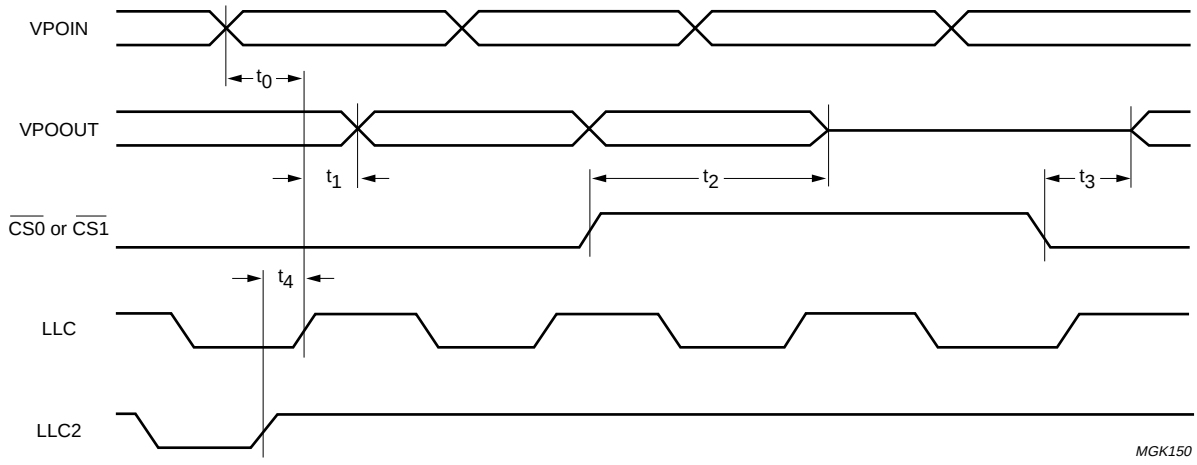


Fig.9 Digital video mode interface timing.

Table 8 Digital video mode interface timing with 13.5 MHz clock and 27 MHz LLC

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
t_0	VPOIN set-up time	4	5	6	ns
t_1	VPOOUT set-up time	8	10	22	ns
t_2	$\overline{CS}$ HIGH to VPOOUT 3-state	6	10	25	ns
t_3	$\overline{CS}$ LOW to VPOOUT enabled	9	11	16	ns
t_4	clock qualifier set-up time	–	1.1	–	ns

13 APPLICATION INFORMATION

13.1 Hardware application circuit for ISA card

A typical application circuit diagram (for the ISA card application) is shown in Fig.10.

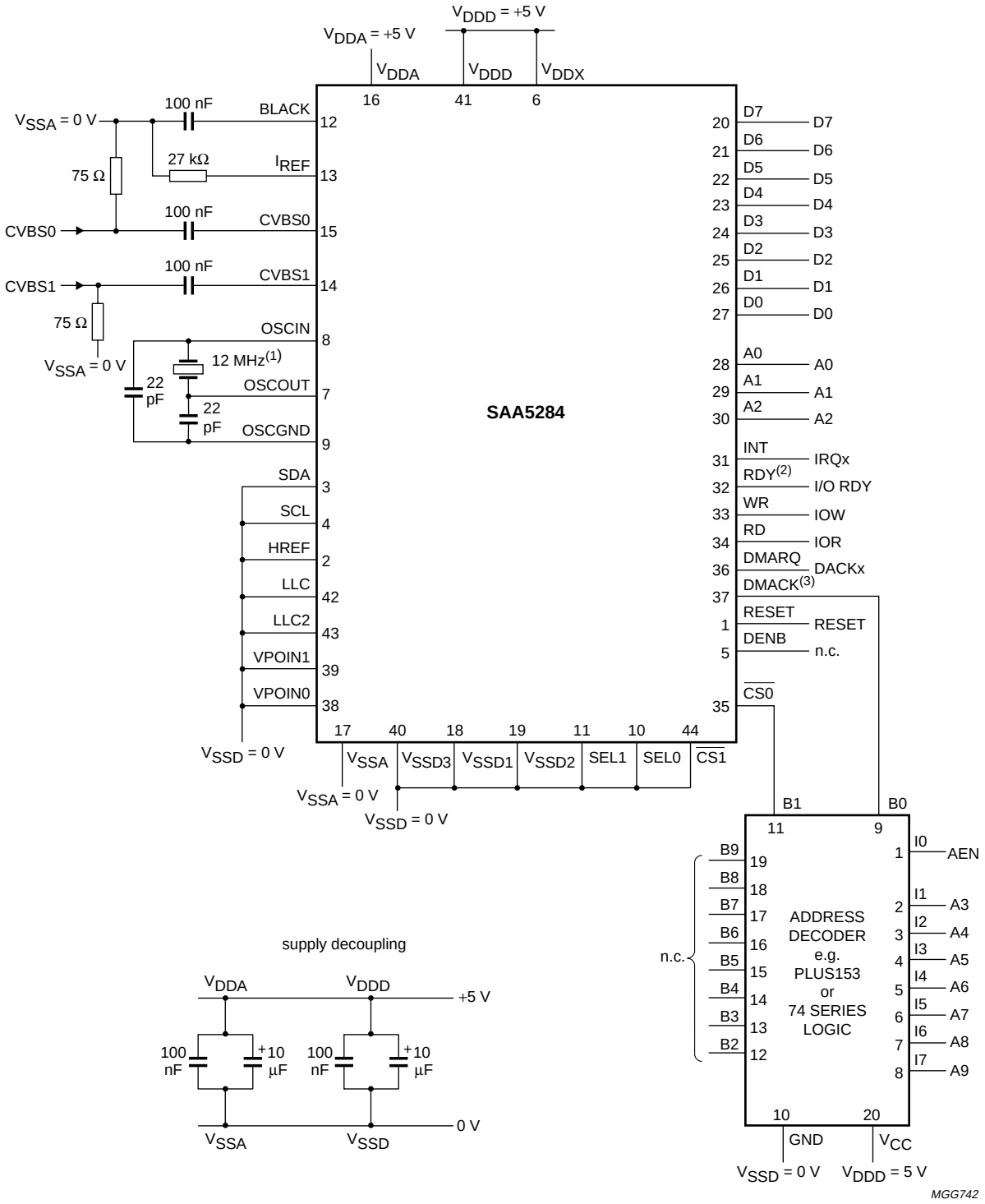
13.2 Hardware application circuit for PCI application

This PCI application is based around the Philips SAA7146 video to PCI bridge IC. SAA7146 has a ‘Data Expansion Bus Interface’ (DEBI) which is an Intel/Motorola style 16-bit parallel interface. This is used to facilitate communications to SAA5284.

The application circuit diagram is shown in Fig.11.

13.3 Software application information

PC application software is available providing two levels of interface. At a low level a VxD based driver offers generic packet gathering and buffering. Full support is provided for ISA based applications with facility for PCI based applications. Higher level support is provided by a series of DLLs. These perform normal teletext display generation and page management.



(1) Option of 13.5, 15 and 16 MHz or direct feed from external clock.

(2) A diode to V_{DDD} is recommended for ESD protection.

(3) Pin DMACK must be connected to V_{DDD} if DMA is not used.

Fig.10 Application circuit diagram for ISA card.

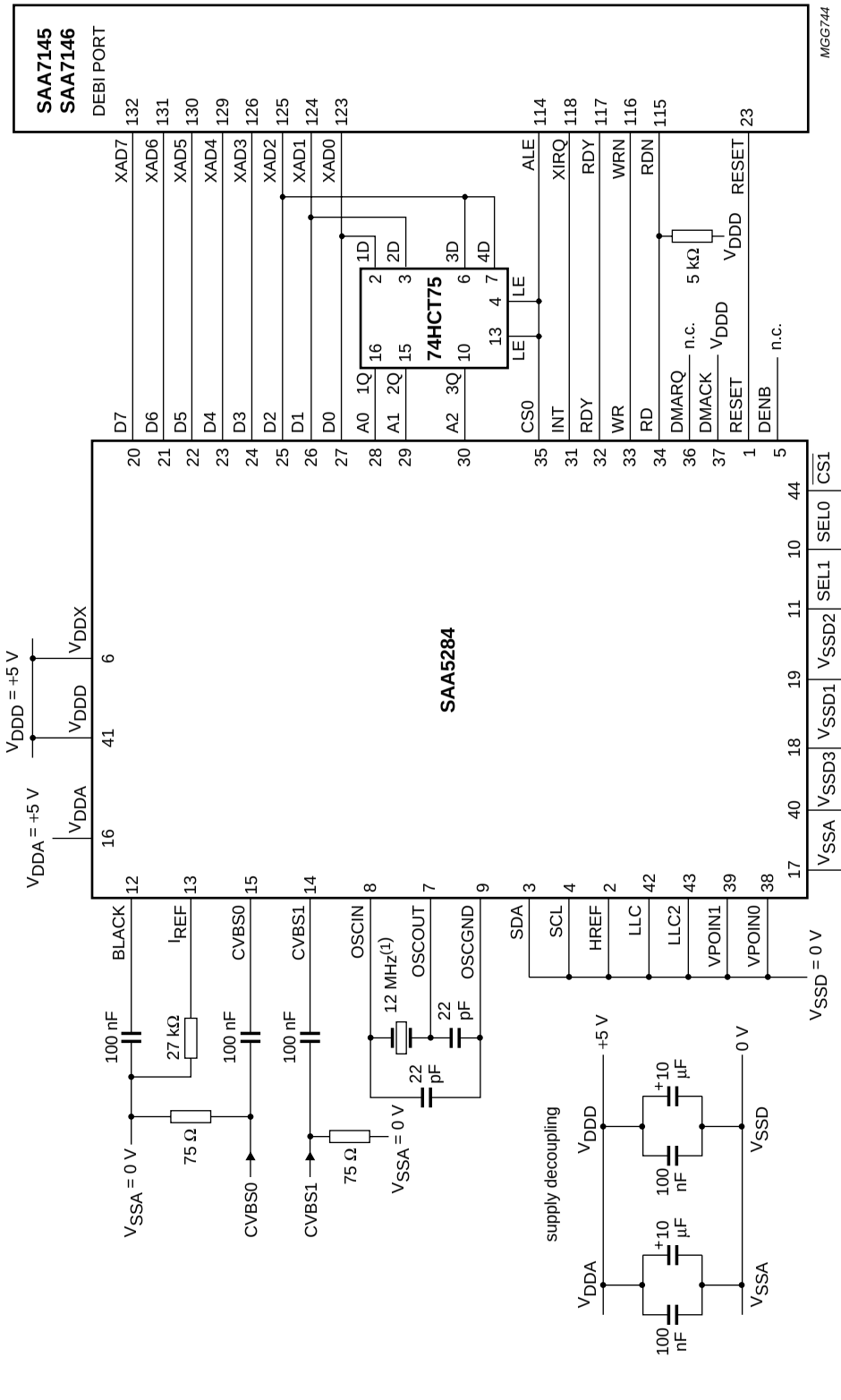
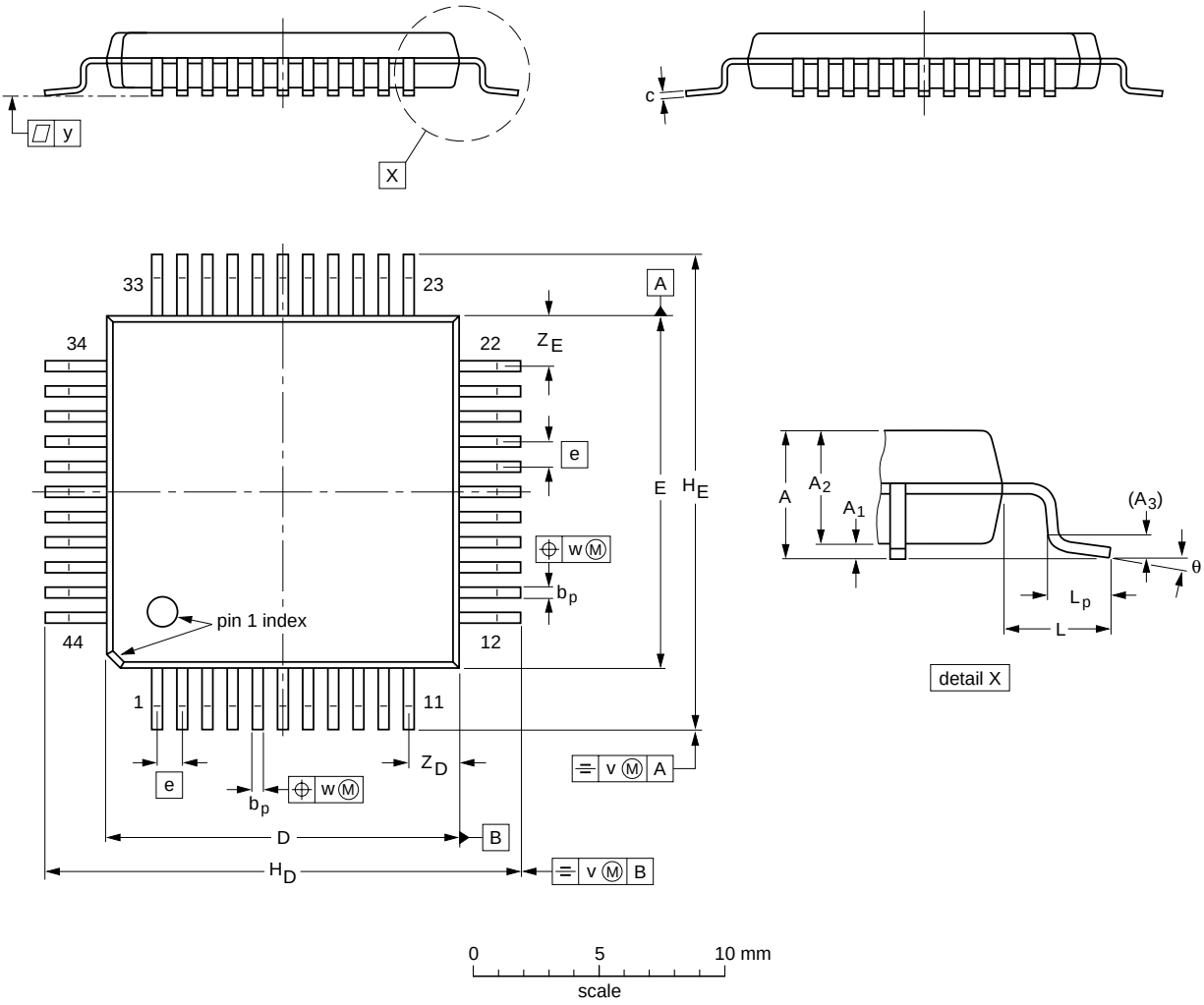


Fig.11 Application circuit diagram for PCI application.

(1) Option of 13.5, 15 and 16 MHz or LLC2 from the SAA7111 if in 13.5 MHz mode.

14 PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm **SOT205-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~95-02-04~~ 97-08-01

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

15.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

15.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

17 LIFE SUPPORT APPLICATIONS

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