DATA SHEET

SAA8115HL
Digital camera USB interface IC

Preliminary specification
File under Integrated Circuits, IC22

1999 Jun 28

Philips
Semiconductors

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Digital camera USB interface IC SAA8115HL

FEATURES

- VGA (progressive mode), CIF and medium resolution (PAL non-interlaced mode) CCD sensors compliant
- D1 digital video input (8 bits YUV 4 : 2 : 2, time multiplexed)
- Internal Pulse Pattern Generator (PPG) dedicated for VGA Panasonic, CIF and medium resolution Sharp sensors or compatibles, and frame rate selection
- Frame rate converter
- SDRAM interface for high quality VGA snapshot (uncompressed 4 : 2 : 2)
- Downsampler and scaler (programmable formatter for CIF, QCIF, sub-QCIF, SIF and QSIF) controlled via SNERT (UART) interface
- Flexible compression engine controlled via SNERT (UART) interface
- Selectable output frame rate (up to 15 fps in VGA, up to 30 fps in CIF and QCIF)
- Video packetizer FIFO
- I^2C-bus interface for communication between the USB protocol hardware and the external microcontroller
- Microphone/audio input to USB (microphone supply, controllable gain and ADC)
- Integrated analog bus driver (ATX)
- Integrated main oscillator
- Integrated 5 V power and reset circuit including functions for bus-powered USB device
- Miscellaneous functions e.g. power management, PLL for audio frequencies.

APPLICATIONS

Low-cost desktop video applications with USB interface.

GENERAL DESCRIPTION

The SAA8115HL is the second generation of an integrated circuit applicable in PC video cameras to convert D1 video signals and analog audio signals to properly formatted USB packets.

This powerful successor of the SAA8117HL can handle up to 15 fps in VGA format or 30 fps in CIF format. High snapshot quality is achieved by using the SDRAM interface to an external memory.

It is designed as a back-end of the SAA8112HL (general camera digital processing IC) and is optimized for use with the TDA8784 to TDA8787 (camera pre-processing ICs).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA8115HL	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

QUICK REFERENCE DATA

Measured over full voltage and temperature range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
$V_{DDA(USB)}$	analog supply voltage from USB	note 1	4.0	5.0	5.5	V
$I_{DD(tot)}$	total supply current	V_{DDD} = 3.3 V	–	tbf	–	mA
V_I	input signal levels	3.0 V < V_{DDD} < 3.6 V	low voltage TTL compatible			V
V_O	output signal levels	3.0 V < V_{DDD} < 3.6 V	low voltage TTL compatible			V
f_{clk}	clock frequency		–	48	–	MHz
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	tbf	–	mW
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	ambient temperature		0	25	70	°C
T_j	junction temperature	T_{amb} = 70 °C	–40	–	+125	°C

Note

1. This concerns pins VBUS1 and VBUS2 (pins 90 and 91).

BLOCK DIAGRAM

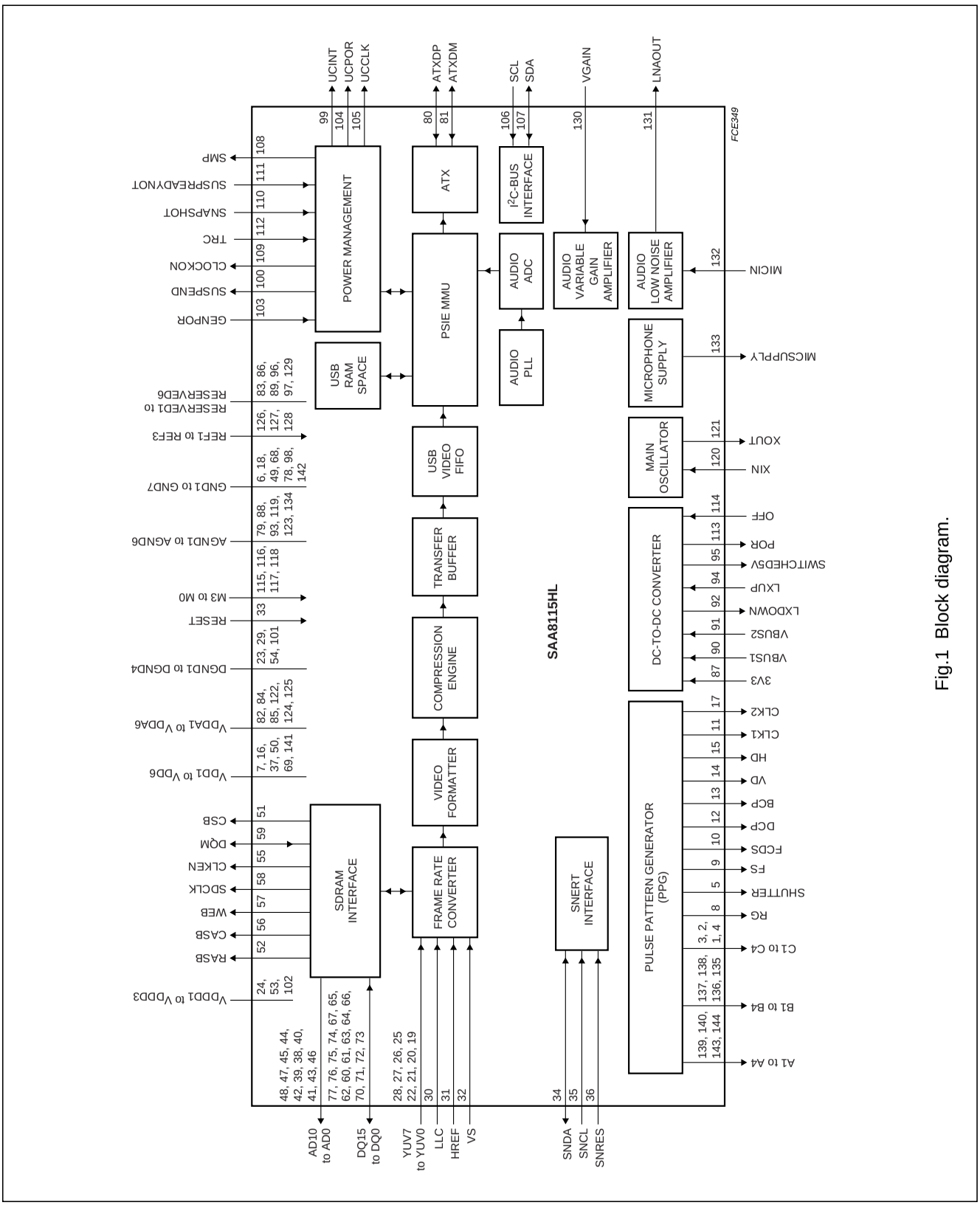


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
C3	1	O	horizontal CCD transfer pulse output
C2	2	O	horizontal CCD transfer pulse output (FH1)
C1	3	O	horizontal CCD transfer pulse output (FH2)
C4	4	O	horizontal CCD transfer pulse output
SHUTTER	5	O	shutter control output for CCD charge reset
GND1	6	P	ground 1 for output buffers
V_{DD1}	7	P	supply voltage 1 for output buffers
RG	8	O	reset output for CCD output amplifier gate
FS	9	O	data sample-and-hold pulse output to TDA8784/87 (SHD)
FCDS	10	O	preset sample-and-hold pulse output to TDA8784/87 (SHP)
CLK1	11	O	pixel clock output to TDA8784/87and SAA8112HL
DCP	12	O	dummy clamp pulse output to TDA8784/86
BCP	13	O	optical black clamp pulse output to TDA8784/86
VD	14	O	vertical definition pulse output to SAA8112HL
HD	15	O	horizontal definition pulse output to SAA8112HL
V_{DD2}	16	P	supply voltage 2 for output buffers
CLK2	17	O	double pixel clock output to SAA8112HL
GND2	18	P	ground 2 for output buffers
YUV0	19	I	multiplexed input YUV bit 0
YUV1	20	I	multiplexed input YUV bit 1
YUV2	21	I	multiplexed input YUV bit 2
YUV3	22	I	multiplexed input YUV bit 3
DGND1	23	P	digital ground 1 for input buffers, predrivers and for the digital core
V_{DDD1}	24	P	digital supply voltage 1 for input buffers, predrivers and one part of the digital core
YUV4	25	I	multiplexed input YUV bit 4
YUV5	26	I	multiplexed input YUV bit 5
YUV6	27	I	multiplexed input YUV bit 6
YUV7	28	I	multiplexed input YUV bit 7
DGND2	29	P	digital ground 2 for input buffers, predrivers and for the digital core
LLC	30	I	line-locked clock input (delayed CLK2) for YUV-port from SAA8112HL
HREF	31	I	horizontal reference input for YUV-port from SAA8112HL
VS	32	I	vertical synchronization input for YUV-port from SAA8112HL
RESET	33	I	Power-on reset input (for video processing and PPG)
SNDA	34	I/O	data input/output for SNERT-interface (communication between SAA8115HL and SAA8112HL)
SNCL	35	I	clock input for SNERT-interface (communication between SAA8115HL and SAA8112HL)
SNRES	36	I	reset input for SNERT-interface (communication between SAA8115HL and SAA8112HL)
V_{DD3}	37	P	supply voltage 3 for output buffers

SYMBOL	PIN	TYPE	DESCRIPTION
AD4	38	O	SDRAM output address bit 4
AD5	39	O	SDRAM output address bit 5
AD3	40	O	SDRAM output address bit 3
AD2	41	O	SDRAM output address bit 2
AD6	42	O	SDRAM output address bit 6
AD1	43	O	SDRAM output address bit 1
AD7	44	O	SDRAM output address bit 7
AD8	45	O	SDRAM output address bit 8
AD0	46	O	SDRAM output address bit 0
AD9	47	O	SDRAM output address bit 9
AD10	48	O	SDRAM output address bit 10
GND3	49	P	ground 3 for output buffers
V_{DD4}	50	P	supply voltage 4 for output buffers
CSB	51	O	SDRAM chip select output
RASB	52	O	SDRAM row address strobe output
V_{DDD2}	53	P	digital supply voltage 2 for the switchable digital core
DGND3	54	P	digital ground 3 for input buffers, predrivers and for the digital core
CLKEN	55	O	SDRAM clock enable output
CASB	56	O	SDRAM column address strobe output
WEB	57	O	SDRAM write enable output
SDCLK	58	O	SDRAM clock output
DQM	59	I/O	SDRAM data input/output mask enable
DQ8	60	I/O	SDRAM data I/O bit 8
DQ7	61	I/O	SDRAM data I/O bit 7
DQ9	62	I/O	SDRAM data I/O bit 9
DQ6	63	I/O	SDRAM data I/O bit 6
DQ5	64	I/O	SDRAM data I/O bit 5
DQ10	65	I/O	SDRAM data I/O bit 10
DQ4	66	I/O	SDRAM data I/O bit 4
DQ11	67	I/O	SDRAM data I/O bit 11
GND4	68	P	ground 4 for output buffers
V_{DD5}	69	P	supply voltage 5 for output buffers
DQ3	70	I/O	SDRAM data I/O bit 3
DQ2	71	I/O	SDRAM data I/O bit 2
DQ1	72	I/O	SDRAM data I/O bit 1
DQ0	73	I/O	SDRAM data I/O bit 0
DQ12	74	I/O	SDRAM data I/O bit 12
DQ13	75	I/O	SDRAM data I/O bit 13
DQ14	76	I/O	SDRAM data I/O bit 14
DQ15	77	I/O	SDRAM data I/O bit 15
GND5	78	P	ground 5 for output buffers

SYMBOL	PIN	TYPE	DESCRIPTION
AGND1	79	P	analog ground 1 for ATX (transceiver)
ATXDP	80	I/O	positive driver of the differential data pair input/output (ATX)
ATXDM	81	I/O	negative driver of the differential data pair input/output (ATX)
V_{DDA1}	82	P	analog supply voltage 1 for ATX
RESERVED1	83	–	test pin 1 (should not be used)
V_{DDA2}	84	P	analog supply voltage 2 for band gap (reference)
V_{DDA3}	85	P	analog supply voltage 3 for band gap, comparator and ring oscillator
RESERVED2	86	–	test pin 2 (should not be used)
3V3	87	I	3V3 detector input signal
AGND2	88	P	analog ground 2 for N-switch
RESERVED3	89	–	test pin 3 (should not be used)
VBUS1	90	I	supply voltage input 1 from the USB
VBUS2	91	I	supply voltage input 2 from the USB
LXDOWN	92	O	LX coil node output (5 V downconverter)
AGND3	93	P	analog ground 3 for N-switch
LXUP	94	I	LX coil node input (5 V upconverter)
SWITCHED5V	95	O	5 V switched power supply
RESERVED4	96	–	test pin 4 (should not be used)
RESERVED5	97	–	test pin 5 (should not be used)
GND6	98	P	ground 6 for output buffers
UCINT	99	O	interrupt output from USB to microcontroller
SUSPEND	100	O	control output from USB protocol hardware to microcontroller
DGND4	101	P	digital ground 4 for input buffers, predrivers and for the digital core
V_{DDD3}	102	P	digital supply voltage 3 for input buffers, predrivers and one part of the digital core
GENPOR	103	I	Power-on reset input (for USB protocol hardware)
UCPOR	104	O	control output from USB protocol hardware to microcontroller
UCCLK	105	O	clock output from USB protocol hardware to microcontroller
SCL	106	I	slave I^2C-bus clock input
SDA	107	I/O	slave I^2C-bus data input/output
SMP	108	O	switch mode pulse output for CCD supplies
CLOCKON	109	O	control output for main oscillator switched on
SNAPSHOT	110	I	input for remote wake-up (snapshot)
SUSPREADYNOT	111	I	input from microcontroller for SUSPEND mode
TRC	112	I	threshold control input for enabling clock
POR	113	O	3.3 V supply domain ready indicator output
OFF	114	I	disable 5 V switchable supply domain input
M3	115	I	test mode control input signal bit 3
M2	116	I	test mode control input signal bit 2
M1	117	I	test mode control input signal bit 1
M0	118	I	test mode control input signal bit 0
AGND4	119	P	analog ground 4 for crystal oscillator (48 MHz, 3rd overtone)

SYMBOL	PIN	TYPE	DESCRIPTION
XIN	120	I	oscillator input
XOUT	121	O	oscillator output
V_{DDA4}	122	P	analog supply voltage 4 for crystal oscillator (48 MHz, 3rd overtone)
AGND5	123	P	analog ground 5 for PLL
V_{DDA5}	124	P	analog supply voltage 5 for PLL
V_{DDA6}	125	P	analog supply voltage 6 for amplifier and ADC
REF1	126	I	reference voltage 1 (used in the ADC)
REF2	127	I	reference voltage 2 (used in the ADC)
REF3	128	I	reference voltage 3 (used in the amplifier and the ADC)
RESERVED6	129	–	test pin 6 (should not be used)
VGAIN	130	I	variable gain amplifier input
LNAOUT	131	O	low noise amplifier output
MICIN	132	I	microphone input
MICSUPPLY	133	O	microphone supply output
AGND6	134	P	analog ground 6 for amplifier and ADC
B4	135	O	vertical CCD load pulse output (VH1X)
B3	136	O	vertical CCD load pulse output (VH3X)
B1	137	O	vertical CCD load pulse output
B2	138	O	vertical CCD load pulse output
A1	139	O	vertical CCD transfer pulse output (V1X)
A2	140	O	vertical CCD transfer pulse output (V2X)
V_{DD6}	141	P	supply voltage 6 for output buffers
GND7	142	P	ground 7 for output buffers
A3	143	O	vertical CCD transfer pulse output (V3X)
A4	144	O	vertical CCD transfer pulse output (V4X)

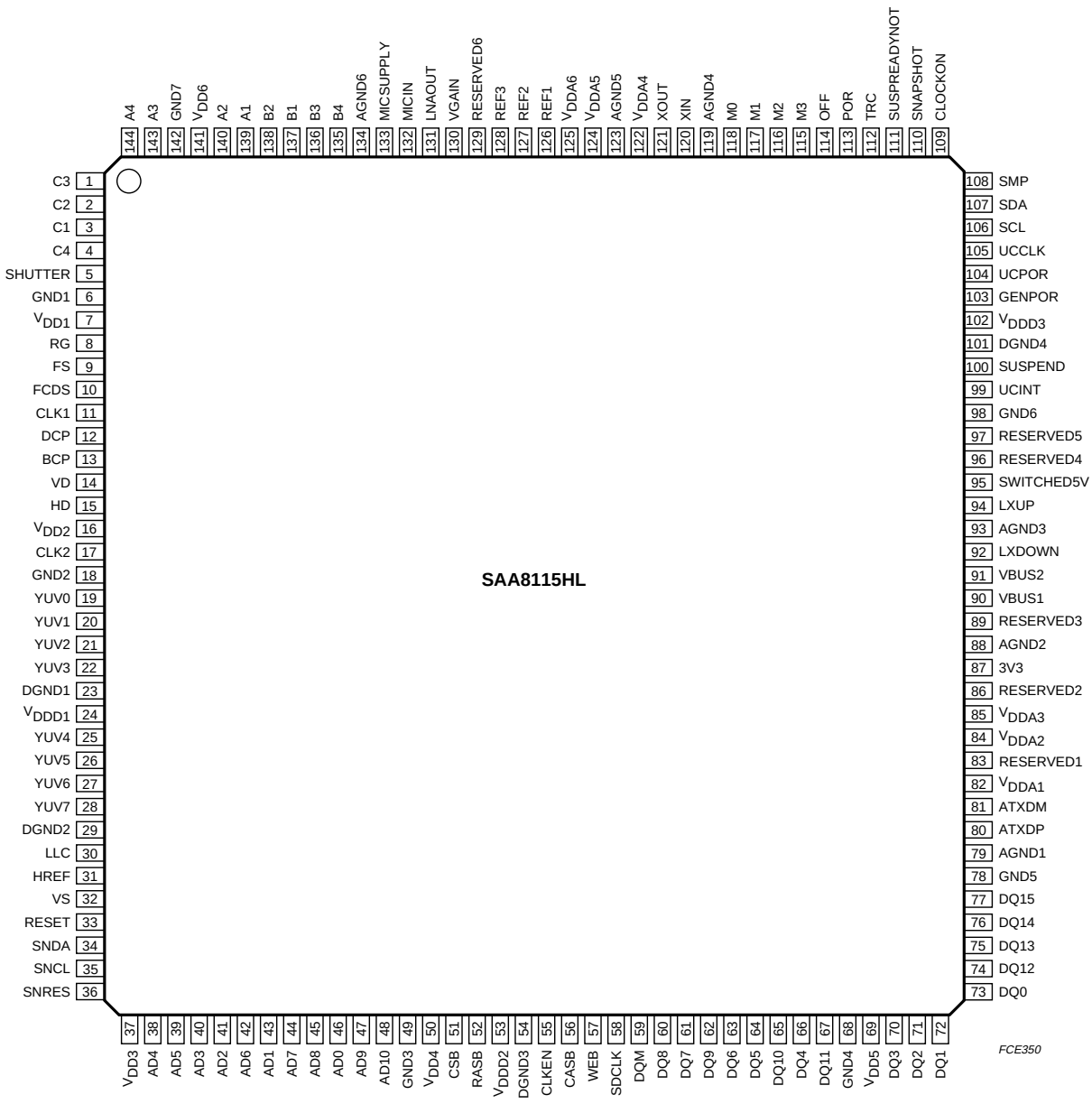


Fig.2 Pin configuration.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	45	K/W

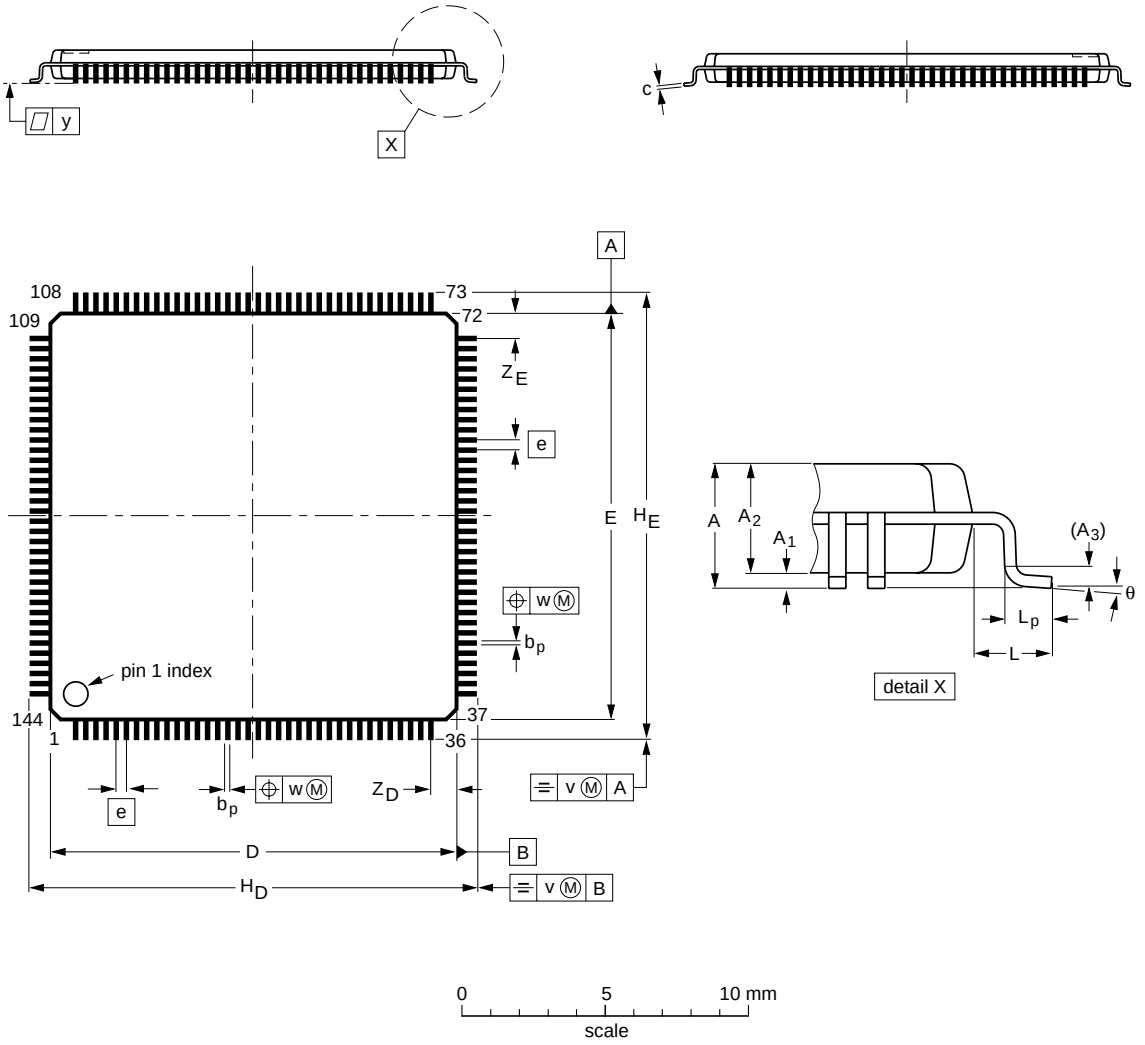
CHARACTERISTICS

$V_{DDD} = V_{DDA} = 3.3$ V ±10%; $T_{amb} = 0$ to 70 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
V_{DGND}	digital ground supply		–0.3	0.0	+0.3	V
V_{AGND}	analog ground supply		–0.3	0.0	+0.3	V
I_{DDD}	digital supply current	T_{amb} = 25 °C	–	tbf	–	mA
I_{DDA}	analog supply current	T_{amb} = 25 °C	–	tbf	–	mA
T_{amb}	temperature range		0	25	70	°C
Data and control inputs						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
Data and control outputs						
V_{OL}	LOW-level output voltage		–	–	0.8	V
V_{OH}	HIGH-level output voltage		2.0	–	–	V

PACKAGE OUTLINE

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.50	22.15 21.85	22.15 21.85	1.0	0.75 0.45	0.2	0.1	0.1	1.40 1.10	1.40 1.10	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT486-1						97-08-04

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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Printed in The Netherlands 545006/25/01/pp16 Date of release: 1999 Jun 28 Document order number: 9397 750 05846

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