

# DATA SHEET

## **TDA8784**

**18 Msps, 10-bit analog-to-digital  
interface for CCD cameras**

Product specification  
Supersedes data of 1998 Aug 05  
File under Integrated Circuits, IC02

1999 Sep 21

# 18 Msps, 10-bit analog-to-digital interface for CCD cameras

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### FEATURES

- Correlated Double Sampling (CDS), AGC, 10-bit ADC and reference regulator included, adjustable bandwidth (CDS and AGC)
- Fully programmable via a 3-wire serial interface
- Sampling frequency up to 18 MHz
- AGC gain from 4.5 to 34.5 dB (in 0.1 dB steps)
- CDS programmable bandwidth from 4 to 120 MHz
- AGC programmable bandwidth from 4 to 54 MHz
- Standby mode available for each block for power saving applications (20 mW typical)
- 6 dB fixed gain analog output for analog iris control
- 8-bit and 10-bit DAC included for analog settings
- Low power consumption of only 483 mW typical
- 5 V operation and 2.5 to 5.25 V operation for the digital outputs
- TTL compatible inputs, TTL and CMOS compatible outputs.

### APPLICATIONS

- CCD camera systems.

### GENERAL DESCRIPTION

The TDA8784 is a 10-bit analog-to-digital interface for CCD cameras. The device includes a correlated double sampling circuit, AGC and a low-power 10-bit Analog-to-Digital Converter (ADC) together with its reference voltage regulator.

The AGC and CDS have a bandwidth circuit controlled by on-chip DACs via a serial interface.

A 10-bit DAC controls the ADC input clamp level.

An additional 8-bit DAC is provided for additional system controls; its output voltage range is 1.4 V (p-p) which is available at pin OFDOUT.

### ORDERING INFORMATION

| TYPE NUMBER | PACKAGE |  |          |
|-------------|---------|--|----------|
|             | NAME    | DESCRIPTION  | VERSION  |
| TDA8784HL   | LQFP48  | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |

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## QUICK REFERENCE DATA

| SYMBOL            | PARAMETER   | CONDITIONS   | MIN. | TYP.  | MAX. | UNIT    |
|-------------------|---|--|------|-------|------|---------|
| $V_{CCA}$         | analog supply voltage                                       |  | 4.75 | 5     | 5.25 | V       |
| $V_{CCD}$         | digital supply voltage                                      |  | 4.75 | 5     | 5.25 | V       |
| $V_{CCO}$         | digital outputs supply voltage                              |  | 2.5  | 3     | 5.25 | V       |
| $I_{CCA}$         | analog supply current                                       |  | –    | 78    | 85   | mA      |
| $I_{CCD}$         | digital supply current                                      |  | –    | 18    | 20   | mA      |
| $I_{CCO}$         | digital outputs supply current                              | $f_{CLK} = 18$ MHz;<br>$C_L = 20$ pF; ramp input                       | –    | 1     | –    | mA      |
| $ADC_{res}$       | ADC resolution  |  | –    | 10    | –    | bits    |
| $V_{i(CDS)(p-p)}$ | CDS input voltage (peak-to-peak value)                      |  | –    | 400   | 1200 | mV      |
| $G_{CDS}$         | CDS output amplifier gain                                   |  | –    | 6     | –    | dB      |
| $f_{CLK(max)}$    | maximum clock frequency                                     | $f_{cut(CDS)} = 120$ MHz;<br>$f_{cut(AGC)} = 54$ MHz                   | 18   | –     | –    | MHz     |
| $AGC_{dyn}$       | AGC dynamic range   |  | –    | 30    | –    | dB      |
| $N_{tot(rms)}$    | total output noise from CDS input to ADC output (RMS value) | gain = 4.5 dB;<br>$f_{cut(CDS)} = 120$ MHz;<br>$f_{cut(AGC)} = 40$ MHz | –    | 0.125 | –    | LSB     |
| $E_{in(rms)}$     | equivalent input noise (RMS value)                          | gain = 34.5 dB   | –    | 125   | –    | $\mu$ V |
| $P_{tot}$         | total power consumption                                     |  | –    | 483   | 550  | mW      |

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### BLOCK DIAGRAM

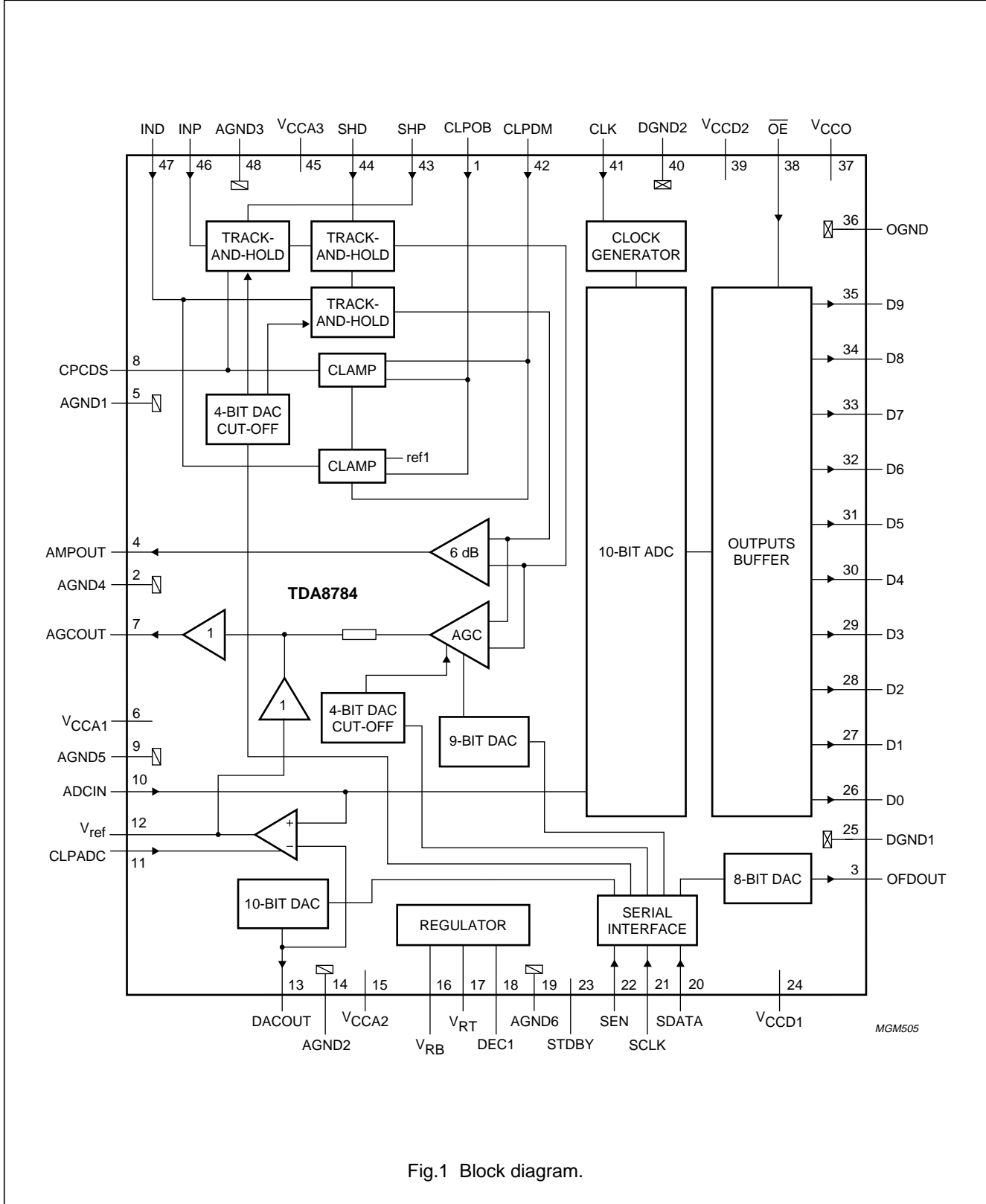


Fig.1 Block diagram.

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## PINNING

| SYMBOL            | PIN | DESCRIPTION  |
|-------------------|-----|--|
| CLPOB             | 1   | clamp pulse input at optical black   |
| AGND4             | 2   | analog ground 4  |
| OFDOUT            | 3   | analog output of the additional 8-bit control DAC (controlled via the serial interface)  |
| AMPOUT            | 4   | CDS amplifier output (fixed gain = 6 dB)   |
| AGND1             | 5   | analog ground 1  |
| V <sub>CCA1</sub> | 6   | analog supply voltage 1  |
| AGCOUT            | 7   | AGC amplifier signal output  |
| CPCDS             | 8   | clamp storage capacitor pin  |
| AGND5             | 9   | analog ground 5  |
| ADCIN             | 10  | ADC analog signal input from AGCOUT via a short circuit  |
| CLPADC            | 11  | clamp control input for ADC analog input signal clamp (used with a capacitor from V <sub>ref</sub> to ground)  |
| V <sub>ref</sub>  | 12  | ADC input clamp reference voltage (normally connected to pin V <sub>RB</sub> or DACOUT, or shorted to ground via a capacitor)  |
| DACOUT            | 13  | DAC output for ADC clamp level   |
| AGND2             | 14  | analog ground 2  |
| V <sub>CCA2</sub> | 15  | analog supply voltage 2  |
| V <sub>RB</sub>   | 16  | ADC reference voltage (BOTTOM) code 0  |
| V <sub>RT</sub>   | 17  | ADC reference voltage (TOP) code 1023  |
| DEC1              | 18  | decoupling 1 (decoupled to ground via a capacitor)   |
| AGND6             | 19  | analog ground 6  |
| SDATA             | 20  | serial data input for the 4 control DACs (9-bit DAC for AGC gain, 8-bit DAC for frequency cut-off; additional 8-bit DAC for OFD output voltage; 10-bit DAC for ADC clamp level and the standby mode per block and edge pulse control); see Table 1 |
| SCLK              | 21  | serial clock input for the control DACs and their serial interface; see Table 1  |
| SEN               | 22  | enable input for the serial interface shift register (active when SEN = logic 0); see Table 1  |
| STDBY             | 23  | standby control pin (active HIGH); all the output bits are logic 0 when standby is enabled   |
| V <sub>CCD1</sub> | 24  | digital supply voltage 1   |
| DGND1             | 25  | digital ground 1   |
| D0                | 26  | ADC digital output 0 (LSB)   |
| D1                | 27  | ADC digital output 1   |
| D2                | 28  | ADC digital output 2   |
| D3                | 29  | ADC digital output 3   |
| D4                | 30  | ADC digital output 4   |
| D5                | 31  | ADC digital output 5   |
| D6                | 32  | ADC digital output 6   |
| D7                | 33  | ADC digital output 7   |
| D8                | 34  | ADC digital output 8   |
| D9                | 35  | ADC digital output 9 (MSB)   |
| OGND              | 36  | digital output ground  |
| V <sub>CCO</sub>  | 37  | digital output supply voltage  |

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| SYMBOL            | PIN | DESCRIPTION   |
|-------------------|-----|---|
| OE                | 38  | output enable (active LOW: digital outputs active; active HIGH: digital outputs high impedance) |
| V <sub>CCD2</sub> | 39  | digital supply voltage 2  |
| DGND2             | 40  | digital ground 2  |
| CLK               | 41  | ADC clock input   |
| CLPDM             | 42  | clamp pulse input at dummy pixel  |
| SHP               | 43  | pre-set sample-and-hold pulse input   |
| SHD               | 44  | data sample-and-hold pulse input  |
| V <sub>CCA3</sub> | 45  | analog supply voltage 3   |
| INP               | 46  | pre-set input signal from CCD   |
| IND               | 47  | data input signal from CCD  |
| AGND3             | 48  | analog ground 3   |

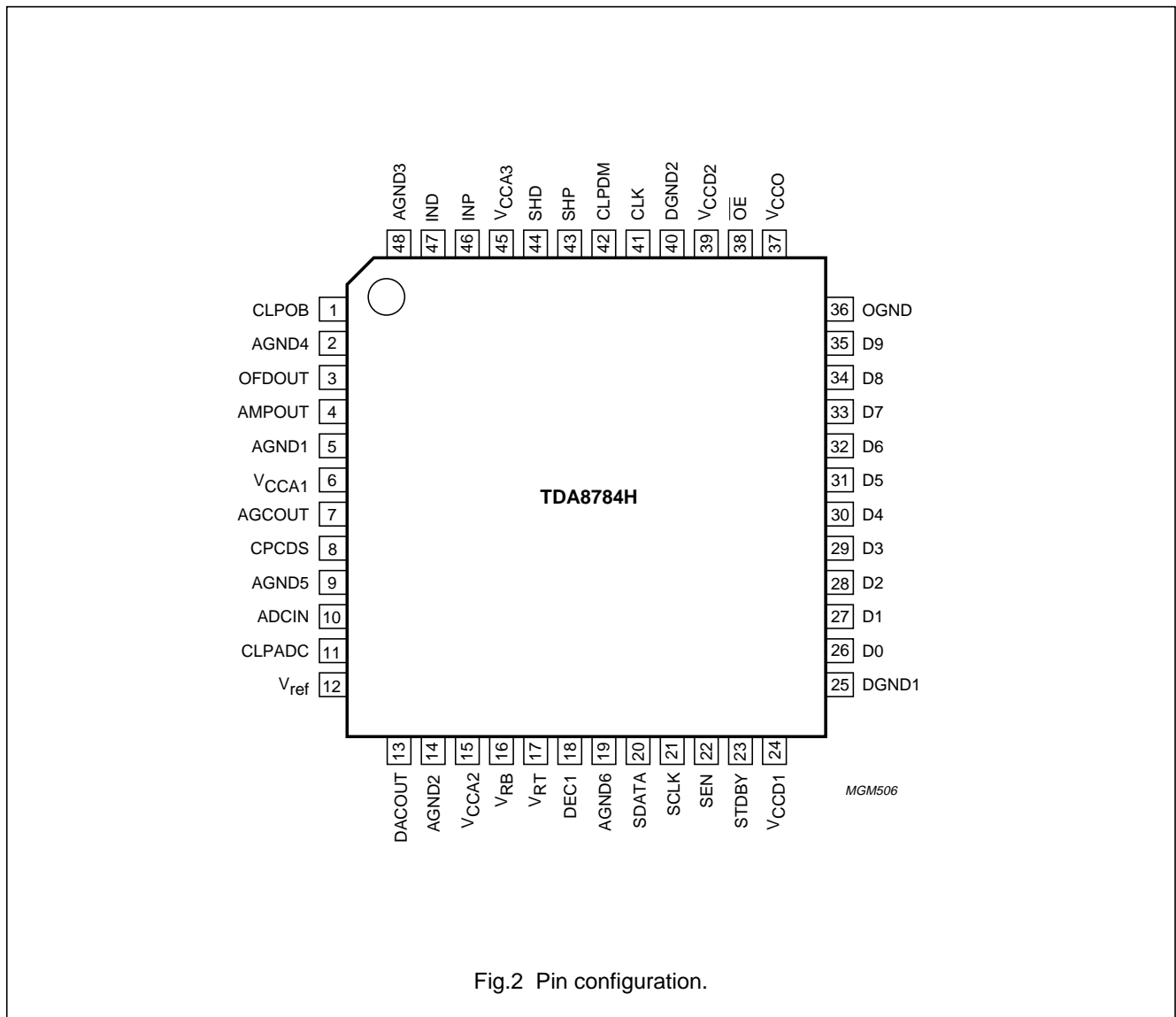


Fig.2 Pin configuration.

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL          | PARAMETER  | CONDITIONS         | MIN. | MAX.      | UNIT |
|-----------------|--|--------------------|------|-----------|------|
| $V_{CCA}$       | analog supply voltage  | note 1             | -0.3 | +7.0      | V    |
| $V_{CCD}$       | digital supply voltage                                       | note 1             | -0.3 | +7.0      | V    |
| $V_{CCO}$       | output stages supply voltage                                 | note 1             | -0.3 | +7.0      | V    |
| $\Delta V_{CC}$ | supply voltage difference<br>between $V_{CCA}$ and $V_{CCD}$ |                    | -1.0 | +1.0      | V    |
|                 | between $V_{CCA}$ and $V_{CCO}$                              |                    | -1.0 | +4.0      | V    |
|                 | between $V_{CCD}$ and $V_{CCO}$                              |                    | -1.0 | +4.0      | V    |
| $V_i$           | input voltage  | referenced to AGND | -0.3 | +7.0      | V    |
| $V_{CLK(p-p)}$  | AC input voltage for switching<br>(peak-to-peak value)       | referenced to DGND | -    | $V_{CCD}$ | V    |
| $I_o$           | output current   |                    | -    | 10        | mA   |
| $T_{stg}$       | storage temperature  |                    | -55  | +150      | °C   |
| $T_{amb}$       | ambient temperature  |                    | -20  | +75       | °C   |
| $T_j$           | junction temperature   |                    | -    | 150       | °C   |

### Note

- The supply voltages  $V_{CCA}$ ,  $V_{CCD}$  and  $V_{CCO}$  may have any value between -0.3 and +7.0 V provided that the supply voltage difference  $\Delta V_{CC}$  remains as indicated.

## HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

## THERMAL CHARACTERISTICS

| SYMBOL        | PARAMETER                                   | CONDITIONS  | VALUE | UNIT |
|---------------|---|-------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 76    | K/W  |

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## CHARACTERISTICS

 $V_{CCA} = V_{CCD} = 5\text{ V}$ ;  $V_{CCO} = 3\text{ V}$ ;  $f_{CLK} = 18\text{ MHz}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

| SYMBOL   | PARAMETER                                      | CONDITIONS  | MIN. | TYP. | MAX.      | UNIT             |
|--|--|---|------|------|-----------|------------------|
| <b>Supplies</b>  |  |   |      |      |           |                  |
| $V_{CCA}$  | analog supply voltage                          |   | 4.75 | 5    | 5.25      | V                |
| $V_{CCD}$  | digital supply voltage                         |   | 4.75 | 5    | 5.25      | V                |
| $V_{CCO}$  | digital outputs supply voltage                 |   | 2.5  | 3    | 5.25      | V                |
| $I_{CCA}$  | analog supply current                          |   | –    | 78   | 85        | mA               |
| $I_{CCD}$  | digital supply current                         |   | –    | 18   | 20        | mA               |
| $I_{CCO}$  | digital outputs supply current                 | $C_L = 20\text{ pF}$ on all data outputs;<br>ramp input   | –    | 1    | –         | mA               |
| <b>Digital inputs</b>  |  |   |      |      |           |                  |
| CLOCK INPUT: CLK (REFERENCED TO DGND)                                      |  |   |      |      |           |                  |
| $V_{IL}$   | LOW-level input voltage                        |   | 0    | –    | 0.8       | V                |
| $V_{IH}$   | HIGH-level input voltage                       |   | 2.0  | –    | $V_{CCD}$ | V                |
| $I_{IL}$   | LOW-level input current                        | $V_{CLK} = 0.8\text{ V}$  | –1   | –    | +1        | $\mu\text{A}$    |
| $I_{IH}$   | HIGH-level input current                       | $V_{CLK} = 2.0\text{ V}$  | –    | –    | 20        | $\mu\text{A}$    |
| $Z_i$  | input impedance                                | $f_{CLK} = 18\text{ MHz}$   | –    | 46   | –         | $\text{k}\Omega$ |
| $C_i$  | input capacitance                              | $f_{CLK} = 18\text{ MHz}$   | –    | 1    | –         | pF               |
| INPUTS: SHP AND SHD  |  |   |      |      |           |                  |
| $V_{IL}$   | LOW-level input voltage                        |   | 0    | –    | 0.8       | V                |
| $V_{IH}$   | HIGH-level input voltage                       |   | 2.0  | –    | $V_{CCD}$ | V                |
| $I_{IL}$   | LOW-level input current                        | $V_{IL} = 0.6\text{ V}$   | –    | –6   | –         | $\mu\text{A}$    |
| $I_{IH}$   | HIGH-level input current                       | $V_{IH} = 2.2\text{ V}$   | –    | 0    | –         | $\mu\text{A}$    |
| INPUTS: SEN, SCLK, SDATA, $\overline{OE}$ , STDBY, CLPDM, CLPOB AND CLPADC |  |   |      |      |           |                  |
| $V_{IL}$   | LOW-level input voltage                        |   | 0    | –    | 0.8       | V                |
| $V_{IH}$   | HIGH-level input voltage                       |   | 2.0  | –    | $V_{CCD}$ | V                |
| $I_i$  | input current                                  |   | –2   | –    | +2        | $\mu\text{A}$    |
| <b>Correlated Double Sampling (CDS)</b>                                    |  |   |      |      |           |                  |
| $V_{i(\text{CDS})(\text{p-p})}$  | CDS input amplitude<br>(peak-to-peak value)    |   | –    | 400  | 1200      | mV               |
| $I_{\text{CPCDS,INP,IND}}$   | input current pins 8, 46<br>and 47             |   | –2   | –    | +2        | $\mu\text{A}$    |
| $t_{\text{CDS}(\text{min})}$   | CDS control pulses minimum<br>active time      | $f_{i(\text{CDS}1,2)} = f_{\text{CLK}(\text{pix})}$ ;<br>$V_{i(\text{CDS})} = 1200\text{ mV (p-p)}$<br>black-to-white transition in<br>1 pixel ( $\pm 1\text{ LSB typ.}$ );<br>$f_{\text{cut}(\text{CDS})} = 40\text{ MHz}$ ;<br>$f_{\text{cut}(\text{AGC})} = 40\text{ MHz}$ | 12   | –    | –         | ns               |
| $t_{\text{hd}1}$   | hold time INP compared to<br>control pulse SHP | see Fig.5   | –    | 1    | –         | ns               |



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| SYMBOL                   | PARAMETER   | CONDITIONS  | MIN. | TYP.          | MAX. | UNIT              |
|--------------------------|---|---|------|---------------|------|-------------------|
| $t_{hd2}$                | hold time of IND compared to control pulse SHD                  | see Fig.5   | –    | 1             | –    | ns                |
| $t_{set(CDS)}$           | CDS settling time   | see Fig.12; control DAC 4 bits input code; AGC gain = 0 dB; $f_{cut(AGC)} = 54$ MHz; $V_{i(CDS)} = 1200$ mV (p-p) black-to-white transition in 1 pixel (1 LSB typ.) |      |               |      |                   |
|                          |   | 0000  | –    | 12            | –    | ns                |
|                          |   | 0001  | –    | 25            | –    | ns                |
|                          |   | 0010  | –    | 45            | –    | ns                |
|                          |   | 0011  | –    | 55            | –    | ns                |
|                          |   | 0100  | –    | 105           | –    | ns                |
|                          |   | 0111  | –    | 140           | –    | ns                |
|                          |   | 1000  | –    | 270           | –    | ns                |
|                          |   | 1011  | –    | 300           | –    | ns                |
|                          |   | 1111  | –    | 365           | –    | ns                |
| <b>Amplifier outputs</b> |   |   |      |               |      |                   |
| $G_{AMPOUT}$             | output amplifier gain   |   | –    | 6             | –    | dB                |
| $Z_{AMPOUT}$             | output amplifier impedance                                      |   | –    | 300           | –    | $\Omega$          |
| $V_{AMPOUT(p-p)}$        | output amplifier dynamic voltage (peak-to-peak value)           |   | –    | 2.4           | –    | V                 |
| $V_{AMPOUT(bl)}$         | output amplifier black level voltage                            |   | –    | 1.5           | –    | V                 |
| $V_{AGCOUT(p-p)}$        | AGC output amplifier dynamic voltage level (peak-to-peak value) |   | –    | 2000          | –    | mV                |
| $V_{AGCOUT}$             | AGC output amplifier black level voltage                        | $V_{ref}$ connected to DACOUT   | –    | $V_{ref}$     | –    | V                 |
| $Z_{AGCOUT}$             | AGC output amplifier output impedance                           | at 10 kHz   | –    | 5             | –    | $\Omega$          |
| $I_{AGCOUT}$             | AGC output static drive current                                 | static  | –    | –             | 1    | mA                |
| $G_{AGC(min)}$           | minimum gain of AGC circuit                                     | AGC DAC input code = 00 (9-bit control)   | –    | 4.5           | –    | dB                |
| $G_{AGC(max)}$           | maximum gain of AGC circuit                                     | AGC DAC input code $\geq 319$ (9-bit control)   | –    | 34.5          | –    | dB                |
| $f_{cut(AGC)}$           | cut-off frequency AGC   | control DAC 4-bit<br>input code = 00<br>input code = 01<br>input code = 15  | –    | 54<br>40<br>4 | –    | MHz<br>MHz<br>MHz |

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| SYMBOL   | PARAMETER  | CONDITIONS  | MIN. | TYP.      | MAX.       | UNIT    |
|--|--|---|------|-----------|------------|---------|
| <b>Clamps</b>  |  |   |      |           |            |         |
| $g_{m(ADC)}$   | ADC clamp transconductance   | at clamp level  | –    | 7         | –          | mS      |
| $g_{m(CDS)}$   | CDS clamp transconductance   | at clamp level  | –    | 1.5       | –          | mS      |
| <b>Analog-to-Digital Converter (ADC)</b>             |  |   |      |           |            |         |
| $f_{CLK(max)}$                                       | maximum clock frequency  |   | 18   | –         | –          | MHz     |
| $t_{CPH}$  | clock pulse width HIGH   |   | 15   | –         | –          | ns      |
| $t_{CPL}$  | clock pulse width LOW  |   | 15   | –         | –          | ns      |
| $SR_{CLK}$   | clock input slew rate (rising and falling edge)                        | 10% to 90%  | 0.5  | –         | –          | V/ns    |
| $V_{i(ADC)(p-p)}$                                    | ADC input voltage level (peak-to-peak value)                           |   | –    | 2         | –          | V       |
| $V_{RB}$   | ADC reference voltage output code 0                                    |   | –    | 1.5       | –          | V       |
| $V_{RT}$   | ADC reference voltage output code 1023                                 |   | –    | 3.5       | –          | V       |
| $I_{ADCIN}$  | input current pin 10   |   | –2   | –         | +120       | $\mu$ A |
| INL  | integral non-linearity   | ramp input  | –    | $\pm 0.6$ | $\pm 1.5$  | LSB     |
| DNL  | differential non-linearity   | ramp input  | –    | $\pm 0.2$ | $\pm 0.75$ | LSB     |
| $t_{d(s)}$   | sampling delay time  |   | –    | –         | 5          | ns      |
| <b>Total chain characteristics (CDS + AGC + ADC)</b> |  |   |      |           |            |         |
| $t_d$  | time delay between SHD and CLK   | see Fig.5; 50% at rising edges CLK and SHP: transition full scale code 0 to 1023;<br>$f_{cut(CDS)} = 40$ MHz;<br>$f_{cut(AGC)} = 40$ MHz;<br>$V_{i(CDS)} = 1200$ mV | –    | 40        | –          | ns      |
| $N_{tot(rms)}$                                       | total output noise (RMS value)   | $f_{cut(CDS)} = 120$ MHz;<br>$f_{cut(AGC)} = 40$ MHz; note 1<br>$G_{AGC} = 4.5$ dB<br>$G_{AGC} = 34.5$ dB   | –    | 0.125     | –          | LSB     |
|  |  |   | –    | 1.6       | –          | LSB     |
| $V_{offset(fl-d)}$                                   | maximum offset between CCD floating level and CCD dark pixel level     |   | –200 | –         | +200       | mV      |
| $V_{n(i)(eq)(rms)}$                                  | equivalent input noise voltage (RMS value)                             | AGC gain = 34.5 dB  | –    | 125       | –          | $\mu$ V |
|  |  | AGC gain = 4.5 dB   | –    | 150       | –          | $\mu$ V |
| <b>Digital-to-analog converter (OFDOUT)</b>          |  |   |      |           |            |         |
| $V_{OFDOUT(p-p)}$                                    | additional 8-bit control DAC (OFD) output voltage (peak-to-peak value) |   | –    | 1.4       | –          | V       |
| $V_{OFDOUT(0)}$                                      | DC output voltage for code 0   |   | –    | 2.3       | –          | V       |
| $V_{OFDOUT(255)}$                                    | DC output voltage for code 255   |   | –    | 3.7       | –          | V       |

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| SYMBOL   | PARAMETER  | CONDITIONS                                       | MIN.                   | TYP. | MAX.             | UNIT |
|--|--|--|------------------------|------|------------------|------|
| Z <sub>OFDOUT</sub>  | additional 8-bit control DAC (OFD) output impedance              |  | –                      | 2000 | –                | Ω    |
| I <sub>OFDOUT</sub>  | OFD output current drive   | static   | –                      | –    | 50               | μA   |
| <b>ADC clamp control DAC (see Fig.8)</b>                                 |  |  |                        |      |                  |      |
| V <sub>DACOUT(p-p)</sub>   | ADC clamp 10-bit control DAC output voltage (peak-to-peak value) |  | –                      | 1    | –                | V    |
| V <sub>DACOUT</sub>  | DC output voltage  | code 0   | –                      | 1.5  | –                | V    |
|  |  | code 1023  | –                      | 2.5  | –                | V    |
| Z <sub>DACOUT</sub>  | ADC clamp control DAC output impedance                           |  | –                      | –    | 250              | Ω    |
| I <sub>DACOUT</sub>  | DAC output current drive   | static   | –                      | –    | 50               | μA   |
| OFE <sub>LOOP</sub>  | maximum offset error of DAC + ADC clamp loop                     | code 0   | –                      | ±5   | –                | LSB  |
|  |  | code 1023  | –                      | ±5   | –                | LSB  |
| <b>Digital outputs (f<sub>CLK</sub> = 18 MHz; C<sub>L</sub> = 20 pF)</b> |  |  |                        |      |                  |      |
| V <sub>OH</sub>  | HIGH-level output voltage  | I <sub>OH</sub> = –1 mA                          | V <sub>CCO</sub> – 0.5 | –    | V <sub>CCO</sub> | V    |
| V <sub>OL</sub>  | LOW-level output voltage   | I <sub>OL</sub> = 1 mA                           | 0                      | –    | 0.5              | V    |
| I <sub>OZ</sub>  | output current in 3-state mode                                   | 0 V < V <sub>o</sub> < V <sub>CCO</sub>          | –20                    | –    | +20              | μA   |
| t <sub>o(h)</sub>  | output hold time   | see Fig.5  | 8                      | –    | –                | ns   |
| t <sub>o(d)</sub>  | output delay time  | C <sub>i</sub> = 20 pF; V <sub>CCO</sub> = 5 V   | –                      | 17   | 23               | ns   |
|  |  | C <sub>i</sub> = 10 pF                           | –                      | 15   | 21               | ns   |
|  |  | C <sub>i</sub> = 20 pF; V <sub>CCO</sub> = 3 V   | –                      | 20   | 29               | ns   |
|  |  | C <sub>i</sub> = 10 pF                           | –                      | 17   | 25               | ns   |
|  |  | C <sub>i</sub> = 20 pF; V <sub>CCO</sub> = 2.5 V | –                      | 22   | 33               | ns   |
|  |  | C <sub>i</sub> = 10 pF                           | –                      | 18   | 28               | ns   |
| <b>Serial interface</b>  |  |  |                        |      |                  |      |
| f <sub>SCLK(max)</sub>   | maximum frequency of serial interface                            |  | 5                      | –    | –                | MHz  |

**Note**

- Noise measurement at ADC outputs: the coupling capacitor at the input is connected to ground, so that only the noise contribution of the front-end is evaluated. The front-end operates at 18 Mpix with a line of 1024 pixels. The first 40 are used to run CLPOB and the last 40 to run CLPDM. Data at the ADC outputs is measured during the other pixels. The differences between the types of codes statistic is then computed; the result is the noise. No quantization noise is taken into account as no signal is input.

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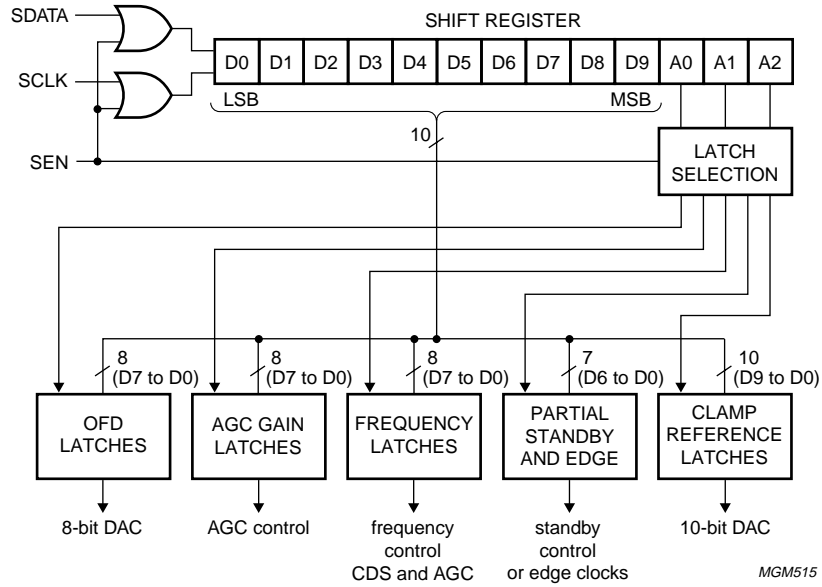
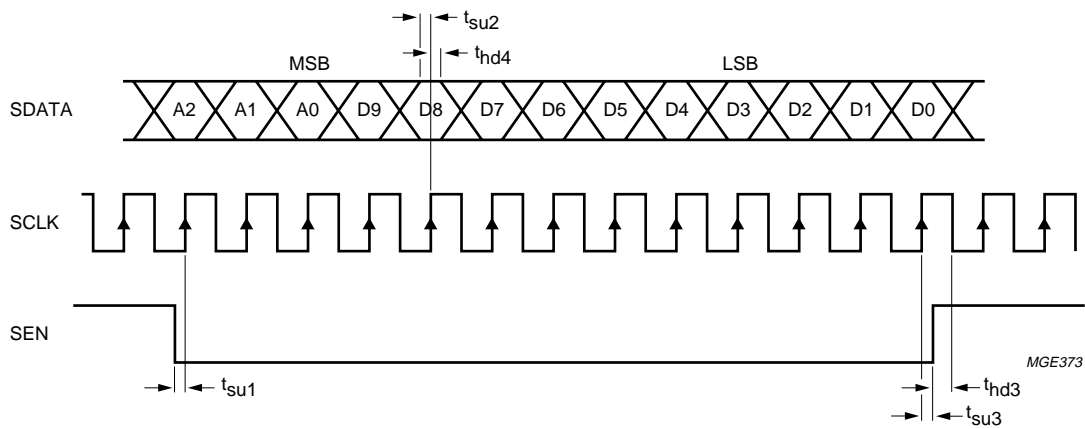


Fig.3 Serial interface block diagram.



$t_{su1} = t_{su2} = 4 \text{ ns (min.)}$ ;  $t_{hd3} = t_{hd4} = 4 \text{ ns (min.)}$ .

Fig.4 Loading sequence of control DACs input data via the serial interface.

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**Table 1** Serial interface programming

| ADDRESS BITS |    |    | DATA BITS D9 to D0   |
|--------------|----|----|--|
| A2           | A1 | A0 |  |
| 0            | 0  | 0  | OFD output control (D7 to D0).   |
| 0            | 0  | 1  | Cut-off frequency of CDS and AGC. Only the 4 LSBs (D3 to D0) are used for CDS. D4 to D7 are used for AGC. D8 and D9 should be set to logic 0.  |
| 0            | 1  | 0  | AGC gain control (D8 to D0).   |
| 0            | 1  | 1  | Partial standby controls for power consumption optimization. Only the 4 LSBs (D3 to D0) are used. Edge control for pulses SHP, SHD, CLAMP and clock ADC:<br>D0 = 1: CDS + AGC in standby; $I_{CCA} + I_{CCD} = 48$ mA<br>D1 = 1: OFD DAC in standby; $I_{CCA} + I_{CCD} = 98$ mA<br>D2 = 1: 6 dB amplifier (output on AMPOUT pin) in standby; $I_{CCA} + I_{CCD} = 98.5$ mA<br>D3 = 1: SHP and SHD activated with falling edge (for positive pulse)<br>D4 = 1: CLPDM, CLPOB and CLPADC activated on HIGH level; note 1<br>D5 = 0: CLKADC activated with falling edge<br>D6 must be set to logic 0. |
| 1            | 0  | 0  | Clamp reference DAC (D9 to D0).  |

**Note**

- When CLPADC is HIGH (D4 = 1: serial interface), the ADC input is clamped to voltage level  $V_{ref}$ .  $V_{ref}$  is connected to ground via a capacitance.

**Table 2** Standby selection

| STDBY | DATA BITS D9 to D0 | $I_{CCA} + I_{CCD}$ (TYP.) |
|-------|--------------------|----------------------------|
| 1     | LOW                | 4 mA                       |
| 0     | active             | 99 mA                      |

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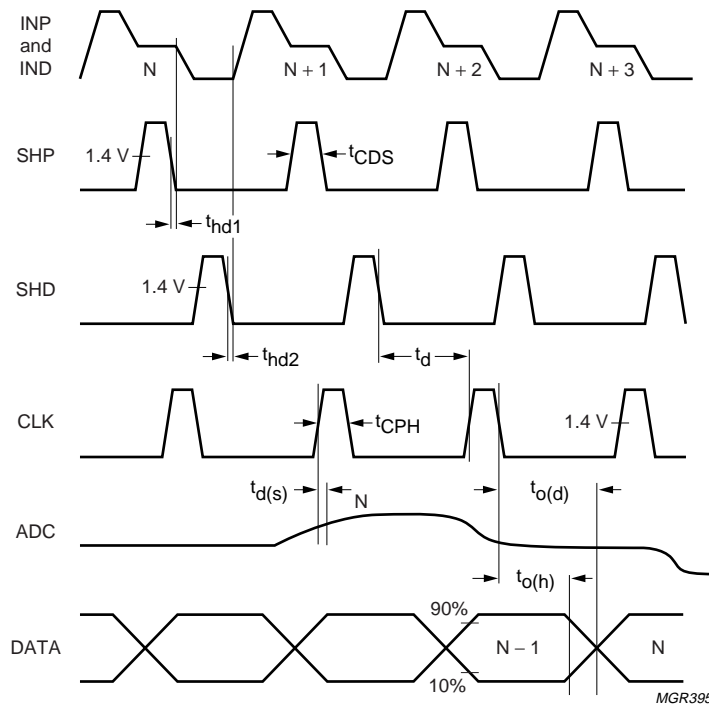
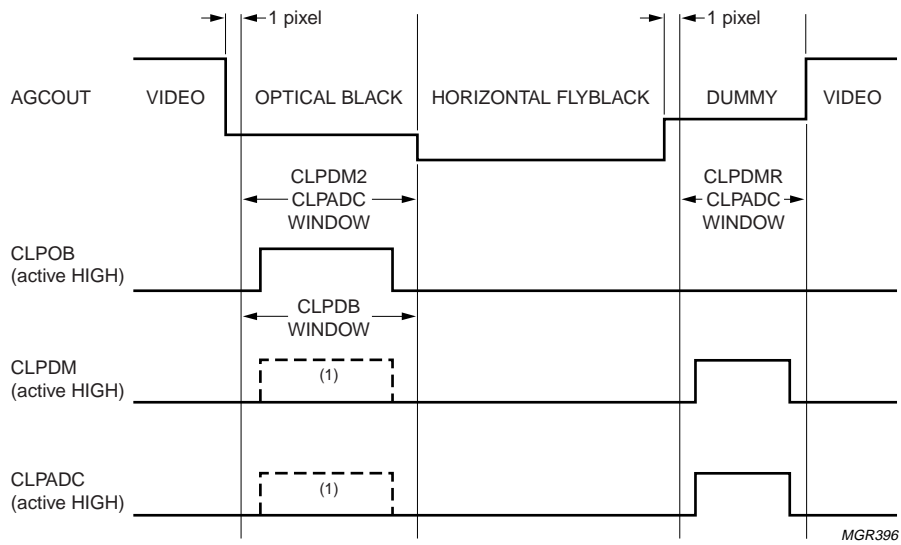


Fig.5 Pixel frequency timing diagram.

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(1) When dummy pixels are not available.

Fig.6 Line frequency timing diagram.

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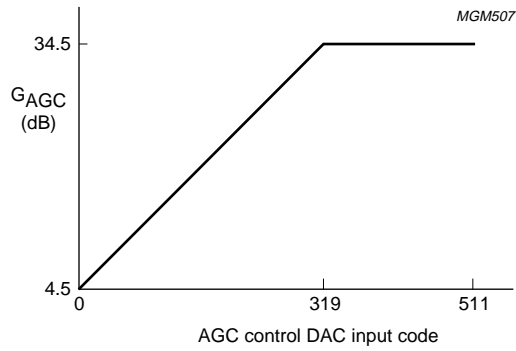


Fig.7 AGC gain as a function of DAC input code.

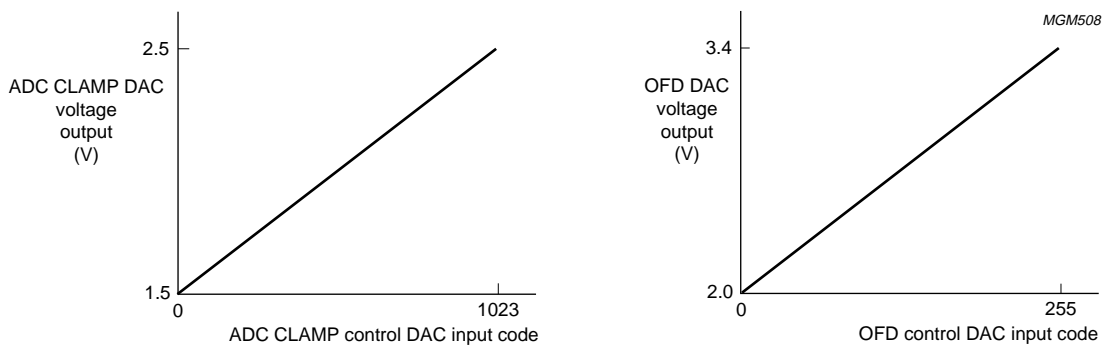


Fig.8 DAC voltage output as a function of DAC input code.



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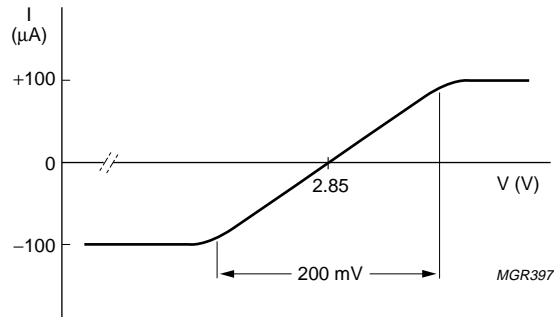


Fig.9 Typical clamp current for pin CPCDS.

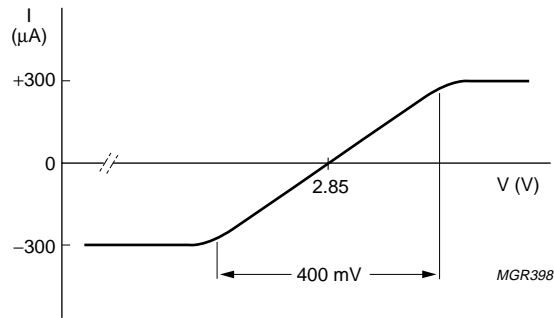


Fig.10 Typical clamp current for pins IND and INP.

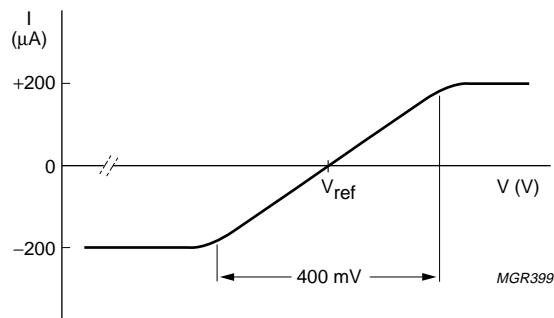
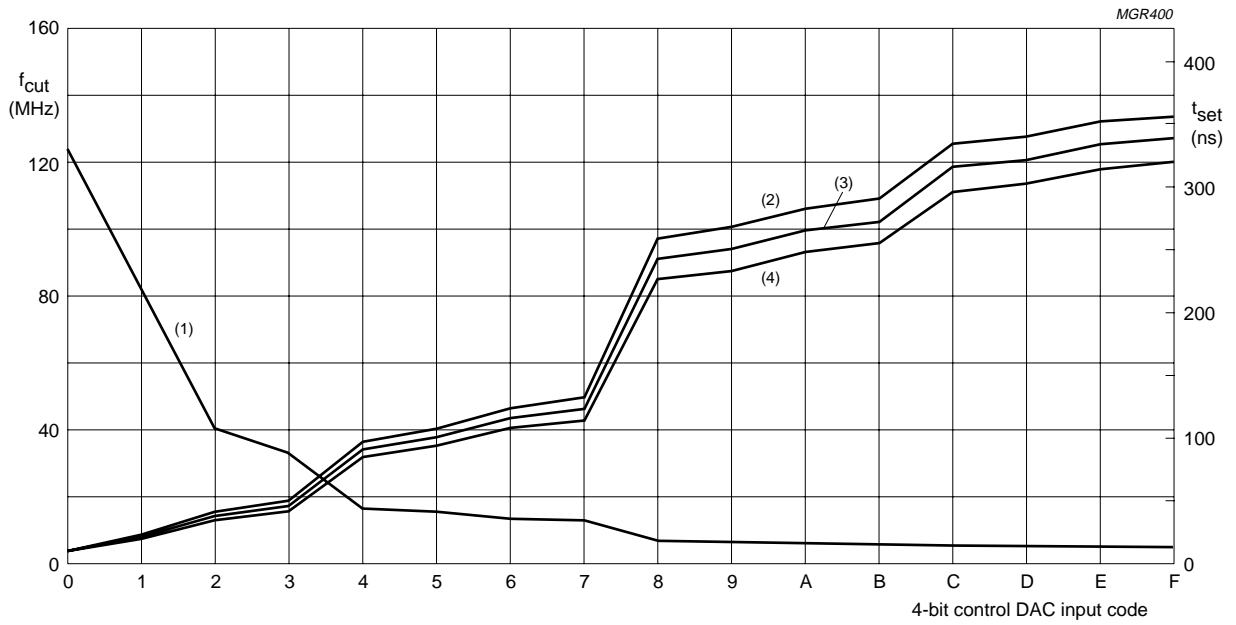


Fig.11 Typical clamp current for pin V<sub>ref</sub>.

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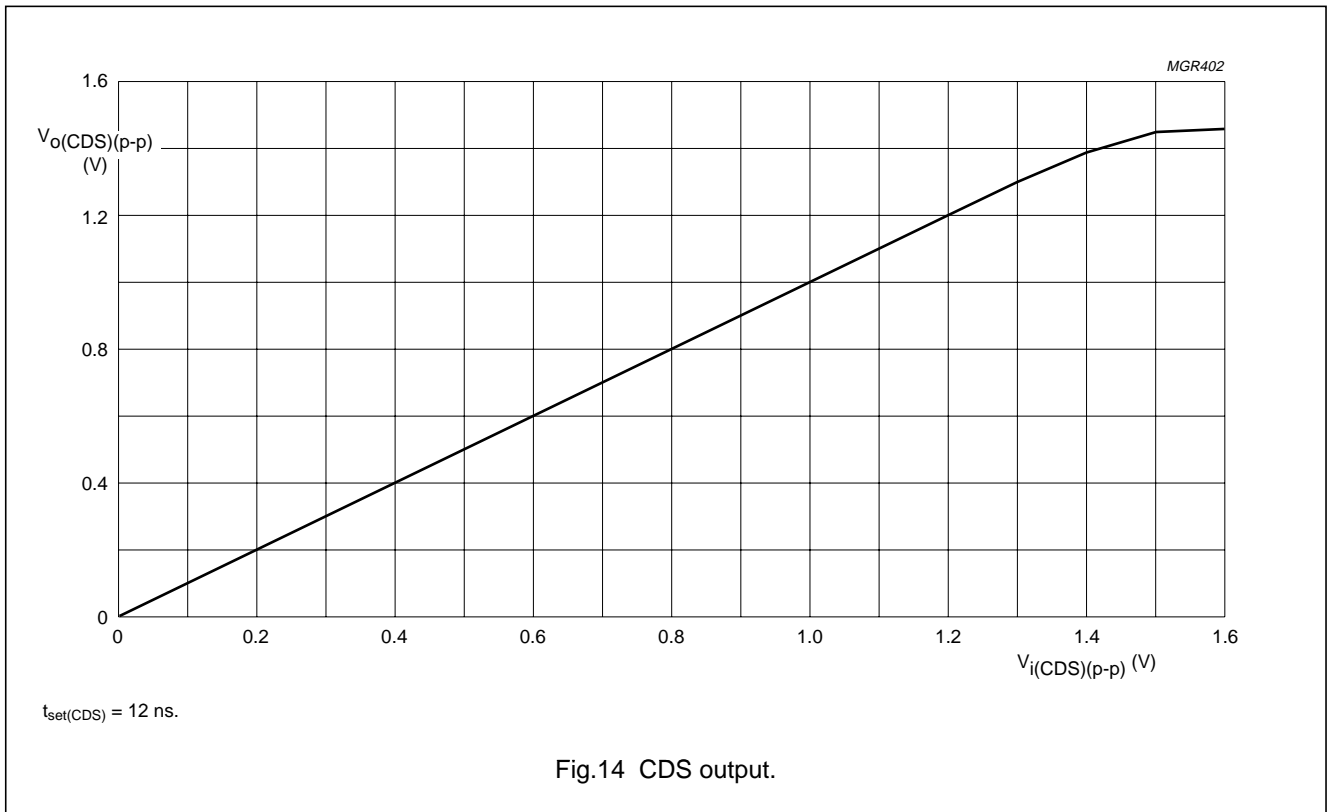
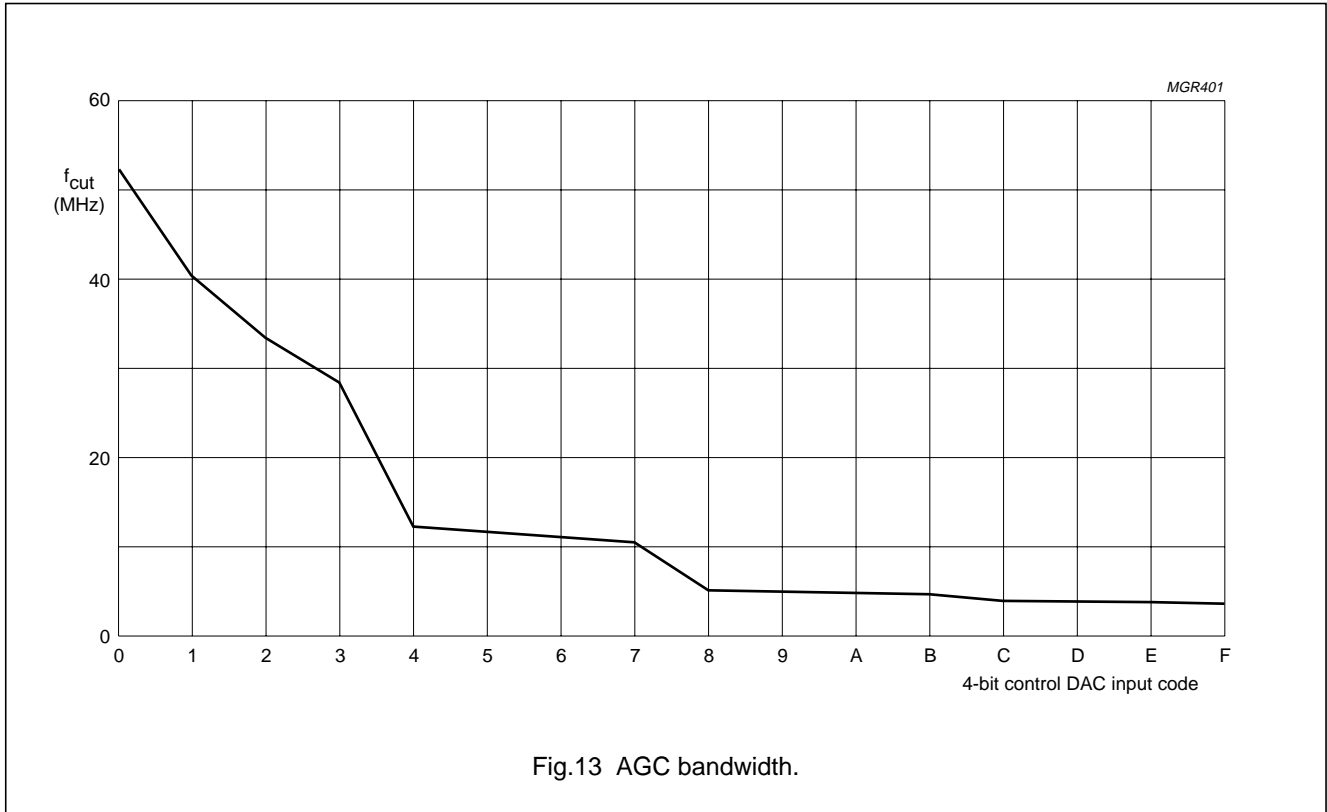


- (1)  $f_{cut}$ .
- (2)  $t_{set}$  (10b).
- (3)  $t_{set}$  (9b).
- (4)  $t_{set}$  (8b).

Fig.12 CDS settling time and bandwidth.

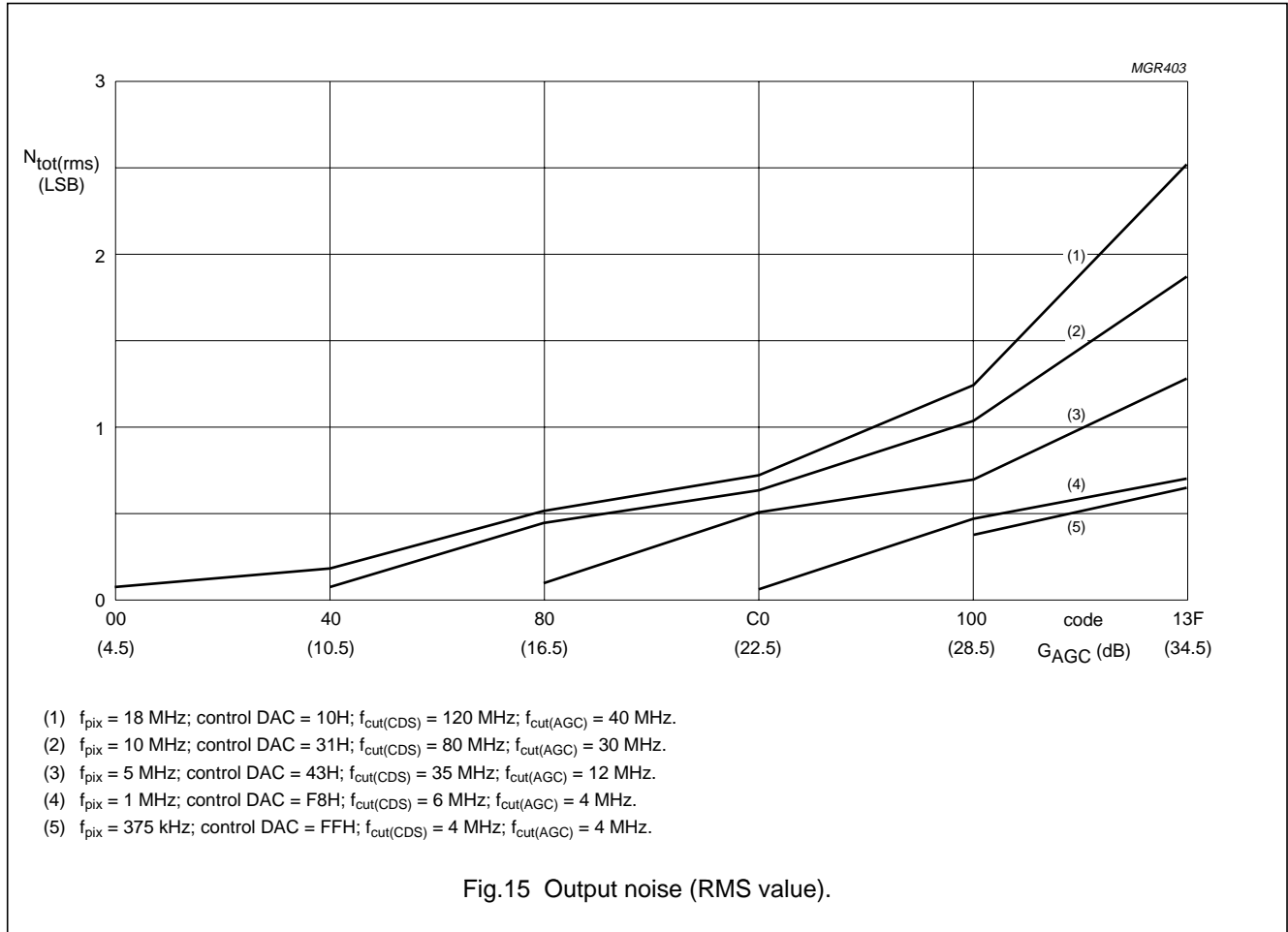
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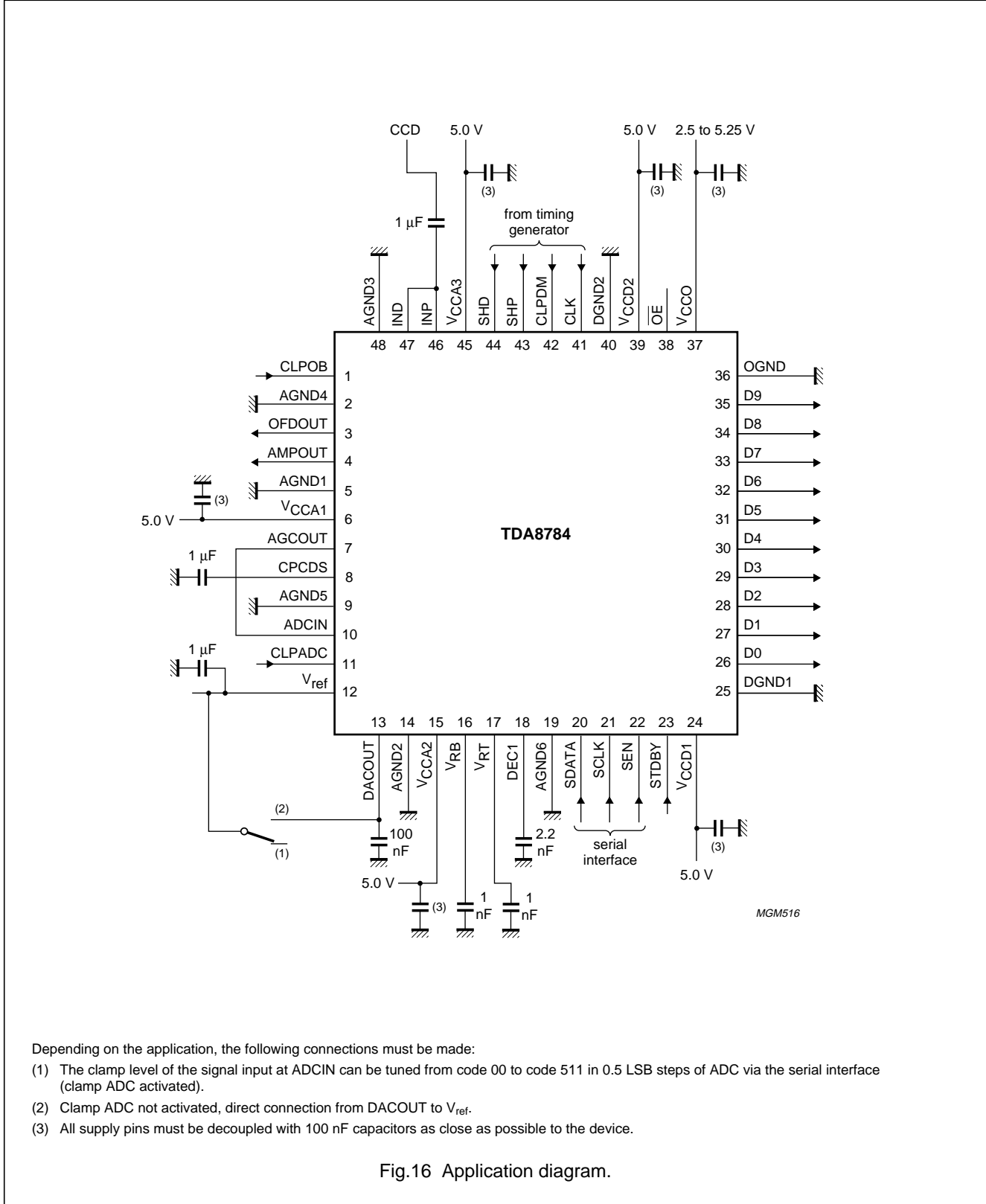
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APPLICATION INFORMATION



Depending on the application, the following connections must be made:

- (1) The clamp level of the signal input at ADCIN can be tuned from code 00 to code 511 in 0.5 LSB steps of ADC via the serial interface (clamp ADC activated).
- (2) Clamp ADC not activated, direct connection from DACOUT to Vref.
- (3) All supply pins must be decoupled with 100 nF capacitors as close as possible to the device.

Fig.16 Application diagram.

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## 18 Msps, 10-bit analog-to-digital interface for CCD cameras

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### Power and grounding recommendations

When designing a printed-circuit board for applications such as PC cameras, surveillance cameras, camcorders and digital still cameras, care should be taken to minimize the noise.

For the front-end integrated circuit, the basic rules of printed-circuit board design and implementation of analogue components (such as classical operational amplifiers) must be respected, particularly with respect to power and ground connections.

The following additional recommendation is given for the CDS input pin(s) which is/are internally connected to the programmable gain amplifier:

- The connections between CCD interface and CDS input should be as short as possible and a ground ring protection around these connections can be beneficial. Separate analogue and digital supplies provide the best solution. If it is not possible to do this on the board then the analogue supply pins must be decoupled effectively from the digital supply pins. If the same power supply and ground are used for all the pins then the decoupling capacitors must be placed as close as possible to the IC package.
- In a two-ground system, in order to minimize the noise through package and die parasitics, the following recommendations must be implemented:
  - All the analogue and digital supply pins must be decoupled to the analogue ground plane. Only the ground pin associated with the digital outputs must be connected to the digital ground plane. All the other ground pins should be connected to the analogue ground plane. The analogue and digital ground planes must be connected together at one point as close as possible to the ground pin associated with the digital outputs.
  - The digital output pins and their associated lines should be shielded by the digital ground plane which can be used then as return path for digital signals.

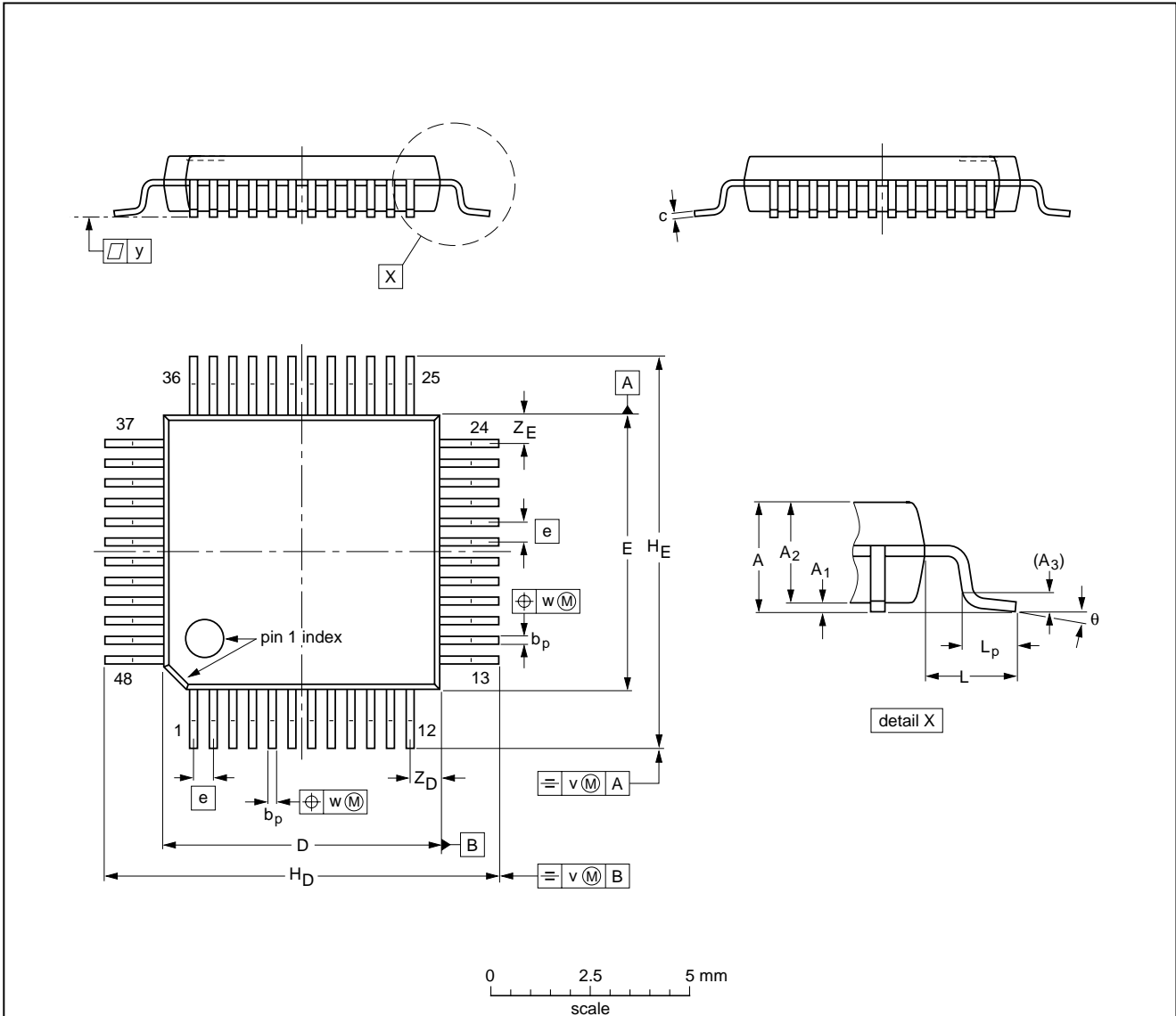
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PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

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DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e   | H <sub>D</sub> | H <sub>E</sub> | L   | L <sub>p</sub> | v   | w    | y   | Z <sub>D</sub> <sup>(1)</sup> | Z <sub>E</sub> <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-----|----------------|----------------|-----|----------------|-----|------|-----|-------------------------------|-------------------------------|----------|
| mm   | 1.60   | 0.20<br>0.05   | 1.45<br>1.35   | 0.25           | 0.27<br>0.17   | 0.18<br>0.12 | 7.1<br>6.9       | 7.1<br>6.9       | 0.5 | 9.15<br>8.85   | 9.15<br>8.85   | 1.0 | 0.75<br>0.45   | 0.2 | 0.12 | 0.1 | 0.95<br>0.55                  | 0.95<br>0.55                  | 7°<br>0° |

Note  
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |       |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|-------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC | EIAJ |  |                     |                      |
| SOT313-2        |            |       |      |  |                     | 94-12-19<br>97-08-01 |

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### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.



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## Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE                                | SOLDERING METHOD                  |                       |
|--|-----------------------------------|-----------------------|
|  | WAVE                              | REFLOW <sup>(1)</sup> |
| BGA, SQFP                              | not suitable                      | suitable              |
| HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS | not suitable <sup>(2)</sup>       | suitable              |
| PLCC <sup>(3)</sup> , SO, SOJ          | suitable                          | suitable              |
| LQFP, QFP, TQFP                        | not recommended <sup>(3)(4)</sup> | suitable              |
| SSOP, TSSOP, VSO                       | not recommended <sup>(5)</sup>    | suitable              |

### Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

### DEFINITIONS

| Data sheet status   |   |
|---|---|
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| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
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| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
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**NOTES**

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**NOTES**

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