

DATA SHEET

XA-H4

Single-chip 16-bit microcontroller

Preliminary specification
IC28 Data Handbook

1999 Sep 24

Single-chip 16-bit microcontroller

XA-H4

DESCRIPTION

The powerful 16-bit XA CPU core and rich feature set make the XA-H3 and XA-H4 devices ideal for high-performance real-time applications such as industrial control and networking. By supporting of up to 32 MB of external memory, these devices provide a low-cost solution to embedded applications of any complexity. Features like DMA, memory controller and four advanced USARTs help solve I/O intensive tasks with a minimum of CPU load.

The XA-H3 feature set is a subset of the XA-H4 (see Table 1). The XA-H3/H4 devices are members of the Philips XA (eXtended Architecture) family of high performance 16-bit microcontrollers.

The XA-H3 and XA-H4 are designed to significantly minimize the need for external components.

FEATURES

- Large Memory Support
- De-multiplexed Address/Data Bus
- Six Programmable Chip Selects
 - Support for Unified Memory – allows easy user modification of all code
 - External ISP Flash support for easy code download
- Dynamic Bus Sizing – each of 6 Chip Selects can be programmed for 8-bit or 16-bit bus.
- Dynamic Bus Timing – each of 6 chip selects has individual programmable bus timing.
- 32 Programmable General Purpose I/O Pins
- Four USARTs with 230.4 kbps capability
- Eight DMA Channels

ADDITIONAL XA-H4 FEATURES (NOT AVAILABLE ON XA-H3)

- Complete DRAM controller supports up to four banks of 8 MB each
- Memory controller supports 16 MB in Unified Mode
- Memory controller supports 32 MB in Harvard Mode
- Serial ports are USARTs
 - Synchronous capability up to 1 Mbps, and include HDLC/SDLC support
 - Four Match Characters are supported on each USART in Async Mode
 - Hardware Autobaud on all four USARTs in Async Mode
 - USARTs are improved 85C30 style

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Table 1. XA-H3 and XA-H4 features comparison

| Feature | XA-H3 | XA-H4 |
|---|---|---|
| Maximum External Memory (Harvard Memory Mode) | 6 MB | 32 MB (16 MB Code, 16 MB Data) |
| Maximum External Memory (Unified Memory Mode) | 6 MB | 16 MB |
| Memory Controller supports both Harvard and Unified architectures | Yes | Yes |
| De-multiplexed Address/Data Bus | Yes | Yes |
| DRAM Controller | No | Yes |
| DMA Channels | 8 | 8 |
| Dynamic Bus Sizing | Yes | Yes |
| Dynamic Bus Timing | Yes | Yes |
| Programmable Chip Selects | 6 | 6 |
| General Purpose IO Pins | 33 | 33 |
| Potential Interrupt Pins | 16 | 16 |
| Interrupts (programmable priority) | 7 Standard SW 4 High Priority SW 9 Hardware Event | 7 Standard SW 4 High Priority SW 9 Hardware Event |
| Two Counter/Timers plus Watchdog | Yes | Yes |
| Baud Rate Generators ¹ | 4 | 4 |
| Serial Ports | 4 UARTs | 4 USARTs |
| Maximum Serial Data Rates | asynch to 230.4 kbps (no sync) | asynch to 230.4 kbps sync to 1 Mbps |
| Match Characters | No | 4 asynch chars per USART |
| Hardware Autobaud | No | up to 230.4 kbps |

NOTE:

1. Can be used as additional counters if not needed as BRGs.

ORDERING INFORMATION

| ROMless Only | Temperature range °C and Package | Freq (MHz) | Package Drawing Number |
|-----------------|--|------------|------------------------|
| H4 = PXAH40KFBE | -40 to +85°C, 100-Pin Low Profile Quad Flat Package (LQFP) | 30 | SOT407-1 |

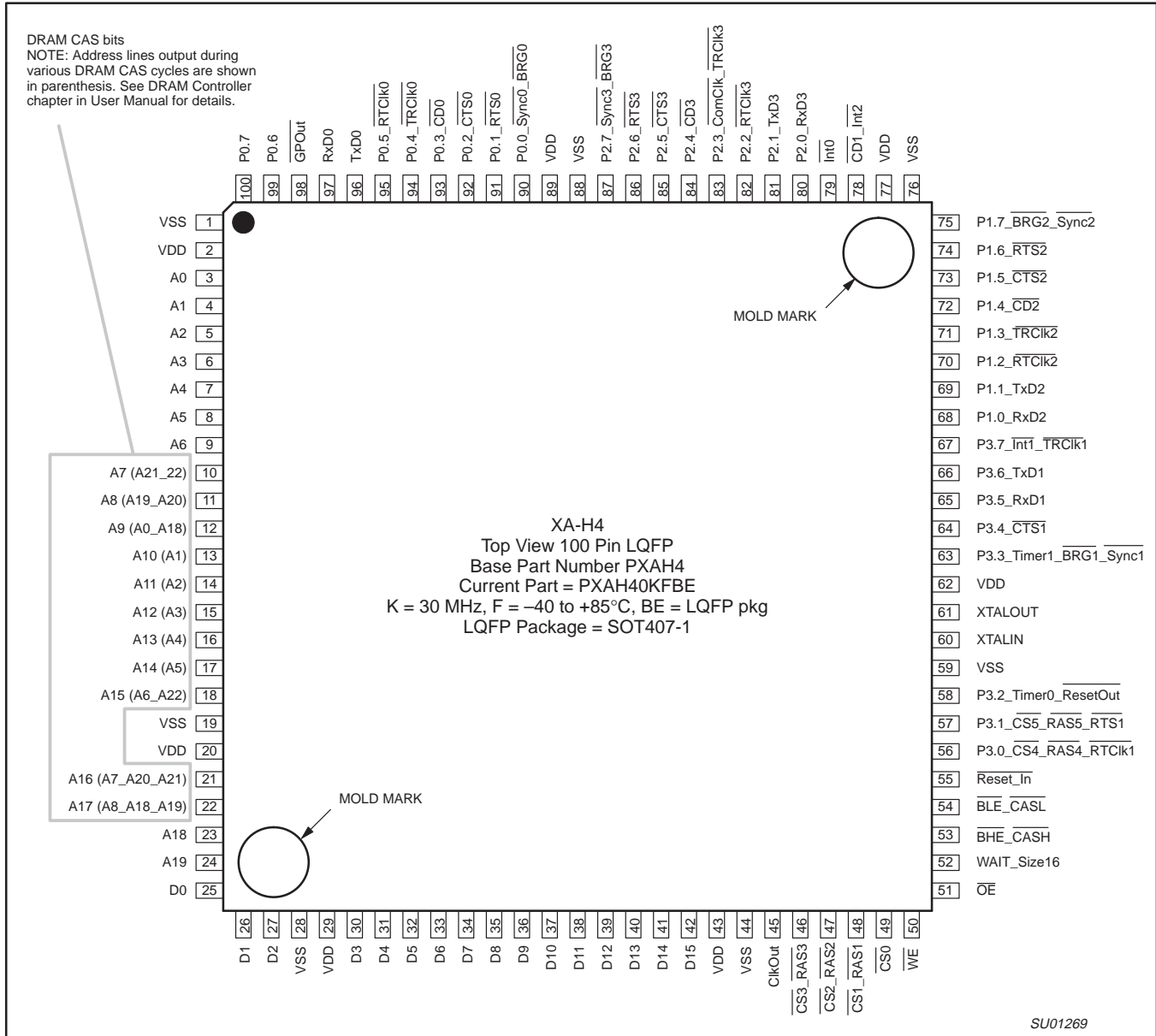
NOTE

K=30 MHz, F = (-40 to +85), BE = LQFP

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PIN CONFIGURATION

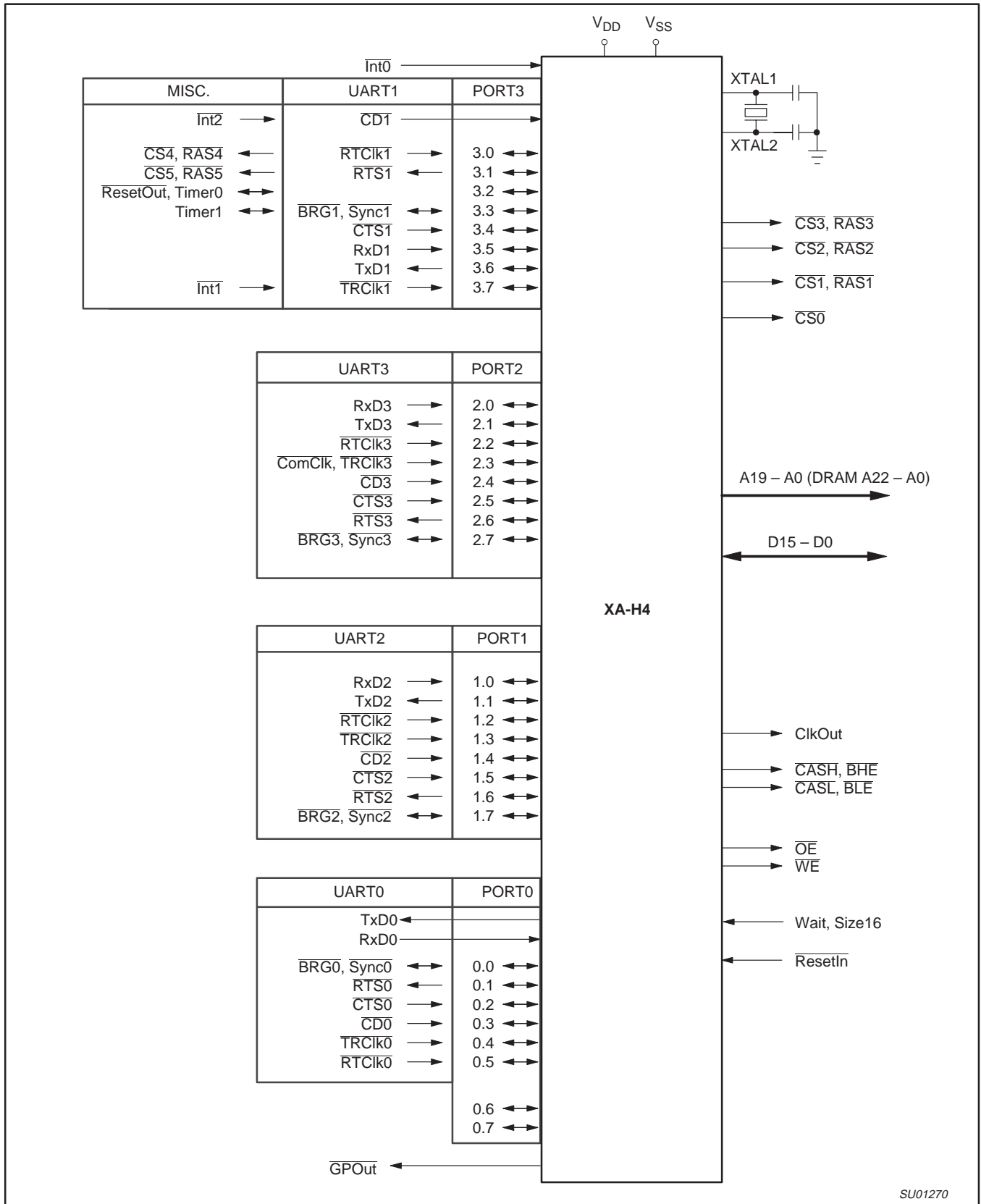


SU01269

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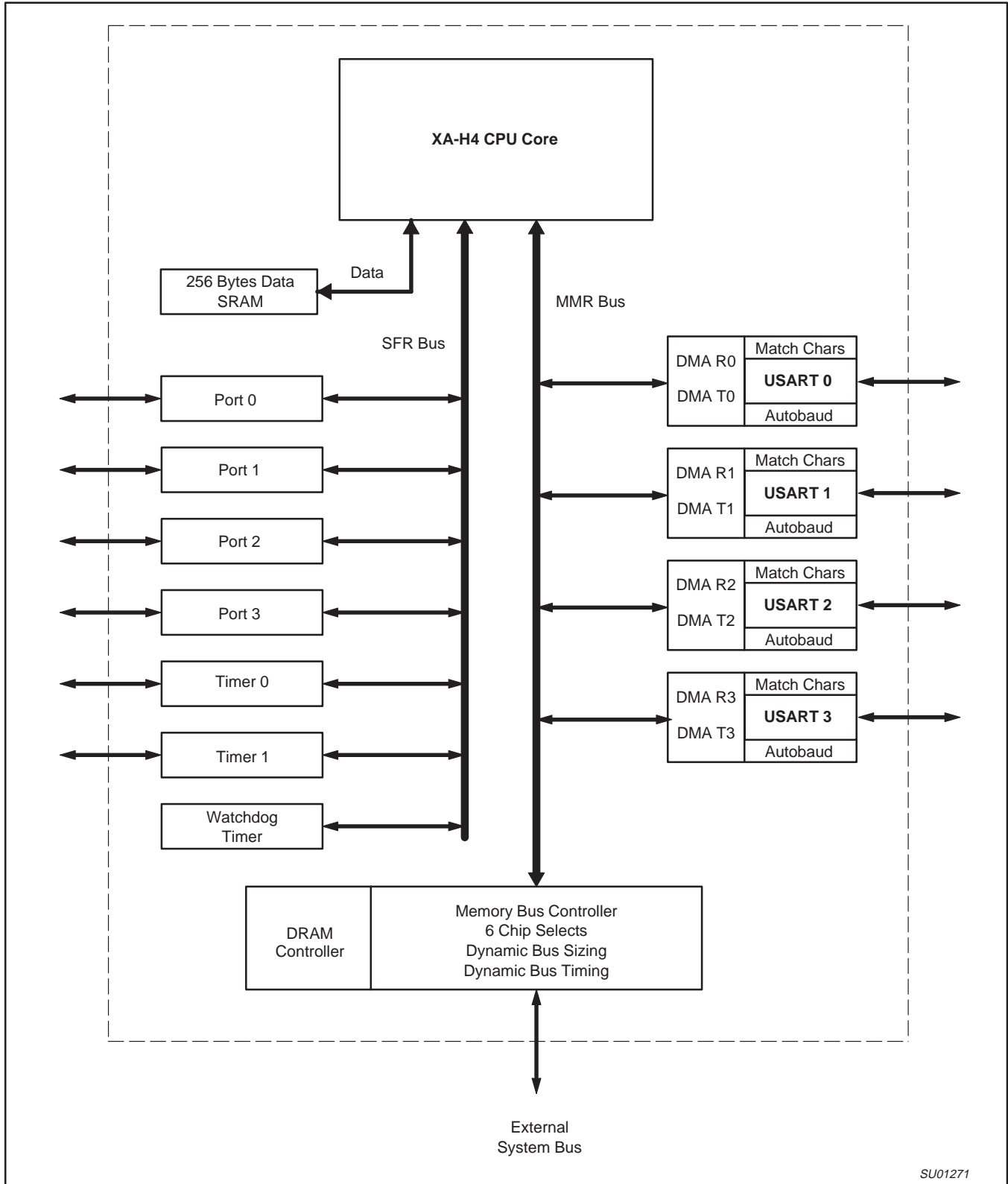
LOGIC SYMBOL XA-H4



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XA-H4 BLOCK DIAGRAM

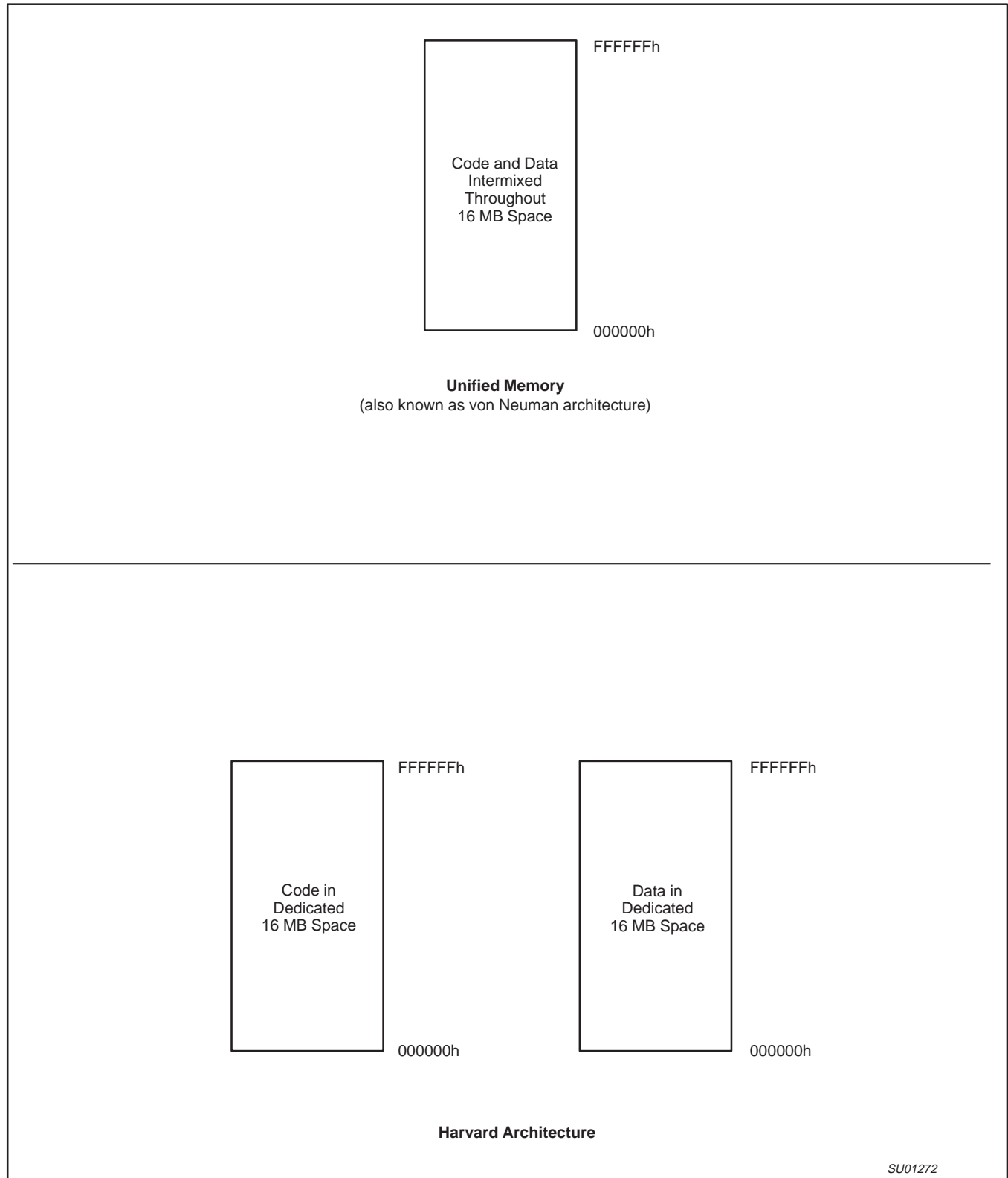


SU01271

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XA-H4 MEMORY MAPS



SU01272

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PIN DESCRIPTIONS

| Mnemonic | Lqfp Pin No. | Type | Name and Function | See Note |
|---|---------------------------|------|--|----------|
| V _{SS} | 1, 19, 28, 44, 59, 76, 88 | I | Ground: 0 V reference. | |
| V _{DD} | 2, 20, 29, 43, 62, 77, 89 | I | Power Supply: This is the power supply voltage for normal, idle, and power down operation. | |
| $\overline{\text{ResetIn}}$ | 55 | I | Reset: A low on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor to begin execution at the address contained in the reset vector. | |
| WAIT/Size16 | 52 | I | Wait/Size16: During Reset, this input determines bus size for boot device ("1" = 16-bit boot device; "0" = 8-bit.) During normal operation this is the Wait input ("1" = Wait; "0" = Proceed.) | |
| XTALIn | 60 | I | Crystal 1: Input to the inverting amplifier used in the oscillator circuit and input to the internal clock generator circuits. | |
| XTALOut | 61 | I | Crystal 2: Output from the oscillator amplifier. | |
| $\overline{\text{CS0}}$ | 49 | O | Chip Select 0: This output provides the active low chip select to the boot device (usually ROM or Flash.) It cannot be connected to DRAM. From reset, it is enabled and mapped to an address range based at 000000h. It can be remapped by software to a higher base in the address map (see the "Memory Interface" chapter in the <i>XA-H4 User Manual</i> .) | |
| CS1_RAS1 | 48 | O | Chip Select 1 or RAS1: Chip Selects and RAS 1 through 5 come out of reset disabled. They can be programmed to function as normal chip selects, or as RAS strobes to DRAM. CS1 can be "swapped" with CS0 (see the SWAP operation and control bit in the "Memory Controller" chapter of the <i>XA-H4 User Manual</i> .) CS1 is usually mapped to be based at 000000h after the swap, but is capable of being based anywhere in the 16 MB space. | |
| CS2_RAS2 | 47 | O | Chip Select 2 or RAS2: Active low Chip Selects CS1 through CS5 come out of reset disabled. They can be programmed to function as normal chip selects, or as RAS strobes to DRAM. CS2 through CS5 are not used with the "SWAP" operation (see the "Memory Controller" chapter in the <i>XA-H4 User Manual</i> .) They are mappable to any region of the 16 MB address space. | |
| CS3_RAS3 | 46 | O | CS3 or RAS3: See Chip Select 2 for description. | |
| See Pins 56, 57 for 2 additional Chip Selects | | | | |
| $\overline{\text{WE}}$ | 50 | O | Write Enable: Goes active low during all bus write cycles only. | |
| $\overline{\text{OE}}$ | 51 | O | Output Enable: Goes active low during all bus read cycles only. | |
| BLE_CASL | 54 | O | Byte Low Enable or CAS Low Byte: Goes active low during all bus cycles that access D7 – D0, read or write, Generic or DRAM. Functions as CAS during DRAM cycles. | |
| BHE_CASH | 53 | O | Byte High Enable or CAS High Byte: Goes active low during all bus cycles that access data bus lines D15 – D8, read or write, Generic or DRAM. Functions as CAS during DRAM cycles. | |
| ClkOut | 45 | O | Clock Output: This pin outputs a buffered version of the internal CPU clock. The clock output may be used in conjunction with the external bus to synchronize WAIT state generators, etc. The clock output may be disabled by software. WARNING: The capacitive loading on this output must not exceed 40 pf. | |
| A19 – A0 | 24 – 21, 18 – 3 | O | Address[19:0]: These address lines output A19 – A0 during (SRAM, etc.) bus cycles. DRAMS (H4 only) are connected only to pins 22, 21, 18 – 10 (pins A17 to A7; see user manual "MIF Chapter" for connecting various DRAM sizes); the appropriate address values are multiplexed onto these 11 pins for RAS and CAS during DRAM bus cycles. | |
| D15 – D0 | 42 – 30, 27 – 25 | I/O | Data[15:0]: Bi-directional data bus, D15 – D0. | |
| P0.0 | 90 | I/O | P0.0_Sync0_BRG0: Port 0 Bit 0, or USART0 Sync input or output, or USART0 BRG output, or USART0 TxClk output. | 1 |
| P0.1 | 91 | I/O | P0.1_RTS0: Port 0 Bit 1, or USART0 RTS (Request To Send) output. | 1 |
| P0.2 | 92 | I/O | P0.2_CTS0: Port 0 Bit 2, or USART0 CTS (Clear To Send) input. | 1 |
| P0.3 | 93 | I/O | P0.3_CD0: Port 0 Bit 3, or USART0 Carrier Detect input. | 1 |
| P0.4 | 94 | I/O | P0.4_TRClk0: Port 0 Bit 4, or USART0 TR clock input. | 1, 2 |
| P0.5 | 95 | I/O | P0.5_RTCIk0: Port 0 Bit 5, or USART0 RT clock input. | 1, 2 |
| P0.6 | 99 | I/O | P0.6: Port 0 Bit 6 | 1 |
| P0.7 | 100 | I/O | P0.7: Port 0 Bit 7 | 1 |

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| Mnemonic | Lqfp Pin No. | Type | Name and Function | See Note |
|-------------------------------|--------------|------|--|----------|
| TxD0 | 96 | O | TxD0 : Transmit data for USART0. | |
| RxD0 | 97 | I | RxD0 : Receive data for USART0. | |
| $\overline{\text{GPOut}}$ | 98 | O | $\overline{\text{GPOut}}$ – General Purpose Output Bar : Similar to GPIO, but Push/Pull and inverted output only. WARNING: This output is inverted. The polarity of the pin is the opposite of the bit that drives it (GPOut[7]). | |
| P1.0 | 68 | I/O | P1.0_RxD2 : Port 1 Bit 0, or USART2 Rx Data input | |
| P1.1 | 69 | I/O | P1.1_TxD2 : Port 1 Bit 1, or USART2 Tx Data output | |
| P1.2 | 70 | I/O | P1.2_RTClk2 : Port 1 Bit 2, or USART2 RT Clock input | 2 |
| P1.3 | 71 | I/O | P1.3_TRClk2 : Port 1 Bit 3, or USART2 TR Clock input | 2 |
| P1.4 | 72 | I/O | P1.4_CD2 : Port 1 Bit 4, or USART2 Carrier Detect input | |
| P1.5 | 73 | I/O | P1.5_CTS2 : Port 1 Bit 5, or USART2 Clear To Send input | |
| P1.6 | 74 | I/O | P1.6_RTS2 : Port 1 Bit 6, or USART2 Request To Send output | |
| P1.7 | 75 | I/O | P1.7_BRG2_Sync2 : Port 1 Bit 7, or USART2 Sync input or output, or BRG output, or TxClk output (see USART clk diagrams in the user manual.) | |
| P2.0 | 80 | I/O | P2.0_RxD3 : Port 2 Bit 0, or USART3 Rx Data input | |
| P2.1 | 81 | I/O | P2.1_TxD3 : Port 2 Bit 1, or USART3 Tx Data output | |
| P2.2 | 82 | I/O | P2.2_RTClk3 : Port 2 Bit 2, or USART3 RT Clock input | 2 |
| P2.3 | 83 | I/O | P2.3_ComClk_TRClk3 : Port 2 Bit 3, or USART3 TR Clock input | 2 |
| P2.4 | 84 | I/O | P2.4_CD3 : Port 2 Bit 4, or USART3 Carrier Detect input | |
| P2.5 | 85 | I/O | P2.5_CTS3 : Port 2 Bit 5, or USART3 Clear To Send input | |
| P2.6 | 86 | I/O | P2.6_RTS3 : Port 2 Bit 6, or USART3 Request To Send output | |
| P2.7 | 87 | I/O | P2.7_Sync3_BRG3 : Port 2 Bit 7, or USART3 Sync input or output, or BRG output, or TxClk output (see USART clock diagrams in the user manual.) | |
| P3.0 | 56 | I/O | P3.0_CS4_RAS4_RTClk1 : Port 3 Bit 0, or CS4 or RAS 4 output, or USART1 RT Clock input Active low chip selects CS1 through CS5 come out of reset disabled. They can be programmed to function as normal chip selects, or as RAS strobes to DRAM. CS2 through CS5 are not used with the “SWAP” operation (see the “Memory Controller” chapter in the <i>XA-H4 User Manual</i> .) They are mappable to any region of the 16 MB address space. | 2 |
| P3.1 | 57 | I/O | P3.1_CS5_RTS1 : Port 3 Bit 1, or CS5 output, or USART1 Request To Send output Active low chip selects CS1 through CS5 come out of reset disabled. They can be programmed to function as normal chip selects, or as RAS strobes to DRAM. CS2 through CS5 are not used with the “SWAP” operation (see the “Memory Controller” chapter in the <i>XA-H4 User Manual</i> .) They are mappable to any region of the 16 MB address space. | |
| P3.2 | 58 | I/O | P3.2_Timer0_ResetOut : Port 3 Bit 2, or Timer0 input or output, or ResetOut output. ResetOut : If the ResetOut function is selected, this pin outputs a low whenever the XA-H4 processor is reset by an internal source (Watchdog Reset or the RESET instruction.) WARNING : Unlike the other 31 GPIO pins, during power up reset, this pin can output a strongly driven low pulse. The duration of this low pulse ranges from 0 ns to 258 system clocks, starting at the time that V _{CC} is valid. The state of the $\overline{\text{ResetIn}}$ pin does not affect this pulse. When used as GPIO, this pin can be driven low by software without resetting the XA-H4. | |
| P3.3 | 63 | I/O | P3.3_Timer1_BRG1_Sync1 : Port 3 Bit 3, or Timer1 input or output, or USART1 BRG output, or USART1 Sync input or output. | |
| P3.4 | 64 | I/O | P3.4_CTS1 : Port 3 Bit 4, or USART1 Clear To Send input | |
| P3.5 | 65 | I/O | P3.5_RxD1 : Port 3 Bit 5, or USART1 Receive Data input | |
| P3.6 | 66 | I/O | P3.6_TxD1 : Port 3 Bit 6, or USART1 Transmit Data output | |
| P3.7 | 67 | I/O | P3.7_Int1_TRClk1 : Port 3 Bit 7, or External Interrupt 1 input, or USART1 TR Clock input | 2 |
| $\overline{\text{CD1_Int2}}$ | 78 | I/O | $\overline{\text{CD1_Int2}}$: USART1 Carrier Detect, or External Interrupt 2 | |
| Int0 | 79 | I/O | External Interrupt 0 | |

NOTES:

- See *XA-H4 User Guide*, “Pins Chapter,” for how to program selection of pin functions.
- RTClk input is usually used for Rx Clock if an external clock is needed, but can be used for either Rx or Tx or both. TRClk is usually used for Tx Clock, but can be used for Rx or Tx or both.

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CONTROL REGISTER OVERVIEW

There are two types of control registers in the XA-H4, these are SFRs (Special Function Registers), and MMRs (Memory Mapped Registers.) The SFR registers, with the exception of MRBL, MRBH, MICFG, BCR, BTRH, BRTL, and RSTSRC are the standard XA core registers. See **WARNINGS** about BCR, BTRH, and BRTL in Table 2.

SFRs are accessed by “direct addressing” only (see *IC25 XA User Manual* for direct addressing.) The MMRs are specific to the XA-H4

on-chip peripherals, and can be accessed by any addressing mode that can be used for off-chip data accesses. The MMRs are implemented in a relocatable block. See the “Memory Controller” chapter in the *XA-H4 User Manual* for details on how to relocate the MMRs by writing a new base address into the MRBL and MRBH (MMR Base Low and High) registers.

Table 2. Special Function Registers (SFR)

| Name | Description | SFR Address | Bit Functions and Addresses | | | | | | | | Reset Value |
|--------|---|-------------|---|--------|--------|--------|------|--------|-------|-------|-------------|
| | | | MSB | | | | LSB | | | | |
| BCR | Bus Configuration Reg RESERVED – see Warning | 46Ah | WARNING – Never write to the BCR register in the XA-H4 – it is initialized to 07h, the only legal value. This is not the same as for some other XA derivatives. | | | | | | | | 07h |
| BTRH | Bus Timing Reg High | 469h | WARNING – Immediately after reset, always write BTRH = 51h, followed by writing BTRL = 40h in that order. Follow these two writes with five NOPS. This is not the same as for some other XA derivatives. | | | | | | | | FFh |
| BTRL | Bus Timing Reg Low | 468h | | | | | | | | | |
| MRBL# | MMR Base Address Low | 496h | MA15 | MA14 | MA13 | MA12 | – | – | – | MRBE | x0h |
| MRBH# | MMR Base Address High | 497h | MA23 | MA22 | MA21 | MA20 | MA19 | MA18 | MA17 | MA16 | xx |
| MICFG# | ClkOut Tri-St Enable 1 = Enabled | 499h | – | – | – | – | – | – | – | CLKOE | 01h |
| CS | Code Segment | 443h | | | | | | | | | 00h |
| DS | Data Segment | 441h | | | | | | | | | 00h |
| ES | Extra Segment | 442h | | | | | | | | | 00h |
| IEH* | Interrupt Enable High | 427h | 33F | 33E | 33D | 33C | 33B | 33A | 339 | 338 | 00h |
| | | | EHSWR3 | EHSWR2 | EHSWR1 | EHSWR0 | – | EAuto | ESC23 | ESC01 | |
| IEL* | Interrupt Enable Low | 426h | 337 | 336 | 335 | 334 | 333 | 332 | 331 | 330 | 00h |
| | | | EA | EDMAH | EDMAL | EX2 | ET1 | EX1 | ET0 | EX0 | |
| IPA0 | Interrupt Priority A0 | 4A0h | – | PT0 | | | – | PX0 | | | 00h |
| IPA1 | Interrupt Priority A1 | 4A1h | – | PT1 | | | – | PX1 | | | 00h |
| IPA2 | Interrupt Priority A2 | 4A2h | – | PDMAL | | | – | PX2 | | | 00h |
| IPA3 | Interrupt Priority A3 | 4A3h | Reserved | | | | – | PDMAH | | | 00h |
| IPA4 | Interrupt Priority A4 | 4A4h | – | PSC23 | | | – | PSC01 | | | 00h |
| IPA5 | Interrupt Priority A5 | 4A5h | – | – | | | – | PAutoB | | | 00h |
| IPA6 | Interrupt Priority A6 | 4A6h | – | PHSWR1 | | | – | PHSWR0 | | | 00h |
| IPA7 | Interrupt Priority A7 | 4A7h | – | PHSWR3 | | | – | PHSWR2 | | | 00h |
| P0* | Port 0 | 430h | 387 | 386 | 385 | 384 | 383 | 382 | 381 | 380 | FFh |
| | | | 38F | 38E | 38D | 38C | 38B | 38A | 389 | 388 | |
| P1* | Port 1 | 431h | | | | | | | | | FFh |
| | | | 397 | 396 | 395 | 394 | 393 | 392 | 391 | 390 | |
| P2* | Port 2 | 432h | | | | | | | | | FFh |
| | | | 39F | 39E | 39D | 39C | 39B | 39A | 399 | 398 | |
| P3* | Port 3 | 433h | | | | | | | | | FFh |

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| Name | Description | SFR Address | Bit Functions and Addresses | | | | | | | | Reset Value | |
|--------|---------------------------|-------------|-----------------------------|-------|-------|-------|-------|-------|-------|-------|-------------|-----|
| | | | MSB | | | | | | | | | LSB |
| P0CFGA | Port 0 Configuration A | 470h | | | | | | | | | | 5 |
| P1CFGA | Port 1 Configuration A | 471h | | | | | | | | | | 5 |
| P2CFGA | Port 2 Configuration A | 472h | | | | | | | | | | 5 |
| P3CFGA | Port 3 Configuration A | 473h | | | | | | | | | | 5 |
| P0CFGB | Port 0 Configuration B | 4F0h | | | | | | | | | | 5 |
| P1CFGB | Port 1 Configuration B | 4F1h | | | | | | | | | | 5 |
| P2CFGB | Port 2 Configuration B | 4F2h | | | | | | | | | | 5 |
| P3CFGB | Port 3 Configuration B | 4F3h | | | | | | | | | | 5 |
| PCON* | Power Control Reg | 404h | 227 | 226 | 225 | 224 | 223 | 222 | 221 | 220 | | 00h |
| | | | – | – | – | – | – | – | PD | IDL | | |
| PSWH* | Program Status Word High | 401h | 20F | 20E | 20D | 20C | 20B | 20A | 209 | 208 | | 2 |
| | | | SM | TM | RS1 | RS0 | IM3 | IM2 | IM1 | IM0 | | |
| PSWL* | Program Status Word Low | 400h | 207 | 206 | 205 | 204 | 203 | 202 | 201 | 200 | | 2 |
| | | | C | AC | – | – | – | V | N | Z | | |
| PSW51* | 80C51 Compatible PSW | 402h | 217 | 216 | 215 | 214 | 213 | 212 | 211 | 210 | | 3 |
| | | | C | AC | F0 | RS1 | RS0 | V | F1 | P | | |
| RSTSRC | Reset Source Reg | 463h | ROEN | – | – | – | – | R_WD | R_CMD | R_EXT | | 7 |
| | | | | | | | | | | | | |
| RTH0 | Timer 0 Reload High | 455h | | | | | | | | | | 00h |
| RTH1 | Timer 1 Reload High | 457h | | | | | | | | | | 00h |
| RTL0 | Timer 0 Reload Low | 454h | | | | | | | | | | 00h |
| RTL1 | Timer 1 Reload Low | 456h | | | | | | | | | | 00h |
| SCR | System Configuration Reg | 440h | – | – | – | – | PT1 | PT0 | CM | PZ | | 00h |
| | | | | | | | | | | | | |
| SSEL* | Segment Selection Reg | 403h | 21F | 21E | 21D | 21C | 21B | 21A | 219 | 218 | | 00h |
| | | | ESWEN | R6SEG | R5SEG | R4SEG | R3SEG | R2SEG | R1SEG | R0SEG | | |
| SWE | Software Interrupt Enable | 47Ah | – | SWE7 | SWE6 | SWE5 | SWE4 | SWE3 | SWE2 | SWE1 | | 00h |
| | | | | | | | | | | | | |
| SWR* | | 42Ah | 357 | 356 | 355 | 354 | 353 | 352 | 351 | 350 | | 00h |
| | | | – | SWR7 | SWR6 | SWR5 | SWR4 | SWR3 | SWR2 | SWR1 | | |
| TCON* | Timer 0/1 Control | 410h | 287 | 286 | 285 | 284 | 283 | 282 | 281 | 280 | | 00h |
| | | | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | | |
| TH0 | Timer 0 High | 451h | | | | | | | | | | 00h |
| TH1 | Timer 1 High | 453h | | | | | | | | | | 00h |
| TL0 | Timer 0 Low | 450h | | | | | | | | | | 00h |
| TL1 | Timer 1 Low | 452h | | | | | | | | | | 00h |
| TMOD | Timer 0/1 Mode | 45Ch | GATE | C/T | M1 | M0 | GATE | C/T | M1 | M0 | | 00h |

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| Name | Description | SFR Address | Bit Functions and Addresses | | | | | | | | Reset Value |
|--------|---------------------------|-------------|-----------------------------|------|------|-----|-----|-------|-------|------|-------------|
| | | | MSB | | | | LSB | | | | |
| TSTAT* | Timer 0/1 Extended Status | 411h | 28F | 28E | 28D | 28C | 28B | 28A | 289 | 288 | 00h |
| | | | – | – | – | – | – | T1OE | – | T0OE | |
| | | | 2FF | 2FE | 2FD | 2FC | 2FB | 2FA | 2F9 | 2F8 | |
| WDCON* | Watchdog Control | 41Fh | PRE2 | PRE1 | PRE0 | – | – | WDRUN | WDTOF | – | 6 |
| WDL | Watchdog Timer Reload | 45Fh | | | | | | | | | 00h |
| WFEED1 | Watchdog Feed 1 | 45Dh | | | | | | | | | x |
| WFEED2 | Watchdog Feed 2 | 45Eh | | | | | | | | | x |

NOTES:

- * SFRs marked with an asterisk (*) are bit addressable.
- # SFRs marked with a pound sign (#) are additional SFR registers specific to the XA-H3 and XA-H4.
- 1. The XA-H4 implements an 8-bit SFR bus, as stated in Chapter 8 of the *IC25 Data Handbook XA User Guide*. All SFR accesses must be 8-bit operations. Attempts to write 16 bits to an SFR will actually write only the lower 8 bits. 16-bit SFR reads will return undefined data in the upper byte.
- 2. SFR is loaded from the reset vector.
- 3. F1, F0, and P reset to “0”. All other bits are loaded from the reset vector.
- 4. Unimplemented bits in SFRs are “X” (unknown) at all times. “1”s should not be written to these bits since they may be used for other purposes in future XA derivatives. The reset value shown for these bits is “0”.
- 5. Port configurations default to quasi-bidirectional when the XA begins execution after reset. Thus all PnCFG_A registers will contain FFh and PnCFG_B register will contain 00h. See warning in *XA-H4 User Manual* about P3.2_Timer0_ResetOut pin during first 258 clocks after power up. Basically, during this period, this pin may output a strongly-driven low pulse. If the pulse does occur, it will terminate in a transition to high at a time no later than the 259th system clock after valid V_{CC} power up.
- 6. The WDCON reset value is E6 for a Watchdog reset; E4 for all other reset causes.
- 7. The RSTSRC register reflects the cause of the last XA reset. One bit will be set to “1”, the others will be “0”. RSTSRC[7] enables the ResetOut function; “1” = Enabled, “0” = Disabled. See *XA-H4 User Manual* for details; RSTSRC[7] differs in function from most other XA derivatives.
- 8. The XA guards writes to certain bits (typically interrupt flags) that may be written by a peripheral function. This prevents loss of an interrupt or other status if a bit was written directly by a peripheral action between the read and write of an instruction that performs a read-modify-write operation. XA-H4 SFR bits that are guarded in this manner are: TF1, TF0, IE1, and IE0 (in TCON), and WDTOF (in WDCON).

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Table 3. Memory Mapped Registers (MMR)

| MMR Name | Read/Write or Read Only | Size | Address Offset | Description | Reset Value |
|--------------------------------------|-------------------------|------|----------------|---|-------------|
| USART0 Registers | | | | | |
| USART0 Write Register 0 | R/W | 8 | 800h | Command register | 00h |
| USART0 Write Register 1 | R/W | 8 | 802h | Tx/Rx Interrupt & data transfer mode | xx |
| USART0 Write Register 2 | R/W | 8 | 804h | Extended Features Control | xx |
| USART0 Write Register 3 | R/W | 8 | 806h | Receive Parameter and Control | 00h |
| USART0 Write Register 4 | R/W | 8 | 808h | Tx/Rx miscellaneous parameters & mode | 00h |
| USART0 Write Register 5 | R/W | 8 | 80Ah | Tx parameter and control | 00h |
| USART0 Write Register 6 (XA-H4 only) | R/W | 8 | 80Ch | HDLC/SDLC address field or asynch Match Character 0 | 00h |
| USART0 Write Register 7 | R/W | 8 | 80Eh | HDLC/SDLC flag or Match Character 1 | xx |
| USART0 Write Register 8 | R/W | 8 | 810h | Transmit Data Buffer | xx |
| USART0 Write Register 9 | R/W | 8 | 812h | Master Interrupt control | xx |
| USART0 Write Register 10 | R/W | 8 | 814h | Miscellaneous Tx/Rx control register | 00h |
| USART0 Write Register 11 | R/W | 8 | 816h | Clock Mode Control | xx |
| USART0 Write Register 12 | R/W | 8 | 818h | Lower Byte of Baud rate time constant | 00h |
| USART0 Write Register 13 | R/W | 8 | 81Ah | Upper Byte of Baud rate time constant | 00h |
| USART0 Write Register 14 | R/W | 8 | 81Ch | Miscellaneous Control bits | xx |
| USART0 Write Register 15 | R/W | 8 | 81Eh | External/Status interrupt control | f8h |
| USART0 Write Register 16 | R/W | 8 | 828h | Match Character 2 (WR16) | 00h |
| USART0 Write Register 17 | R/W | 8 | 82Ah | Match Character 3 (WR17) | 00h |
| USART0 Read Register 0 | RO | 8 | 820h | Tx/Rx buffer and external status | |
| USART0 Read Register 1 | RO | 8 | 822h | Receive condition status/residue code | |
| Reserved – do not write | | | 824h | | – |
| USART0 Read Register 3 | RO | 8 | 826h | Interrupt Pending Bits | |
| see WR16 and 17 | | | 828–82Ah | see WR16 and 17 above | |
| USART0 Read Register 6 | RO | 8 | 82Ch | SDLC byte count low register | |
| USART0 Read Register 7 | RO | 8 | 82Eh | SDLC byte count high and FIFO status | |
| USART0 Read Register 8 | RO | 8 | 830h | Receive Buffer | |
| Reserved | | | 832h | | |
| USART0 Read Register 10 | RO | 8 | 834h | Loop/clock status | |
| Reserved | | | 836-83Eh | | – |
| USART1 Registers | | | | | |
| USART1 Write Register 0 | R/W | 8 | 840h | Command register | 00h |
| USART1 Write Register 1 | R/W | 8 | 842h | Tx/Rx Interrupt & data transfer mode | xx |
| USART1 Write Register 2 | R/W | 8 | 844h | Extended Features Control | xx |
| USART1 Write Register 3 | R/W | 8 | 846h | Receive Parameter and Control | 00h |
| USART1 Write Register 4 | R/W | 8 | 848h | Tx/Rx miscellaneous parameters & mode | 00h |
| USART1 Write Register 5 | R/W | 8 | 84Ah | Tx parameter and control | 00h |
| USART1 Write Register 6 | R/W | 8 | 84Ch | HDLC/SDLC address field or Match Character 0 | 00h |
| USART1 Write Register 7 | R/W | 8 | 84Eh | HDLC/SDLC flag or async Match Character 1 | xx |
| USART1 Write Register 8 | R/W | 8 | 850h | Transmit Data Buffer | xx |
| USART1 Write Register 9 | R/W | 8 | 852h | Master Interrupt control | xx |
| USART1 Write Register 10 | R/W | 8 | 854h | Miscellaneous Tx/Rx control register | 00h |
| USART1 Write Register 11 | R/W | 8 | 856h | Clock Mode Control | xx |
| USART1 Write Register 12 | R/W | 8 | 858h | Lower Byte of Baud rate time constant | 00h |
| USART1 Write Register 13 | R/W | 8 | 85Ah | Upper Byte of Baud rate time constant | 00h |

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| MMR Name | Read/Write or Read Only | Size | Address Offset | Description | Reset Value |
|--------------------------|-------------------------|------|----------------|--|-------------|
| USART1 Write Register 14 | R/W | 8 | 85Ch | Miscellaneous Control bits | xx |
| USART1 Write Register 15 | R/W | 8 | 85Eh | External/Status interrupt control | f8h |
| USART1 Write Register 16 | R/W | 8 | 868h | Match Character 2 (WR16) | 00h |
| USART1 Write Register 17 | R/W | 8 | 86Ah | Match Character 3 (WR17) | 00h |
| USART1 Read Register 0 | RO | 8 | 860h | Tx/Rx buffer and external status | |
| USART1 Read Register 1 | RO | 8 | 862h | Receive condition status/residue code | |
| Reserved | | | 864h | | |
| USART1 Read Register 3 | RO | 8 | 866 | Interrupt Pending Bits | |
| see WR16 and WR17 | | 8 | 86Ch | see WR16 and 17 above | |
| USART1 Read Register 6 | RO | 8 | 86Eh | SDLC byte count low register | |
| USART1 Read Register 7 | RO | 8 | 86Eh | SDLC byte count high and FIFO status | |
| USART1 Read Register 8 | RO | 8 | 870h | Receive Buffer | |
| Reserved | | | 872h | | |
| USART1 Read Register 10 | RO | 8 | 874h | Loop/clock status | |
| Reserved | | | 876-87Eh | | |
| USART2 Registers | | | | | |
| USART2 Write Register 0 | R/W | 8 | 880h | Command register | 00h |
| USART2 Write Register 1 | R/W | 8 | 882h | Tx/Rx Interrupt & data transfer mode | xx |
| USART2 Write Register 2 | R/W | 8 | 884h | Extended Features Control | xx |
| USART2 Write Register 3 | R/W | 8 | 886h | Receive Parameter and Control | 00h |
| USART2 Write Register 4 | R/W | 8 | 888h | Tx/Rx miscellaneous parameters & mode | 00h |
| USART2 Write Register 5 | R/W | 8 | 88Ah | Tx parameter and control | 00h |
| USART2 Write Register 6 | R/W | 8 | 88Ch | HDLC/SDLC address field or Match Character 0 | 00h |
| USART2 Write Register 7 | R/W | 8 | 88Eh | HDLC/SDLC flag or Match Character 1 | xx |
| USART2 Write Register 8 | R/W | 8 | 890h | Transmit Data Buffer | xx |
| USART2 Write Register 9 | R/W | 8 | 892h | Master Interrupt control | xx |
| USART2 Write Register 10 | R/W | 8 | 894h | Miscellaneous Tx/Rx control register | 00h |
| USART2 Write Register 11 | R/W | 8 | 896h | Clock Mode Control | xx |
| USART2 Write Register 12 | R/W | 8 | 898h | Lower Byte of Baud rate time constant | 00h |
| USART2 Write Register 13 | R/W | 8 | 89Ah | Upper Byte of Baud rate time constant | 00h |
| USART2 Write Register 14 | R/W | 8 | 89Ch | Miscellaneous Control bits | xx |
| USART2 Write Register 15 | R/W | 8 | 89Eh | External/Status interrupt control | f8h |
| USART2 Write Register 16 | R/W | 8 | 8A8h | Match Character 2 (WR16) | 00h |
| USART2 Write Register 17 | R/W | 8 | 8AAh | Match Character 3 (WR17) | 00h |
| USART2 Read Register 0 | RO | 8 | 8A0h | Tx/Rx buffer and external status | |
| USART2 Read Register 1 | RO | 8 | 8A2h | Receive condition status | |
| Reserved | | | 8A4h | | |
| USART2 Read Register 3 | RO | 8 | 8A6h | Interrupt Pending Bits | |
| see WR16 and WR17 | | 8 | 8ACh | see WR16 and 17 above | |
| USART2 Read Register 6 | RO | 8 | 8AEh | SDLC byte count low register | |
| USART2 Read Register 7 | RO | 8 | 8AEh | SDLC byte count high and FIFO status | |
| USART2 Read Register 8 | RO | 8 | 8B0h | Receive Buffer | |
| Reserved | | | 8B2h | | |
| USART2 Read Register 10 | RO | 8 | 8B4h | Loop/clock status | |
| Reserved | | | 8B6-8BEh | | |

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| MMR Name | Read/Write or Read Only | Size | Address Offset | Description | Reset Value |
|--|-------------------------|------|----------------|---|-------------|
| USART3 Registers | | | | | |
| USART3 Write Register 0 | R/W | 8 | 8C0h | Command register | 00h |
| USART3 Write Register 1 | R/W | 8 | 8C2h | Tx/Rx Interrupt & data transfer mode | xx |
| USART3 Write Register 2 | R/W | 8 | 8C4h | Extended Features Control | xx |
| USART3 Write Register 3 | R/W | 8 | 8C6h | Receive Parameter and Control | 00h |
| USART3 Write Register 4 | R/W | 8 | 8C8h | Tx/Rx miscellaneous parameters & mode | 00h |
| USART3 Write Register 5 | R/W | 8 | 8CAh | Tx parameter and control | 00h |
| USART3 Write Register 6 | R/W | 8 | 8CCh | HDLC/SDLC address field or Match Character 0 | 00h |
| USART3 Write Register 7 | R/W | 8 | 8CEh | HDLC/SDLC flag or Match Character 1 | xx |
| USART3 Write Register 8 | R/W | 8 | 8D0h | Transmit Data Buffer | xx |
| USART3 Write Register 9 | R/W | 8 | 8D2h | Master Interrupt control | xx |
| USART3 Write Register 10 | R/W | 8 | 8D4h | Miscellaneous Tx/Rx control register | 00h |
| USART3 Write Register 11 | R/W | 8 | 8D6h | Clock Mode Control | xx |
| USART3 Write Register 12 | R/W | 8 | 8D8h | Lower Byte of Baud rate time constant | 00h |
| USART3 Write Register 13 | R/W | 8 | 8DAh | Upper Byte of Baud rate time constant | 00h |
| USART3 Write Register 14 | R/W | 8 | 8DCh | Miscellaneous Control bits | xx |
| USART3 Write Register 15 | R/W | 8 | 8DEh | External/Status interrupt control | f8h |
| USART3 Write Register 16 | R/W | 8 | 8E8h | Match Character 2 (WR16) | 00h |
| USART3 Write Register 17 | R/W | 8 | 8EAh | Match Character 3 (WR17) | 00h |
| USART3 Read Register 0 | RO | 8 | 8E0h | Tx/Rx buffer and external status | |
| USART3 Read Register 1 | RO | 8 | 8E2h | Receive condition status/residue code | |
| Reserved | | | 8E4h | | |
| USART3 Read Register 3 | RO | 8 | 8E6h | Interrupt Pending Bits | |
| USART3 Read Register 6 | RO | 8 | 8ECh | SDLC byte count low register | |
| USART3 Read Register 7 | RO | 8 | 8EEh | SDLC byte count high and FIFO status | |
| USART3 Read Register 8 | RO | 8 | 8F0h | Receive Buffer | |
| Reserved | | | 8F2h | | – |
| USART3 Read Register 10 | RO | 8 | 8F4h | Loop/clock status | |
| Reserved | | | 8F6-8FEh | | |
| Rx DMA Registers | | | | | |
| DMA Control Register Ch.0 Rx | R/W | 8 | 100h | Control Register | 00h |
| FIFO Control & Status Reg Ch.0 Rx | R/W | 8 | 101h | Control & Status Register | 00h |
| Segment Register Ch.0 Rx | R/W | 8 | 102h | Points to 64 k data segment | 00h |
| Buffer Base Register Ch.0 Rx | R/W | 8 | 104h | Wrap Reload Value for A15 – A8, A7 – A0 reloaded to zero by hardware | 00h |
| Buffer Bound Register Ch.0 Rx | R/W | 16 | 106h | Upper Bound (plus 1) on A15 – A0 | 0000h |
| Address Pointer Reg Ch.0 Rx | R/W | 16 | 108h | Current Address pointer A15 – A0 | 0000h |
| Byte Count Register Ch.0 Rx | R/W | 16 | 10Ah | Corresponds to A15 – A0 Byte Count, generates interrupt if enabled and byte count exceeded. | 0000h |
| Data FIFO Register Ch.0 Lo Rx | R/W | 16 | 10Ch | 10Ch = Byte 0 = older, 10Dh = Byte 1 = younger | 00h 00h |
| Data FIFO Register Ch.0 Hi Rx | R/W | 16 | 10Eh | 10Eh = Byte 2 = older, 10Fh = Byte 3 = younger | 00h 00h |
| DMA Control Register Ch.1 Rx | R/W | 8 | 110h | Control Register | 00h |
| FIFO Control & Status Register Ch.1 Rx | R/W | 8 | 111h | Control & Status Register | 00h |
| Segment Register Ch. 1 Rx | R/W | 8 | 112h | Points to 64 k data segment | 00h |

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| MMR Name | Read/Write or Read Only | Size | Address Offset | Description | Reset Value |
|--|-------------------------|------|----------------|---|-------------|
| Buffer Base Register Ch. 1 Rx | R/W | 8 | 114h | Wrap Reload Value for A15 – A8, A7 – A0 reloaded to zero by hardware | 00h |
| Buffer Bound Register Ch.1 Rx | R/W | 16 | 116h | Upper Bound (plus 1) on A15 – A0 | 0000h |
| Address Pointer Reg Ch.1 Rx | R/W | 16 | 118h | Current Address pointer A15 – A0 | 0000h |
| Byte Count Register Ch.1 Rx | R/W | 16 | 11Ah | Corresponds to A15 – A0 Byte Count, generates interrupt if enabled and byte count exceeded. | 0000h |
| Data FIFO Register Ch.1 Lo Rx | R/W | 16 | 11Ch | 11Ch = Byte 0 = older, 11Dh = Byte 1 = younger | 00h 00h |
| Data FIFO Register Ch.1 Hi Rx | R/W | 16 | 11Eh | 11Eh = Byte 2 = older, 11Fh = Byte 3 = younger | 00h 00h |
| DMA Control Register Ch.2 Rx | R/W | 8 | 120h | Control Register | 00h |
| FIFO Control & Status Register Ch.2 Rx | R/W | 8 | 121h | Control & Status Register | 00h |
| Segment Register Ch. 2 Rx | R/W | 8 | 122h | Points to 64 k data segment | 00h |
| Buffer Base Register Ch. 2 Rx | R/W | 8 | 124h | Wrap Reload Value for A15 – A8, A7 – A0 reloaded to zero by hardware | 00h |
| Buffer Bound Register Ch.2 Rx | R/W | 16 | 126h | Upper Bound (plus 1) on A15 – A0 | 0000h |
| Address Pointer Reg Ch.2 Rx | R/W | 16 | 128h | Current Address pointer A15 – A0 | 0000h |
| Byte Count Register Ch.2 Rx | R/W | 16 | 12Ah | Corresponds to A15 – A0 Byte Count, generates interrupt if enabled and byte count exceeded. | 0000h |
| Data FIFO Register Ch.2 Lo Rx | R/W | 16 | 12Ch | 12Ch = Byte 0 = older, 12Dh = Byte 1 = younger | 00h 00h |
| Data FIFO Register Ch.2 Hi Rx | R/W | 16 | 12Eh | 12Eh = Byte 2 = older, 12Fh = Byte 3 = younger | 00h 00h |
| DMA Control Register Ch.3 Rx | R/W | 8 | 130h | Control Register | 00h |
| FIFO Control & Status Register Ch.3 Rx | R/W | 8 | 131h | Control & Status Register | 00h |
| Segment Register Ch. 3 Rx | R/W | 8 | 132h | Points to 64 k data segment | 00h |
| Buffer Base Register Ch. 3 Rx | R/W | 8 | 134h | Wrap Reload Value for A15 – A8, A7 – A0 reloaded to zero by hardware | 00h |
| Buffer Bound Register Ch.3 Rx | R/W | 16 | 136h | Upper Bound (plus 1) on A15 – A0 | 0000h |
| Address Pointer Reg Ch.3 Rx | R/W | 16 | 138h | Current Address pointer A15 – A0 | 0000h |
| Byte Count Register Ch.3 Rx | R/W | 16 | 13Ah | Corresponds to A15 – A0 Byte Count, generates interrupt if enabled and byte count exceeded. | 0000h |
| Data FIFO Register Ch.3 Lo Rx | R/W | 16 | 13Ch | 13Ch = Byte 0 = older, 13Dh = Byte 1 = younger | 00h 00h |
| Data FIFO Register Ch.3 Hi Rx | R/W | 16 | 13Eh | 13Eh = Byte 2 = older, 13Fh = Byte 3 = younger | 00h 00h |
| Tx DMA Registers | | | | | |
| DMA Control Register Ch.0 Tx | R/W | 8 | 140h | Control Register | 00h |
| FIFO Control & Status Register Ch.0 Tx | R/W | 8 | 141h | Control & Status Register | 00h |
| Segment Register Ch. 0 Tx | R/W | 8 | 142h | Points to 64 k data segment | 00h |
| Buffer Base Register Ch. 0 Tx | R/W | 8 | 144h | Wrap Reload Value for A15 – A8, A7 – A0 reloaded to zero by hardware | 00h |
| Buffer Bound Register Ch.0 Tx | R/W | 16 | 146h | Upper Bound (plus 1) on A15 – A0 | 0000h |
| Address Pointer Reg Ch.0 Tx | R/W | 16 | 148h | Current Address pointer A15 – A0 | 0000h |
| Byte Count Register Ch.0 Tx | R/W | 16 | 14Ah | Corresponds to A15 – A0 Byte Count, generates interrupt if enabled and byte count exceeded. | 0000h |
| Data FIFO Register Ch.0 Tx | R/W | 16 | 14Ch | 14C = Byte0 = older 14D = Byte 1 = younger | 0000h |

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| MMR Name | Read/Write or Read Only | Size | Address Offset | Description | Reset Value |
|--|-------------------------|------|----------------|--|-------------|
| Data FIFO Register Ch.0 Tx | R/W | 16 | 14Eh | 14E = Byte2 = older 14F = Byte3 = younger | 0000h |
| DMA Control Register Ch.1 Tx | R/W | 8 | 150h | Control Register | 00h |
| FIFO Control & Status Register Ch.1 Tx | R/W | 8 | 151h | Control & Status Register | 00h |
| Segment Register Ch.1 Tx | R/W | 8 | 152h | Points to 64 k data segment | 00h |
| Buffer Base Register Ch.1 Tx | R/W | 8 | 154h | Wrap Reload Value for A15 – A8, A7 – A0 reloaded to zero by hardware | 00h |
| Buffer Bound Register Ch.1 Tx | R/W | 16 | 156h | Upper Bound (plus 1) on A15 – A0 | 0000h |
| Address Pointer Reg Ch.1 Tx | R/W | 16 | 158h | Current Address pointer A15 – A0 | 0000h |
| Byte Count Register Ch.1 Tx | R/W | 16 | 15Ah | Corresponds to A15 – A0 Byte Count, generates interrupt if enabled and byte count exceeded. | 0000h |
| Data FIFO Register Ch.1 Lo Tx | R/W | 16 | 15Ch | Byte0 & 1 | 0000h |
| Data FIFO Register Ch.1 Hi Tx | R/W | 16 | 15Eh | Byte2 & 3 | 0000h |
| DMA Control Register Ch.2 Tx | R/W | 8 | 160h | Control Register | 00h |
| FIFO Control & Status Register Ch.2 Tx | R/W | 8 | 161h | Control & Status Register | 00h |
| Segment Register Ch.2 Tx | R/W | 8 | 162h | Points to 64 k data segment | 00h |
| Buffer Base Register Ch.2 Tx | R/W | 8 | 164h | Wrap Reload Value for A15 – A8, A7 – A0 reloaded to zero by hardware | 00h |
| Buffer Bound Register Ch.2 Tx | R/W | 16 | 166h | Upper Bound (plus 1) on A15 – A0 | 0000h |
| Address Pointer Reg Ch.2 Tx | R/W | 16 | 168h | Current Address pointer A15 – A0 | 0000h |
| Byte Count Register Ch.2 Tx | R/W | 16 | 16Ah | Corresponds to A15 – A0 Byte Count, generates interrupt if enabled and byte count exceeded. | 0000h |
| Data FIFO Register Ch.2 Lo Tx | R/W | 16 | 16Ch | Byte0 & 1 | 0000h |
| Data FIFO Register Ch.2 Hi Tx | R/W | 16 | 16Eh | Byte2 & 3 | 0000h |
| DMA Control Register Ch.3 Tx | R/W | 8 | 170h | Control Register | 00h |
| FIFO Control & Status Register Ch.3 Tx | R/W | 8 | 171h | Control & Status Register | 00h |
| Segment Register Ch. 3 Tx | R/W | 8 | 172h | Points to 64 k data segment | 00h |
| Buffer Base Register Ch. 3 Tx | R/W | 8 | 174h | Wrap Reload Value for A15 – A8, A7 – A0 reloaded to zero by hardware | 00h |
| Buffer Bound Register Ch.3 Tx | R/W | 16 | 176h | Upper Bound (plus 1) on A15 – A0 | 0000h |
| Address Pointer Reg Ch.3 Tx | R/W | 16 | 178h | Current Address pointer A15 – A0 | 0000h |
| Byte Count Register Ch.3 Tx | R/W | 16 | 17Ah | Corresponds to A15 – A0 Byte Count, generates interrupt if enabled and byte count exceeded. | 0000h |
| Data FIFO Register Ch.3 Lo Tx | R/W | 16 | 17Ch | Byte0 & 1 | 0000h |
| Data FIFO Register Ch.3 Hi Tx | R/W | 16 | 17Eh | Byte2 & 3 | 0000h |
| | R/W | | 180-1FEh | RESERVED for future DMA | – |
| Miscellaneous DMA Registers | | | | | |
| Rx Character Time Out Register Ch.0 | R/W | 8 | 200h | 0 value disables counter interrupt | 00h |
| Rx Character Time Out Register Ch.1 | R/W | 8 | 202h | Same as above, for Rx1 | 00h |
| Rx Character Time Out Register Ch.2 | R/W | 8 | 204h | Same as above, for Rx2 | 00h |
| Rx Character Time Out Register Ch.3 | R/W | 8 | 206h | Same as above, for Rx3 | 00h |
| Global DMA Interrupt Register | R/W | 16 | 210h | DMA Interrupt Flags | 0000h |
| GPOut | R/W | 8 | 260h | GPOut[7] drives pin 98 (GPOut) through an inverter. GPOut[6-0] are unused, and must be written with zeroes. | 8xh |
| Autobaud Registers (H4 Only) | | | | | |
| BDAEE (H4 Only) | R/W | 8 | 270h | Autobaud echo enable (H4 Only) | 00h |
| BDCS (H4 Only) | R/W | 8 | 272h | Autobaud Control and Status (H4 Only) | 00h |

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| MMR Name | Read/Write or Read Only | Size | Address Offset | Description | Reset Value |
|---|-------------------------|------|----------------|---|-------------|
| Memory Interface (MIF) Registers | | | | | |
| B0CFG | R/W | 8 | 280h | MIF Bank 0 Config | 0Fh |
| B0AM | R/W | 8 | 281h | MIF Bank 0 Base Address | 00h |
| B0TMG | R/W | 8 | 282h | MIF Bank 0 Timing Params | |
| B1CFG | R/W | 8 | 284h | MIF Bank 1 Config | |
| B1AM | R/W | 8 | 285h | MIF Bank 1 Base Address | |
| B1TMG | R/W | 8 | 286h | MIF Bank 1 Timing Params | |
| B2CFG | R/W | 8 | 288h | MIF Bank 2 Config | |
| B2AM | R/W | 8 | 289h | MIF Bank 2 Base Address | |
| B2TMG | R/W | 8 | 28Ah | MIF Bank 2 Timing Params | |
| B3CFG | R/W | 8 | 28Ch | MIF Bank 3 Config | |
| B3AM | R/W | 8 | 28Dh | MIF Bank 3 Base Address | |
| B3TMG | R/W | 8 | 28Eh | MIF Bank 3 Timing Params | |
| B4CFG | R/W | 8 | 290h | MIF Bank 4 Config | |
| B4AM | R/W | 8 | 291h | MIF Bank 4 Base Address | |
| B4TMG | R/W | 8 | 292h | MIF Bank 4 Timing Params | |
| B5CFG | R/W | 8 | 294h | MIF Bank 5 Config | |
| B5AM | R/W | 8 | 295h | MIF Bank 5 Base Address | |
| B5TMG | R/W | 8 | 296h | MIF Bank 5 Timing Params | |
| MBCL | R/W | 8 | 2BEh | MIF Memory Bank Configuration Lock Register | |
| RFSH | R/W | 8 | 2BFh | MIF Refresh Control | |
| Miscellaneous Registers | | | | | |
| Hi-Pri Soft Ints & Pin Mux Control Reg. | R/W | 16 | 2D0h | Control bits for Hi-Priority Soft Ints, and Pin Mux | 0000h |
| XInt2 | R/W | 8 | 2D2h | External Interrupt 2 Control | 00h |

FUNCTIONAL DESCRIPTION

The XA-H4 functions are described in the following sections. Because all blocks are thoroughly documented in either the *IC25 XA Data Handbook*, or the *XA-H4 User Manual*, only brief descriptions are given in this datasheet in conjunction with references to the appropriate document.

XA CPU

The CPU is a 30 MHz implementation of the standard XA CPU core. See the *XA Data Handbook (IC25)* for details. The CPU core is identical to the G3 core. See the caveat in the next paragraph about the Bus Interface Unit.

Bus Interface Unit (BIU)

This is the internal Bus, not the bus at the pins. This internal bus connects the CPU to the MIF (Memory and DRAM Controller.)

WARNING: Immediately after reset, always write BTRH = 51h, followed by BTRL = 40h, in that order. Once written, do not change the values in these registers. Follow these two writes with five NOPS. Never write to the BCR register. It comes out of reset initialized to 07h, which is the only value that will work.

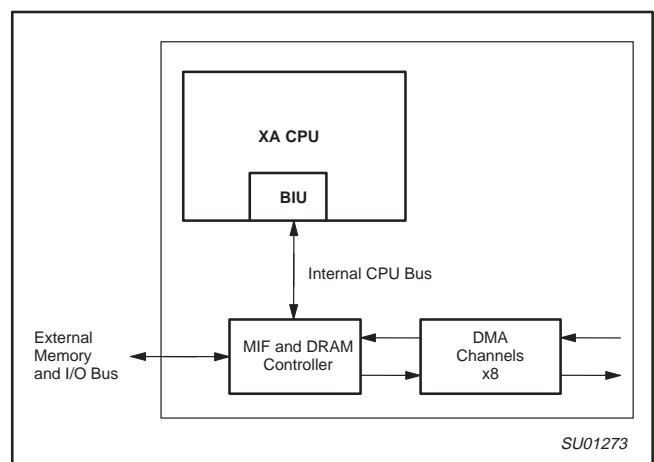


Figure 1. XA CPU core BIU (Bus Interface Unit)

Timers 0 and 1

Timers 0 and 1 are the standard XA-G3 Timer 0 and 1. Each has an associated I/O pin and interrupt. See the XA-G3 data sheet in the *IC25 XA Data Handbook* for details. Many XA derivatives include a standard XA Timer 2 and standard UARTs. These blocks have been removed in order to provide other functions on the XA-H4. There is no Timer 2 and the UARTs have been replaced with full function USARTs.

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Watchdog Timer

This timer is a standard XA-G3 Watchdog Timer. See the G3 datasheet in IC25. Also, if you intend to use the Watchdog Timer to assert the $\overline{\text{ResetOut}}$ pin, see “ResetOut” in the *XA-H4 User Manual*. The Watchdog Timer is enabled at reset, and must be periodically fed to prevent timeout. If the watchdog times out, it will generate an internal reset; if $\overline{\text{ResetOut}}$ is enabled, the internal reset will generate a $\overline{\text{ResetOut}}$ pulse (active low pulse on $\overline{\text{ResetOut}}$ pin.)

Reset

On the XA-H4 there are two pins associated with reset. The $\overline{\text{ResetIn}}$ pin provides an external reset into the XA-H4. The port pin P3.2_Timer0_ $\overline{\text{ResetOut}}$ output can be configured as $\overline{\text{ResetOut}}$.

Because $\overline{\text{ResetOut}}$ does not reflect $\overline{\text{ResetIn}}$, the $\overline{\text{ResetOut}}$ pin can be tied directly back into the $\overline{\text{ResetIn}}$ pin without other PC board logic. This configuration will make all resets (internal or external) appear to the XA as external resets. See the *XA-H4 User Manual* for a full discussion of the reset functions.

ResetIn

The $\overline{\text{ResetIn}}$ function is the standard XA-G3 $\overline{\text{ResetIn}}$ function. The $\overline{\text{ResetIn}}$ signal does NOT get passed on to $\overline{\text{ResetOut}}$. See the *XA-H4 User Manual* for details on reset.

ResetOut

The P3.2_Timer0_ $\overline{\text{ResetOut}}$ pin provides an external indication (if the $\overline{\text{ResetOut}}$ function is enabled in the RSRSRC register) via an active low output when an internal reset occurs (internal reset is Reset instruction or Watchdog time out.) If the $\overline{\text{ResetOut}}$ function is enabled, the $\overline{\text{ResetOut}}$ pin will be driven low when a Watchdog reset occurs or the Reset instruction is executed. This signal may be used to inform other devices in the system that the XA-H4 has been internally reset. The $\overline{\text{ResetIn}}$ signal does NOT get passed on to $\overline{\text{ResetOut}}$. When activated, the duration of the $\overline{\text{ResetOut}}$ pulse is 256 system clocks.

WARNING: At power on time, from the time that power coming up is valid, the P3.2_Timer0_ $\overline{\text{ResetOut}}$ pin may be driven low for any period from zero nanoseconds up to 258 system clocks. This is true independently of whether $\overline{\text{ResetIn}}$ is active or not.

Reset Source Register

The Reset Source Identification Register (RSTSRC) indicates the cause of the most recent XA reset. The cause may have been an externally applied reset signal, execution of the RESET instruction, or a Watchdog reset. Figure 2 shows the fields in the RSTSRC register. If the $\overline{\text{ResetOut}}$ function is tied back into the $\overline{\text{ResetIn}}$ pin, then all resets will be external resets, and will thus appear as external resets in the reset source register. RSTSRC[7] enables the $\overline{\text{ResetOut}}$ function; 1 = Enabled, 0 = Disabled. See *XA-H4 User Manual* for details; RSTSRC[7] differs in function from most other XA derivatives.

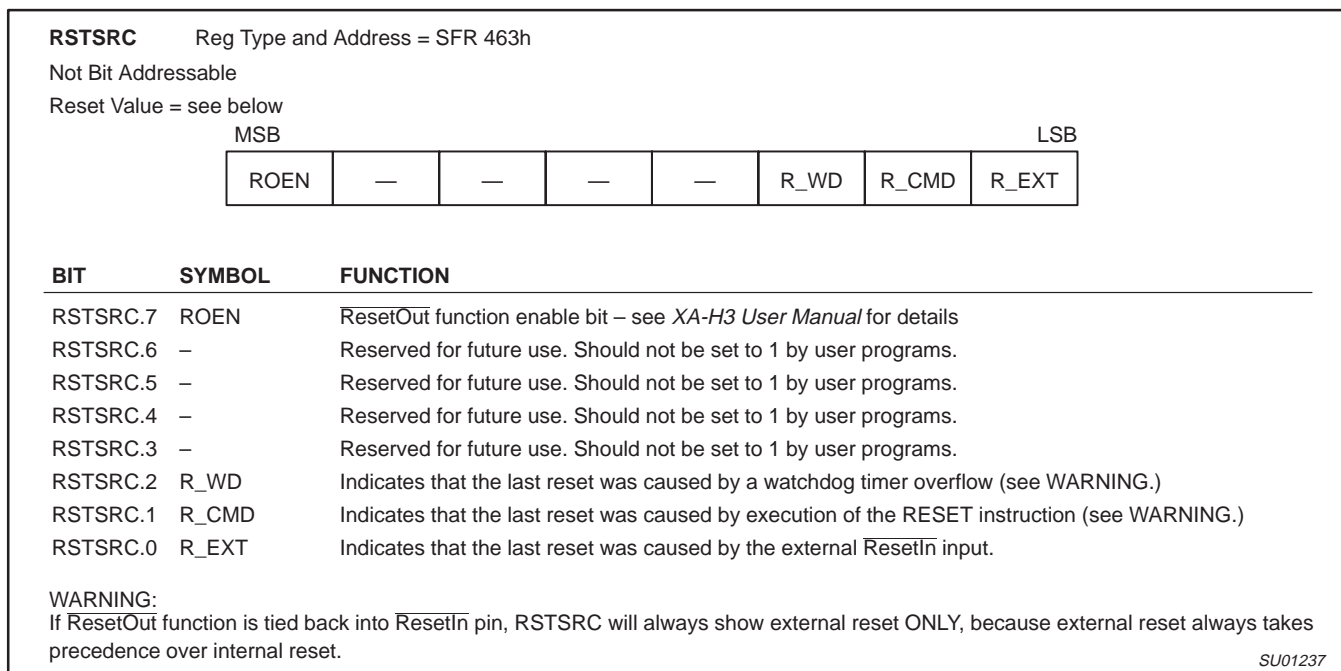


Figure 2. RSTSRC reset source register

DRAM CONTROLLER AND MEMORY / I/O BUS INTERFACE (MIF)

In the memory or system bus interface terminology, generic bus cycles are synonymous with SRAM bus cycles, because these cycles are designed to service SRAMs, Flash, EEPROM, peripheral chips, etc. Chip select output pins function as either CS or $\overline{\text{RAS}}$ (DRAMs and thus RAS on X-4H only) depending on whether the memory bank has been programmed as generic or DRAM.

The XA-H4 has a highly programmable memory bus interface with a complete complete onboard DRAM controller. Most DRAMs (up to 8 MB per $\overline{\text{RAS}}$ pin), SRAMs, Flash, ROMs, and peripheral chips can be connected to this interface with zero glue chips. The bus interface provides 6 mappable chip select outputs, five of which can be programmed to function as $\overline{\text{RAS}}$ strobes to DRAM. $\overline{\text{CAS}}$ generation, proper address multiplexing for a wide range of DRAM sizes, and refresh are all generated onboard. The bus timing for each individual

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memory bank or peripheral can be programmed to accommodate slow or fast devices.

Each memory bank and its associated $\overline{\text{RAS}}$ (chip select in DRAM mode) output, can be programmed to access up to an 8 MB mappable address space in either EDO or FPM DRAM modes (up to a total of 32 MB of DRAM. **WARNING:** Future XA-H4 derivatives may not support separate code and data spaces.)

Each memory bank and associated chip select programmed for "generic" (SRAM, Flash, ROM, peripheral chips, etc.) is capable of supporting a 1 MB address space.

The Memory Interface can be programmed to support both Intel style and 68000 bus style SRAMs and peripherals.

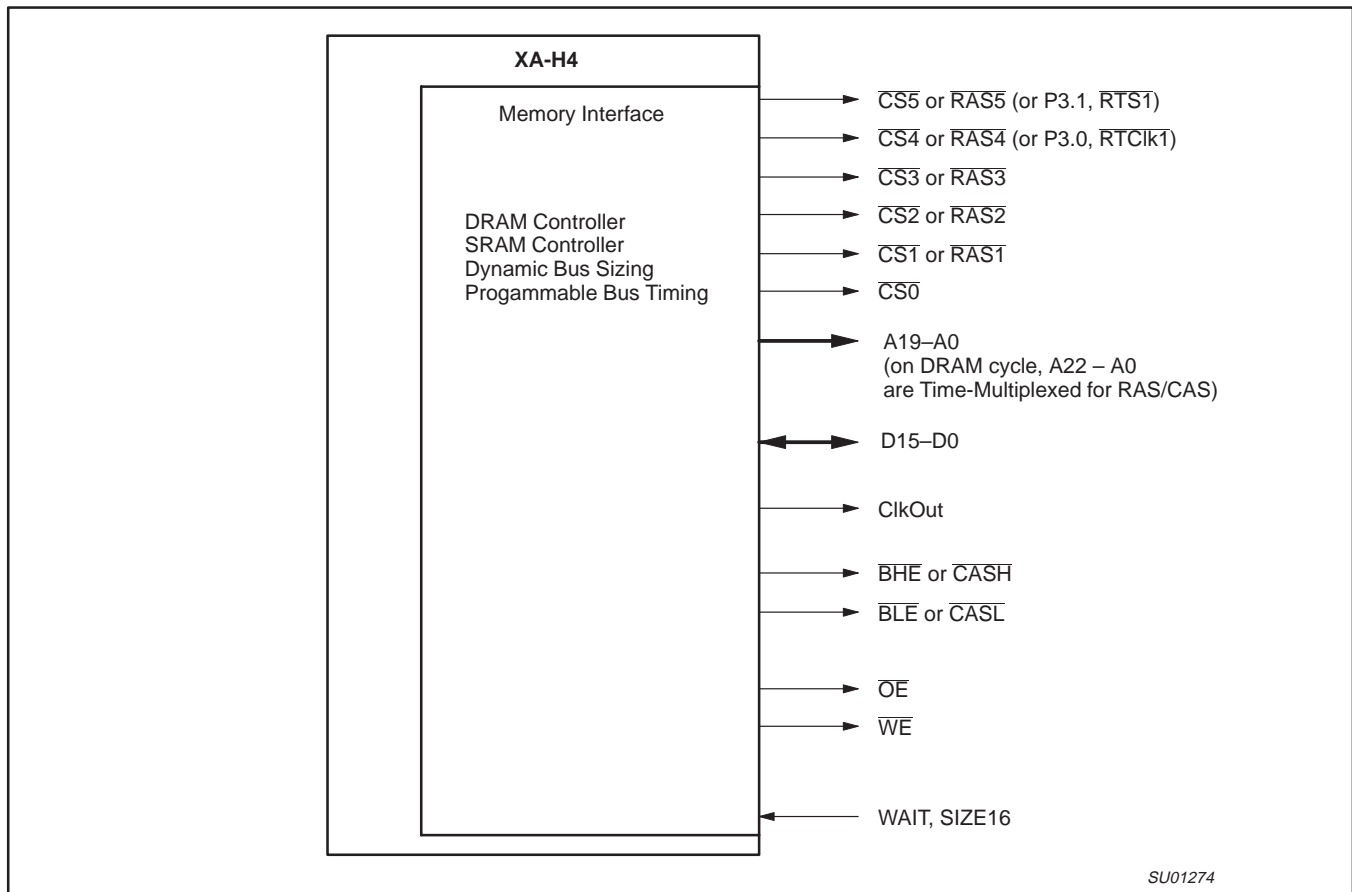


Figure 3. Memory bus interface signal pins

Bus Interface Pins

For the following discussion, see Figure 3.

Chip Select Pins

There are six chip select pins ($\overline{\text{CS}}5 - \overline{\text{CS}}0$) mapped to six sets of bank control registers. The following attributes are individually programmable for each bank and associated chip select (or $\overline{\text{RAS}}$, if DRAM): bank on/off, address range, external device access time, detailed bus strobe sequence, DRAM cycle or generic bus cycle, DRAM size if DRAM, and bus width. Pin $\overline{\text{CS}}0$ is always generic in order to service the boot device, thus $\overline{\text{CS}}0$ cannot be connected to DRAM.

WARNING: On the external bus, ALL XA-H4 reads are 16-bit Reads. If the CPU instruction only specifies 8-bits, then the CPU uses the appropriate byte, and discards the extra byte. Thus "8-Bit Reads" and "16-Bit Reads" appear to be identical on the bus. **On an 8-bit bus, this will appear as two consecutive 8-bit reads** even though the CPU instruction specified a byte read.

Some 8-bit I/O devices (especially FIFOs) cannot operate correctly with 2 bytes being read for a 1 Byte Read. The most common (and least expensive) solution is to operate these 8-bit devices on a 16-bit bus, and access them in software on all odd byte (or all even byte) boundaries. An added benefit of this technique is that byte Reads are faster than on an 8-bit bus, because only 1 word is fetched (a single Read) instead of 2 consecutive bytes.

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Clock Output

The ClkOut pin allows easier external bus interfacing in some situations. This output reflects the XTALIn clock input to the XA (referred to internally as CClk or System Clock), but is delayed to match the external bus outputs and strobes. The default is for

ClkOut to be output enabled at reset, but it may be turned off (tri-state disabled) by software via the MICFG MMR.

WARNING: The capacitive loading on this output must not exceed 40 pf.

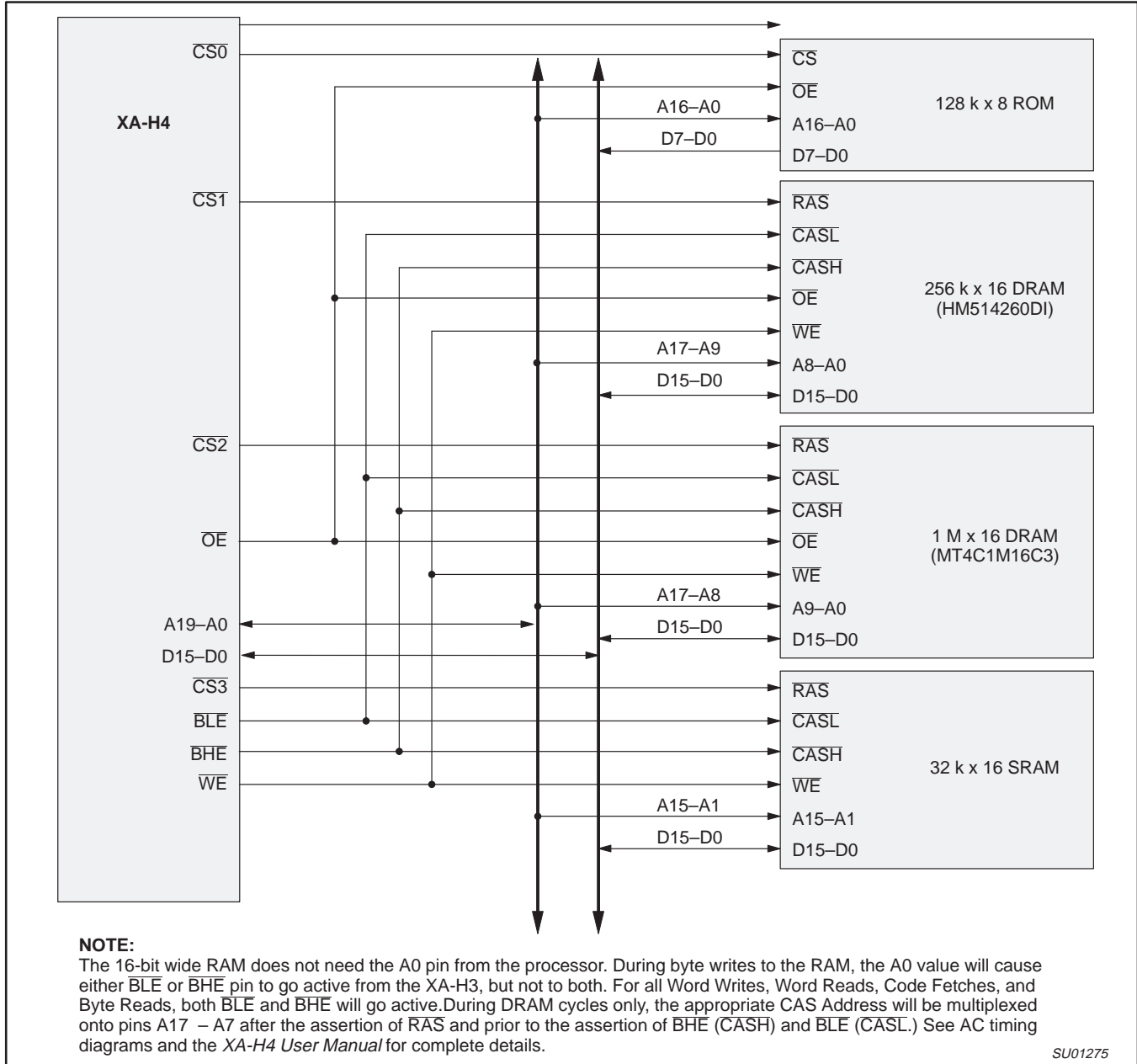


Figure 4. Typical system bus configuration

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Table 4. Memory interface control registers

| | Register Name | Reg Type | Description |
|-------|--|---------------|--|
| MRBH | “MMR Base Address” High | SFR 8 bits | This SFR is used to relocate the MMRs. It contains address bits a23 – a16 of the base address for the 4 kB Memory Mapped Register space. See the <i>XA-H4 User Manual</i> for using this SFR to relocate the MMRs. |
| MRBL | “MMR Base Address” Low | SFR 8 bits | Contains address bits a15 – a12 of the base address for the 4 kB Memory Mapped Register space. |
| MICFG | MIF Configuration | MMR 8 bits | Contains the ClkOut Enable bit. |
| MBCL | Memory Bank Configuration Lock | MMR 8 bits | Contains the bits for locking and unlocking the BiCFG Registers. |
| BiCFG | Bank i Configuration | MMR 8 bits | Contains the size, type, bus width, and enable bits for Memory Bank i. |
| BiAM | Bank i Base Address/DRAM Address Multiplexer Control | MMR 8 bits | Contains the base address bits and DRAM address multiplex control bits for Memory Bank i. |
| BiTMG | Bank i Timing | MMR 8 bits | Contains the timing control bits for Memory Bank i. |
| RFSH | Refresh Timing | MMR 8 bits | Contains the refresh time constant and DRAM Refresh Timer enable bit. |

EIGHT CHANNEL DMA CONTROLLER

The XA-H3/H4 has eight DMA channels; one Rx DMA channel dedicated to each USART Receive (Rx) channel, and one Tx DMA channel dedicated to each USART Transmit (Tx) channel. All DMA channels are optimized to support memory efficient circular data buffers in external memory. All DMA channels can also support traditional linear data buffers.

Transmit DMA Channel Modes

The four Tx channels have four DMA modes specifically designed for various applications of the attached USARTs. These modes are summarized in Table 5. Full details for all DMA functions can be found in the DMA chapter of the *XA-H4 User Manual*.

Table 5. Tx DMA modes summary

| Mode | Byte Count Source | Maskable Interrupt | Description |
|---------------------------|---|--|---|
| Non-SDLC/HDLC Tx Chaining | Header in memory | On stop | DMA channel picks up header from memory at the end of transmission. If the byte count in the header is greater than zero, then DMA transmits the number of bytes specified in the byte count. If byte count equals 0, then a maskable interrupt is generated. This process repeats until the byte count in the data header is zero. See <i>XA-H4 User Manual</i> for details. |
| SDLC/HDLC Tx Chaining | Header in memory | End of packet (not end of fragment) | Same as above, except DMA header distinguishes between fragment of packet and full pack. See <i>XA-H4 User Manual</i> for details. |
| Stop on TC | Processor loads Byte Count Register (for each fragment) | Byte count completed (Tx DMA stops) | Processor loads byte count into DMA. DMA sends that number of bytes, generates maskable interrupt, and stops. |
| Periodic Interrupt | Processor loads Byte Count Register (only once) | When Byte Counter reaches zero and is reloaded by DMA hardware from the byte count register. | DMA runs until commanded to stop by processor. Every time byte counter rolls over, a new maskable interrupt is generated. |

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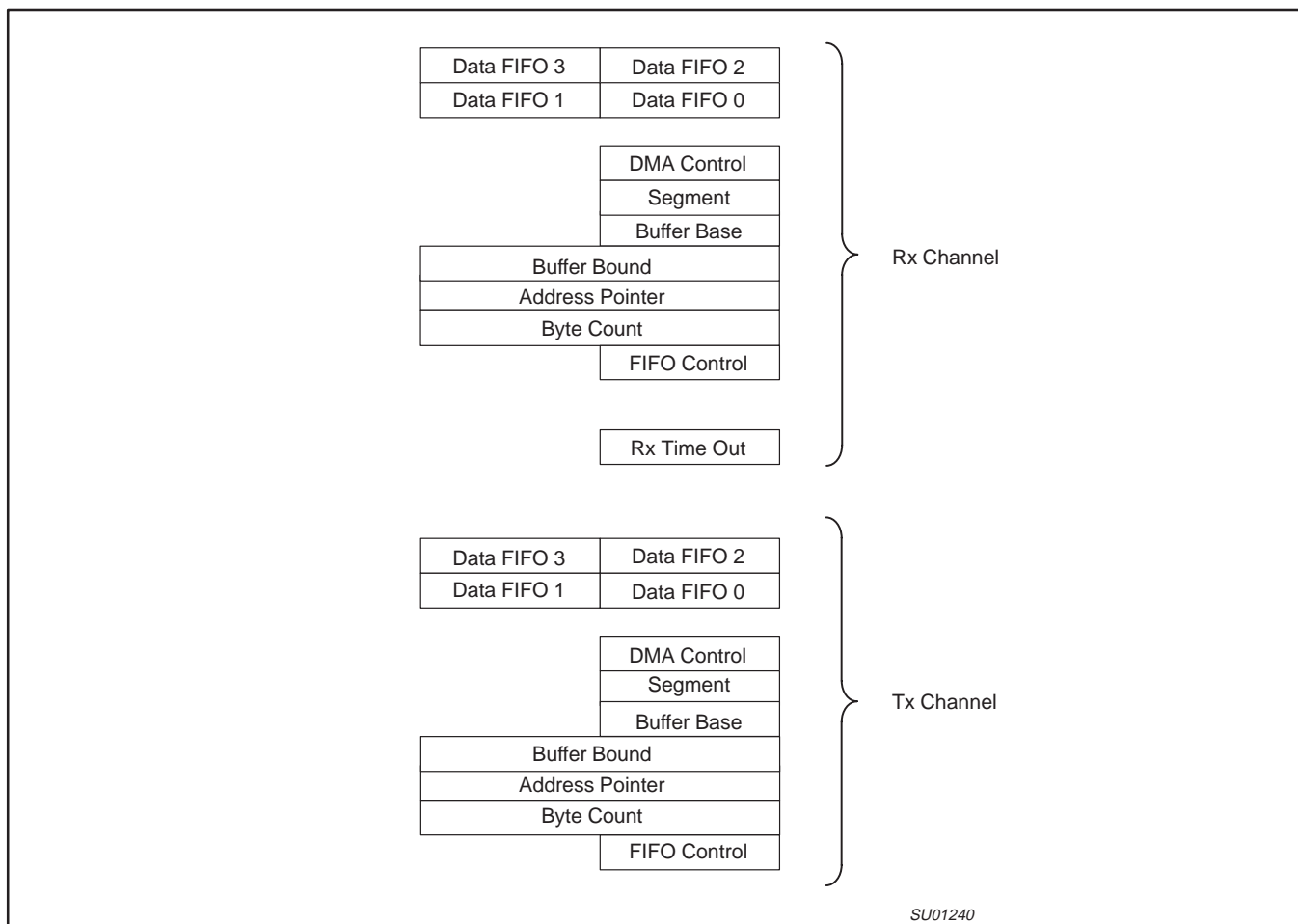
Receive DMA Channel Modes

The Rx DMA channels have four DMA modes specifically designed for various applications of the attached USARTs. These modes are

summarized in Table 6. For full details on implementation and use, see the *XA-H4 User Manual*.

Table 6. Rx DMA modes summary

| Mode | Byte Count Source | Maskable Interrupt | Description |
|---------------------------------|---|--|---|
| SDLC/HDLC Rx Chaining | DMA stores byte count in header in memory with data packet. | At end of received packet | When a complete or aborted SDLC/HDLC packet has been received, the packet byte count and status information are stored in memory with the packet. A maskable interrupt is generated. |
| Periodic Interrupt | Loaded by processor into DMA, used only to determine the number of bytes between interrupts. Processor can infer the byte count from the DMA address pointer. | When Byte Counter reaches zero and is reloaded by DMA hardware from the byte count register. | The DMA channel runs until commanded to stop by the processor. It generates a maskable interrupt once per <i>n</i> bytes, where <i>n</i> is the number written once into the byte count register by the processor, thus an interrupt is generated once every <i>n</i> received bytes. |
| Asynchronous Character Time Out | Byte Count can be calculated by software from the DMA address pointer. | If no character is received within a specified time out period, then interrupt. | Processor specifies time out period between incoming characters. If no character is received within that time, a maskable interrupt is generated. |
| Asynchronous Character Match | Byte Count can be calculated by software from the DMA address pointer. | When matched character is stored in memory. | There are four match registers, each incoming character is received within that time, a maskable interrupt is generated. When a matched character is stored in memory by DMA, a maskable interrupt is generated. |



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Figure 5. Rx and Tx DMA Registers

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DMA Registers

In addition to the 16-bit Global DMA Interrupt Register (which is shared by all eight DMA channels), each DMA channel has seven control registers and a four-byte Data FIFO. The four Rx DMA channels have one additional register, the Rx Character Time Out Register. All DMA registers can be read and written in Memory Mapped Register (MMR) space. These registers are summarized below.

- Global DMA Interrupt Register (not shown in figure): All DMA interrupt flags are in this register .
- DMA Control Register: Contains the master mode select and interrupt enable bits for the channel.
- Segment Register: Holds A23–A16 (the current segment) of the 24-bit data buffer address.
- Buffer Base Register: Holds a pointer (A15–A8) to the lowest byte in the memory buffer.
- Buffer Bound Register: Points to the first out-of-bounds address above a circular buffer.
- Address Pointer Register: Points to a single byte or word in the data buffer in memory. The 24-bit DMA address is formed by concatenating the contents of the Segment Register [A23–A16] with the contents of the Address Pointer Register [A15–A0].
- Byte Count Register: Holds the initial number of bytes to be transferred. In Tx Chaining mode, this register is not used because the byte count is brought into the byte counter from buffer headers in memory.
- FIFO Control & Status Register: Holds the queuing order and full/empty status for the Data FIFO Registers.
- Data FIFO Registers: A four-byte data FIFO buffer internal to the DMA channel.
- Rx Char Time Out Register (RxCTOR, Rx DMA channels only): Holds the initial value for an 8-bit character timeout countdown timer which can generate an interrupt.

Four USARTS

- Asynchronous features:
 - Asynchronous transfers up to 921.6 kbps
 - Can monitor input stream for up to four match characters per receiver (H4 only)
 - 5, 6, 7, or 8 data bits per character
 - 1, 1.5, or 2 Stop bits per character
 - Even or Odd parity generate and check
 - Parity, Rx Overrun, and Framing Error detection
 - Break detection
 - Supports hardware Autobaud detection and response up to 921.6 kbps.
- SDLC/HDLC features:
 - Automatic Flag and Abort Character generation and recognition
 - Automatic CRC generation and checking (can be disabled for “pass-thru”)
 - Automatic zero-bit insertion and stripping
 - Automatic partial byte residue code generation
 - 14-bit Packet byte count stored in memory with received packet by DMA

- Synchronous character-oriented protocol features (XA-H4 only):
 - Automatic CRC generation and checking
 - External Sync option
- Data encoding/decoding options:
 - FM0 (Biphase Space)
 - FM1 (Biphase Mark)
 - NRZ
 - NRZI
- Programmable Baud Rate Generator
- Auto Echo and Local Loopback modes

Autobaud Detectors

Each USART has its own Autobaud detector, capable of baud rate detection up to 921.6 kbaud. The detectors can be programmed to automatically echo the industry standard autobaud sequences. They can be programmed to update the necessary control registers in the USARTs and turn on the receiver, which in turn will automatically initiate DMA into memory of received data. Thus, once the baud rate is determined, reception begins without intervention from the processor. When the baud rate is detected, a maskable interrupt is sent to the processor. See the “Autobaud” chapter in the *XA-H4 User Manual* for details.

I/O Port Output Configuration

Port input/output configurations are the same as standard XA ports: open drain, quasi-bidirectional, push-pull, and off (off means tri-state Hi-Z, and allows the pin to be used as an input. **WARNING:** At power on time, from the time that power coming up is valid, the P3.2_Timer0_ResetOut pin may be driven low for any period from zero nanoseconds up to 258 system clocks. This is true independently of whether ResetIn is active or not.

Power Reduction Modes

The XA-H4 supports Idle and Power Down modes of power reduction. The idle mode leaves most peripherals running in order to allow them to activate the processor when an interrupt is generated. The power down mode stops the oscillator in order to absolutely minimize power. The processor can be made to exit power down mode via a reset or one of the external interrupt inputs (INT0 or INT1). This will occur if the interrupt is enabled and its priority is higher than that defined by IM3 through IM0. In power down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM} . This retains the RAM, register, and SFR contents at the point where power down mode was entered. **WARNING:** V_{DD} must be raised to within the operating range before power down mode is exited.

Interrupts

In the XA architecture, all exceptions, including Reset, are handled in the same general exception structure. The highest priority exception is, of course, Reset, and is non-maskable. All exceptions are vectored through the Exception Vector Table in low memory. Coming out of Reset, these vectors must be stored in non-volatile memory based at location 000000. Later in the boot sequence, DRAM or SRAM can be mapped into this address space if desired. There is a feature in the XA-H4 Memory Controller called “Bank Swap” that supports replacing the ROM vector table and other low memory with RAM. See the *XA-H4 User Manual* for details.

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The XA-H4 has a standard XA CPU Interrupt Controller, implemented with 15 Maskable Event Interrupts. Event Interrupts are defined as maskable interrupts usually generated by hardware events. However, in the XA-H4, 4 of the 15 Event Interrupts are generated by software writing directly to the interrupt flag bit. These 4 interrupts are referred to as "High Priority Software Interrupts."

See the *IC25 XA Data Handbook* for a full explanation of the exception structure, including event interrupts, of the XA CPU. Because the High Priority Software Interrupts are not implemented on all XA derivatives, they are explained in the *XA-H4 User Manual*.

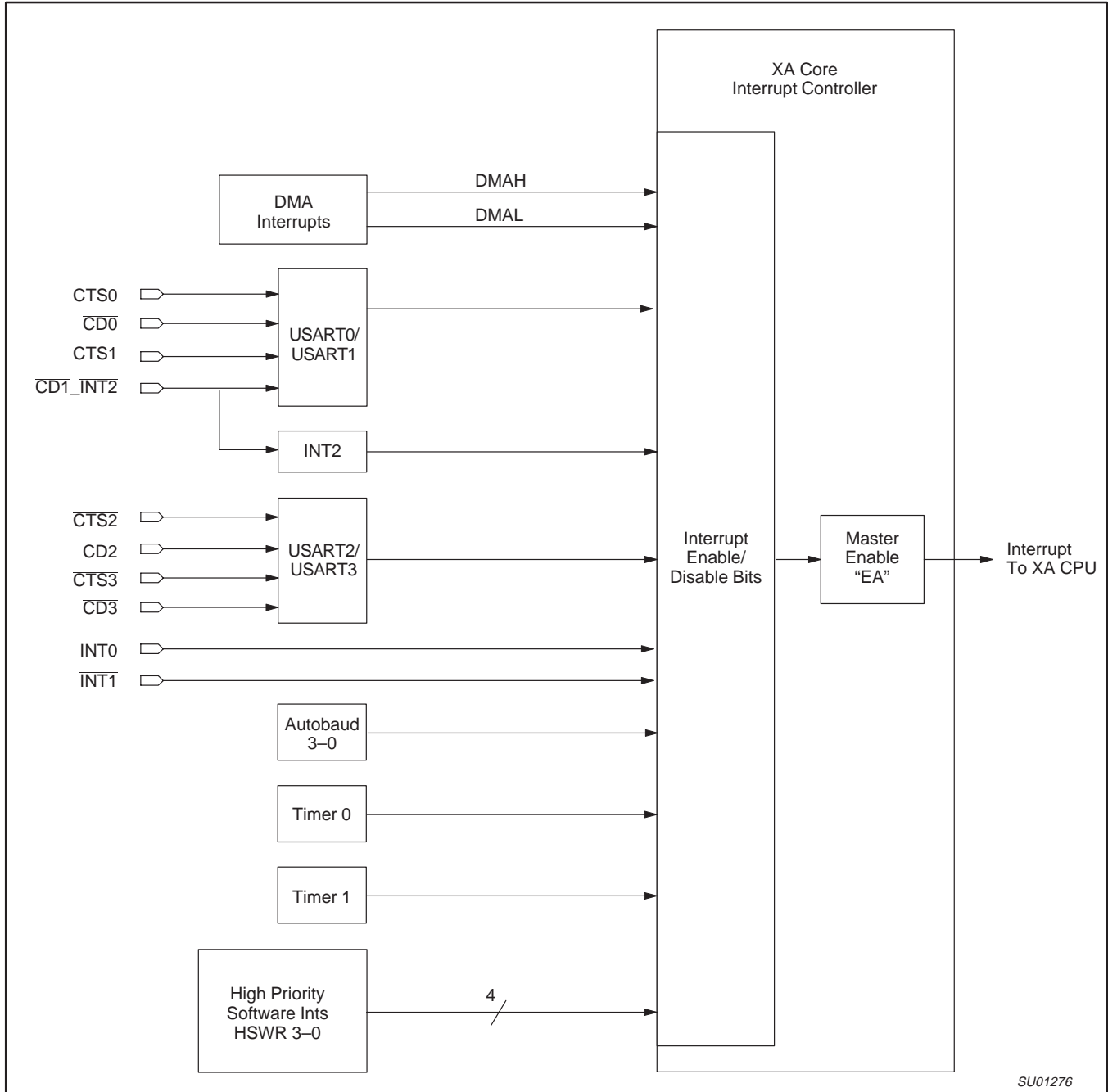


Figure 6. XA-H4 Interrupt Structure Overview

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Table 7. USART0 Interrupts (Interrupt structure is the same, except for bit locations, for all 4 USARTs)

| Potential USART0 Interrupt | Individual Enable Bit MMR Hex Offset | Source Bit MMR Hex Offset | Group Enable Bit(S) MMR Hex Offset | Group Flag Bit MMR Hex Offset | Master Enable Bit MMR Hex Offset |
|----------------------------|---|------------------------------|--|--|---|
| Rx Character Available | – | RR0[0] 820[0] | WR1[4:3] 802[4:3] | Even Channel Rx IP RR3[5] 826[5] | USART0/1 Master Interrupt Enable WR9[3] 812[3] |
| SDLC EOF (XA-H4 Only) | – | RR1[7] 822[7] | | | |
| CRC/Framing Error | – | RR1[6] 822[6] | | | |
| Rx Overrun | – | RR1[5] 822[5] | | | |
| Parity Error | WR1[2] 802[2] | RR1[4] 822[4] | | | |
| Tx Buffer Empty | See WR1[1] | RR0[2] 820[2] | Tx Interrupt Enable WR1[1] 802[1] | Even Channel Tx IP RR3[4] 826[4] | |
| Break/Abort | Break/ Abort IE WR15[7] 81E[7] | RR0[7] 820[7] | Master External/Status Interrupt Enable WR1[0] 802[0] | Even Channel External/Status IP RR3[3] 826[3] | |
| Tx Underrun/EOM | Tx Underrun/EOM IE WR15[6] 81E[6] | RR0[6] 820[6] | | | |
| CTS | CTS IE WR15[5] 81E[5] | RR0[5] 820[5] | | | |
| SYNC/HUNT (XA-H4 Only) | SYNC/ HUNT IE WR15[4] 81E[4] | RR0[4] 822[4] | | | |
| DCD | DCD IE WR15[3] 81E[3] | RR0[3] 820[3] | | | |
| Zero Count | Zero Count IE WR15[1] 81E[1] | RR0[1] 820[1] | | | |

EXCEPTION/TRAPS PRECEDENCE

| Description | Vector Address | Arbitration Ranking |
|----------------------------|----------------|---------------------|
| Reset (h/w, watchdog, s/w) | 0000–0003 | 0 (High) |
| Break Point | 0004–0007 | 1 |
| Trace | 0008–000B | 1 |
| Stack Overflow | 000C–000F | 1 |
| Divide by 0 | 0010–0013 | 1 |
| User RETI | 0014–0017 | 1 |
| TRAP 0–15 (software) | 0040–007F | 1 |

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EVENT INTERRUPTS

| Description Event Interrupt Source | Flag Bit | Interrupt Vector Address | Enable Bit (SFR) | Priority Register Bit Field (SFR) | Arb. Rank |
|------------------------------------|-------------------------------------|--------------------------|-------------------------|-----------------------------------|-----------|
| High Priority Software Interrupt 3 | H3WR3 MMR 2D0[15] | 00BF–00BC | E3HWR3 427[7] 33F | P3HWR3 4A7[6:4] | 17 |
| High Priority Software Interrupt 2 | H2WR2 MMR 2D0[14] | 00BB–00B8 | E2HWR2 427[6] 33E | P2HWR2 4A7[2:0] | 16 |
| High Priority Software Interrupt 1 | H1WR1 MMR 2D0[13] | 00B7–00B4 | E1HWR1 427[5] 33D | P1HWR1 4A6[6:4] | 15 |
| High Priority Software Interrupt 0 | H0WR0 MMR 2D0[12] | 00B3–00B0 | E0HWR0 427[4] 33C | P0HWR0 4A6[2:0] | 14 |
| USART "USART2/3" Interrupt | multiple OR from USART2 & USART3 | 00A7–00A4 | ESC23 427[1] 339 | PSC23 4A4[6:4] | 11 |
| USART "USART0/1" Interrupt | multiple OR from USART0 & USART1 | 00A3–00A0 | ESC01 427[0] 338 | PSC01 4A4[2:0] | 10 |
| DMA "DMAH" Interrupt | multiple OR from DMA | 009B–0098 | EDMAH 426[6] 336 | PDMAH 4A3[2:0] | 8 |
| DMA "DMAL" Interrupt | multiple OR from DMA | 0097–0094 | EDMAL 426[5] 335 | PDMAL 4A2[6:4] | 7 |
| External Interrupt 2 (INT2) | IE2 MMR 2D2[0] | 0093–0090 | EX2 426[4] 334 | PX2 4A2[2:0] | 6 |
| Timer 1 | TF1 SFR 410[7] 287 | 008F–008C | ET1 426[3] 333 | PT1 4A1[6:4] | 5 |
| External Interrupt 1 (INT1) | IE1 SFR 410[3] 283 | 008B–0088 | EX1 426[2] 332 | PX1 4A1[2:0] | 4 |
| Timer 0 | TF0 SFR 410[5] 285 | 0087–0084 | ET0 426[1] 331 | PT0 4A0[6:4] | 3 |
| External Interrupt 0 (INT0) | IE0 SFR 410[1] | 0083–0080 | EX0 426[0] 330 | PX0 4A0[2:0] | 2 |

SOFTWARE INTERRUPTS

| Description | Flag Bit | Vector Address | Enable Bit | Interrupt Priority |
|----------------------|----------|----------------|------------|--------------------|
| Software Interrupt 1 | SWR1 | 0100–0103 | SWE1 | (fixed at 1) |
| Software Interrupt 2 | SWR2 | 0104–0107 | SWE2 | (fixed at 2) |
| Software Interrupt 3 | SWR3 | 0108–010B | SWE3 | (fixed at 3) |
| Software Interrupt 4 | SWR4 | 010C–010F | SWE4 | (fixed at 4) |
| Software Interrupt 5 | SWR5 | 0110–0113 | SWE5 | (fixed at 5) |
| Software Interrupt 6 | SWR6 | 0114–0117 | SWE6 | (fixed at 6) |
| Software Interrupt 7 | SWR7 | 0118–011B | SWE7 | (fixed at 7) |

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ABSOLUTE MAXIMUM RATINGS

| Parameter | Rating | Unit |
|--|------------------------|------|
| Operating temperature under bias | -55 to +125 | °C |
| Storage temperature range | -65 to +150 | °C |
| Voltage on any other pin to V_{SS} | -0.5 to $V_{DD}+0.5$ V | v |
| Maximum I_{OL} per I/O pin | 15 | mA |
| Power dissipation (based on package heat transfer, not device power consumption) | 1.5 | W |

PRELIMINARY DC ELECTRICAL CHARACTERISTICS

$V_{DD} = 5.0$ V +/- 10% or 3.3 V +/- 10% unless otherwise specified; $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ for industrial, unless otherwise specified.

| Symbol | Parameter | Test Conditions | Limits | | | Unit |
|-----------|---|--|--------------|-----|---------------|---------------|
| | | | Min | Typ | Max | |
| I_{DD} | Power supply current, operating | 5.0 V, 30 MHz | | 64 | 80 | mA |
| | | 3.3 V, 30 MHz | | 55 | 70 | mA |
| I_{ID} | Power supply current, Idle mode | 5.0 V, 30 MHz | | 50 | 70 | mA |
| | | 3.3 V, 30 MHz | | 44 | 60 | mA |
| I_{PDI} | Power supply current, Power Down mode ¹ | 5.0 V, 3.0 V | | | 500 | μA |
| V_{RAM} | RAM keep-alive voltage | | 1.5 | | | V |
| V_{IL} | Input low voltage | | -0.5 | | $0.22 V_{DD}$ | V |
| V_{IH} | Input high voltage, except Xtal1, RST | | 2.2 | | | V |
| V_{IH1} | Input high voltage to Xtal1, RST | For both 3.0 & 5.0 V | $0.7 V_{DD}$ | | | V |
| V_{OL} | Output low voltage all ports ⁸ | $I_{OL} = 3.2$ mA, $V_{DD} = 4.5$ V | | | 0.5 | V |
| | | $I_{OL} = 1.0$ mA, $V_{DD} = 3.0$ V | | | 0.4 | V |
| V_{OH1} | Output high voltage, all ports | $I_{OH} = -100$ μA , $V_{DD} = 4.5$ V | 2.4 | | | V |
| | | $I_{OH} = -30$ μA , $V_{DD} = 3.0$ V | 2.0 | | | V |
| V_{OH2} | Output high voltage, all ports | $I_{OH} = 3.2$ mA, $V_{DD} = 4.5$ V | 2.4 | | | V |
| | | $I_{OH} = 1.0$ mA, $V_{DD} = 3.0$ V | 2.2 | | | V |
| C_{IO} | Input/Output pin capacitance | | | | 15 | pF |
| I_{IL} | Logical 0 input current, all ports ⁷ | $V_{IN} = 0.45$ V | | | -50 | μA |
| I_{LI} | Input leakage current, all ports ⁶ | $V_{IN} = V_{IL}$ or V_{IH} | | | ± 10 | μA |
| I_{TL} | Logical 1 to 0 transition current, all ports ⁵ | At $V_{DD} = 5.5$ V | | | -650 | μA |
| | | At $V_{DD} = 3.6$ V | | | -250 | μA |

NOTE:

- V_{DD} must be raised to within the operating range before power down mode is exited.
- Ports in quasi-bidirectional mode with weak pullup.
- Ports in PUSH-PULL mode, both pullup and pulldown assumed to be the same strength.
- In all output modes.
- Port pins source a transition current when used in quasi-bidirectional mode and externally driven from 1 to 0. This current is highest when V_{IN} is approximately 2 V.
- Measured with port in high impedance mode.
- Measured with port in quasi-bidirectional mode.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

| | |
|---|--|
| Maximum I_{OL} per port pin: | 15 mA (NOTE: This is $+85^{\circ}\text{C}$ specification for $V_{DD} = 5$ V) |
| Maximum I_{OL} per 8-bit port: | 26 mA |
| Maximum total I_{OL} for all outputs: | 71 mA |

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

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PRELIMINARY AC ELECTRICAL CHARACTERISTICS (5.0 V +/-10%) $V_{DD} = 5.0 \text{ V} \pm 10\%$; $T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (industrial)

| Symbol | Figure | Parameter | Limits | | Unit |
|---|--------------------------------------|--|--------------------|----------------|------|
| | | | Min | Max | |
| All Cycles | | | | | |
| F_C | | System Clock Frequency | 0 | 30 | MHz |
| t_C | 23 | System Clock Period = $1/F_C$ | 33.33 | – | ns |
| t_{CHCX} | 23 | XTALIN High Time | $t_C^* 0.5$ | – | ns |
| t_{CLCX} | 23 | XTALIN Low Time | $t_C^* 0.4$ | – | ns |
| t_{CLCH} | 23 | XTALIN Rise Time | – | 5 | ns |
| t_{CHCL} | 23 | XTALIN Fall Time | – | 5 | ns |
| t_{AVSL} | All | Address Valid to Strobe low | $t_C - 21$ | – | ns |
| t_{CHAH} | All | Address hold after ClkOut rising edge ⁹ | 1 | – | ns |
| t_{CHAV} | All | Delay from ClkOut rising edge to address valid | – | 25 | ns |
| t_{CHSH} | All | Delay from ClkOut rising edge to Strobe High ⁹ | 1 | 21 | ns |
| t_{CHSL} | All | Delay from ClkOut rising edge to Strobe Low ⁹ | 1 | 19 | ns |
| t_{CODH} | 24 | ClkOut Duty Cycle High (into 40 pF max.) | $t_{CHCX} - 7$ | $t_{CHCX} + 3$ | ns |
| t_{CPWH} | 11, 12, 17, 18, 19, 20 | \overline{CAS} Pulse Width High | $t_C - 12$ | – | ns |
| t_{CPWL} | 11, 19 | \overline{CAS} Pulse Width Low | $t_C - 10$ | – | ns |
| All DRAM Cycles | | | | | |
| t_{RP} | 22 | RAS precharge time, thus minimum RAS high time ⁸ | $(n * t_C) - 16^8$ | – | ns |
| Generic Data Read Only | | | | | |
| t_{AHDR} | 7, 14 | Address hold (A19 – A1 only, not A0) after \overline{CS} , \overline{BLE} , \overline{BHE} rise at end of Generic Data Read Cycle (not code fetch) | $t_C - 12$ | – | ns |
| Data Read and Instruction Fetch Cycles | | | | | |
| t_{DIS} | 7, 8, 10, 11, 12, 14, 15, 17, 18, 19 | Data In Valid setup to ClkOut rising edge | 25 | – | ns |
| t_{DIH} | 7, 8, 10, 14, 15, 17, 18 | Data In Valid hold after ClkOut rising edge ² | 0 | – | ns |
| t_{OHDE} | 8, 10, 11, 14, 18 | \overline{OE} high to XA Data Bus Driver Enable | $t_C - 14$ | – | ns |
| Write Cycles | | | | | |
| t_{CHDV} | 9, 13 | Clock High to Data Valid | – | 25 | ns |
| t_{DVSL} | 16, 20 | Data Valid prior to Strobe Low | $t_C - 23$ | – | ns |
| t_{SHAH} | 9, 16 | Minimum Address Hold Time after strobe goes inactive | $t_C - 25$ | – | ns |
| t_{SHDH} | 9, 16 | Data hold after strobes (\overline{CS} and $\overline{BHE}/\overline{BLE}$) high | $t_C - 25$ | – | ns |
| Refresh | | | | | |
| t_{CLRL} | 21 | \overline{CAS} low to \overline{RAS} low | $t_C - 15$ | – | ns |
| Wait Input | | | | | |
| t_{WS} | 25 | WAIT setup (stable high or low) to ClkOut rising edge | 20 | – | ns |
| t_{WH} | 25 | WAIT hold (stable high or low) after ClkOut rising edge | 0 | – | ns |

NOTE:

1. See notes after the 3.3 V AC Timing Table

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AC ELECTRICAL CHARACTERISTICS (3.3 V +/-10%) $V_{DD} = 3.3 \text{ V} \pm 10\%$; $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (industrial)

| Symbol | Figure | Parameter | Limits | | Unit |
|---|--------------------------------------|---|--------------------|----------------|------|
| | | | Min | Max | |
| All Cycles | | | | | |
| F_C | | System Clock (internally called CClk) Frequency | 0 | 30 | MHz |
| t_C | 23 | System Clock Period = $1/F_C$ | 33.33 | – | ns |
| t_{CHCX} | 23 | XTALIN High Time | $t_C * 0.5$ | – | ns |
| t_{CLCX} | 23 | XTALIN Low Time | $t_C * 0.4$ | – | ns |
| t_{CLCH} | 23 | XTALIN Rise Time | – | 5 | ns |
| t_{CHCL} | 23 | XTALIN Fall Time | – | 5 | ns |
| t_{AVSL} | All | Address Valid to Strobe low | $t_C - 21$ | – | ns |
| t_{CHAH} | All | Address hold after ClkOut rising edge ⁹ | 1 | – | ns |
| t_{CHAV} | All | Delay from ClkOut rising edge to address valid | – | 30 | ns |
| t_{CHSH} | All | Delay from ClkOut rising edge to Strobe High ⁹ | 1 | 28 | ns |
| t_{CHSL} | All | Delay from ClkOut rising edge to Strobe Low ⁹ | 1 | 25 | ns |
| t_{CODH} | 24 | ClkOut Duty Cycle High (into 40 pF max.) | $t_{CHCX} - 7$ | $t_{CHCX} + 3$ | ns |
| t_{CPWH} | 11, 12, 17, 18, 19, 20 | $\overline{\text{CAS}}$ Pulse Width High | $t_C - 12$ | – | ns |
| t_{CPWL} | 11, 19 | $\overline{\text{CAS}}$ Pulse Width Low | $t_C - 10$ | – | ns |
| All DRAM Cycles | | | | | |
| t_{RP} | 22 | $\overline{\text{RAS}}$ precharge time, thus minimum $\overline{\text{RAS}}$ high time ⁸ | $(n * t_C) - 16^8$ | – | ns |
| Data Read Only | | | | | |
| t_{AHDR} | 7, 14 | Address hold (A19 – A1 only, not A0) after $\overline{\text{CS}}$, $\overline{\text{BLE}}$, $\overline{\text{BHE}}$ rise at end of Data Read Cycle (not code fetch) | $t_C - 12$ | – | ns |
| Data Read and Instruction Fetch Cycles | | | | | |
| t_{DIS} | 7, 8, 10, 11, 12, 14, 15, 17, 18, 19 | Data In Valid setup to ClkOut rising edge | 32 | – | ns |
| t_{DIH} | 7, 8, 10, 14, 15, 17, 18 | Data In Valid hold after ClkOut rising edge ² | 0 | – | ns |
| t_{OHDE} | 8, 10, 11, 14, 18 | $\overline{\text{OE}}$ high to XA Data Bus Driver Enable | $t_C - 19$ | – | ns |
| Write Cycles | | | | | |
| t_{CHDV} | 9, 13 | Clock High to Data Valid | – | 30 | ns |
| t_{DVSL} | 16, 20 | Data Valid prior to Strobe Low | $t_C - 23$ | – | ns |
| t_{SHAH} | 9, 16 | Minimum Address Hold Time after strobe goes inactive | $t_C - 25$ | – | ns |
| t_{SHDH} | 9, 16 | Data hold after strobes ($\overline{\text{CS}}$ and $\overline{\text{BHE/BLE}}$) high | $t_C - 25$ | – | ns |
| Refresh | | | | | |
| t_{CLRL} | 21 | $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ low | $t_C - 15$ | – | ns |
| Wait Input | | | | | |
| t_{WS} | 25 | WAIT setup (stable high or low) prior to ClkOut rising edge | 25 | – | ns |
| t_{WH} | 25 | WAIT hold (stable high or low) after ClkOut rising edge | 0 | – | ns |

NOTE:

- On a 16-bit bus, if only one byte is being written, then only one of $\overline{\text{BLE_CASL}}$ or $\overline{\text{BHE_CASH}}$ will go active. On an 8-bit bus, $\overline{\text{BLE_CASL}}$ goes active for all (odd or even address) accesses. $\overline{\text{BHE_CASH}}$ will not go active during any accesses on an 8-bit bus.
- The bus timing is designed to make meeting hold time very straightforward without glue logic. On all generic reads and fetches, in order to meet hold time, the slave should hold data valid on the bus until the earliest of $\overline{\text{CS}}$, $\overline{\text{BHE/BLE}}$, $\overline{\text{OE}}$, goes high (inactive), or until the address changes. On all FPM DRAM reads and fetches, hold data valid on the bus until a new $\overline{\text{CAS}}$ is asserted, or until $\overline{\text{OE}}$ goes high (inactive).
- To avoid 3-State fights during read cycles and fetch cycles, do not drive data bus until $\overline{\text{OE}}$ goes active.
- To meet hold time, EDO DRAM drives data onto the bus until $\overline{\text{OE}}$ rises, or until a new falling edge of $\overline{\text{CAS}}$.
- WARNING: ClkOut is specified at 40 pF max.** More than 40 pF on ClkOut may significantly degrade the ClkOut waveform. Load capacitance for all outputs (except ClkOut) = 80 pF.
- Not all combinations of bus timing configuration values result in valid bus cycles. Please refer to the *XA-H4 User Manual* for details.
- When code is being fetched on the external bus, a burst mode fetch is used. This burst can be from 2 to 16 bytes long. On a 16-bit bus, A3 – A1 are incremented for each new word of the burst. On an 8-bit bus, A3 – A0 are incremented for each new byte of the burst code fetch.

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8. t_{RP} is specified as the minimum high time (thus inactive) on each of the 5 individual $\overline{CS_RAS}[5:1]$ pins when such pin is programmed in the memory controller to service DRAM. The number of CClks (system clocks) in t_{RP} is programmable, and is represented by n in the t_{RP} equation in the AC tables. Regardless of what value is programmed into the control register, n will never be less than 2 clocks. Thus, at 30 Mhz system clock, the minimum value for \overline{RAS} precharge is $t_{RP} = ((2 * t_C) - 16) = ((2 * 33.33) - 16) = 50.6$ ns. As the system clock frequency F_C , is slowed down, t_C (system clock period) of course becomes greater, and thus t_{RP} becomes greater.
9. The MIN value for this parameter is guaranteed by design and is not tested in production to the specified limit. In those cases where a maximum value is specified in the table for this parameter, it is tested.

TIMING DIAGRAMS

All references to numbered Notes are to the notes following the AC Electrical Characteristics tables

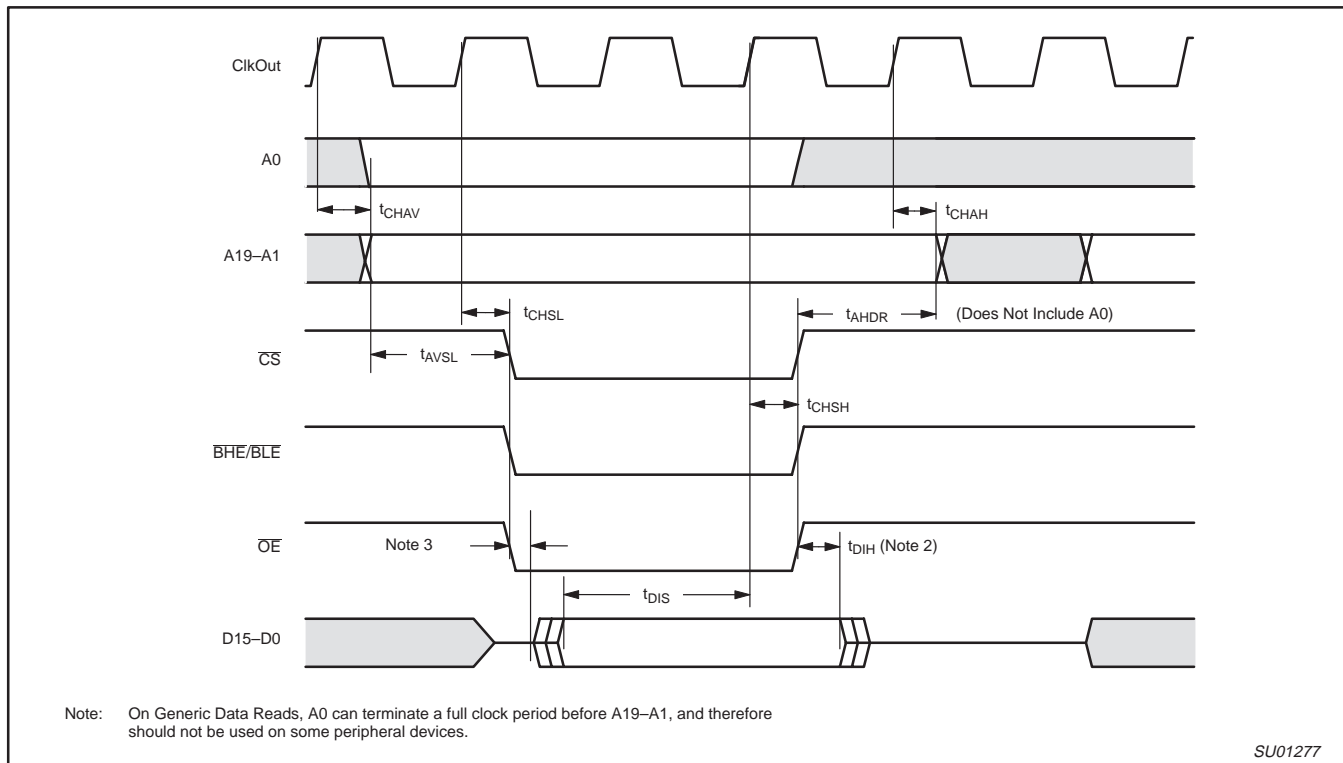


Figure 7. Generic (SRAM, ROM, Flash, I/O Devices, etc.) Read on 16-Bit Bus

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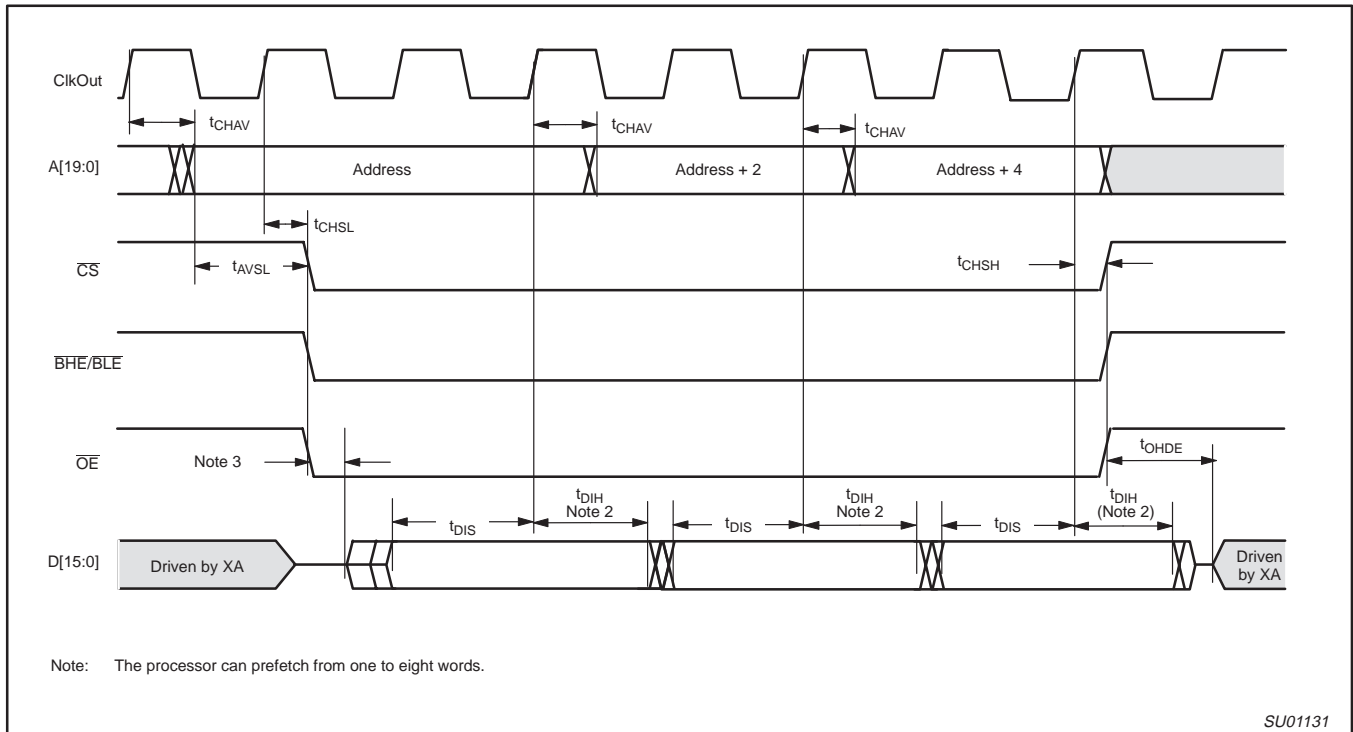


Figure 8. Generic (SRAM, ROM, Flash, etc.) Burst Code Fetch on 16-Bit Bus

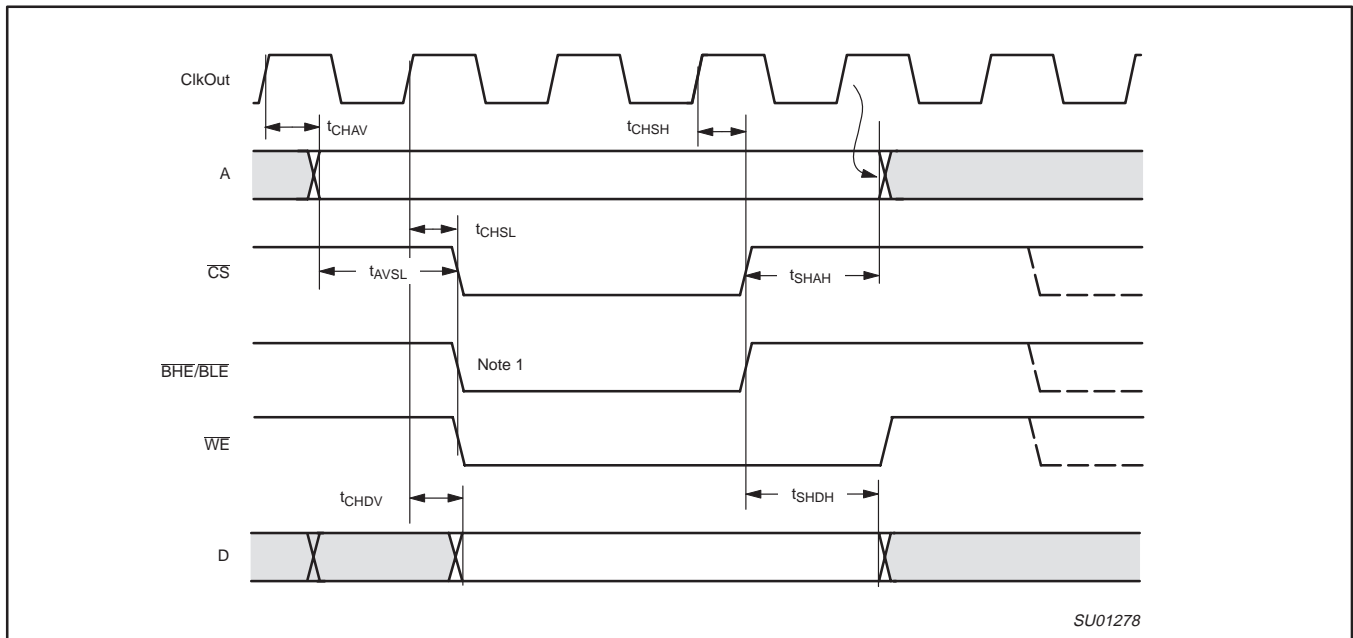


Figure 9. Generic (SRAM, I/O Devices, etc.) Write

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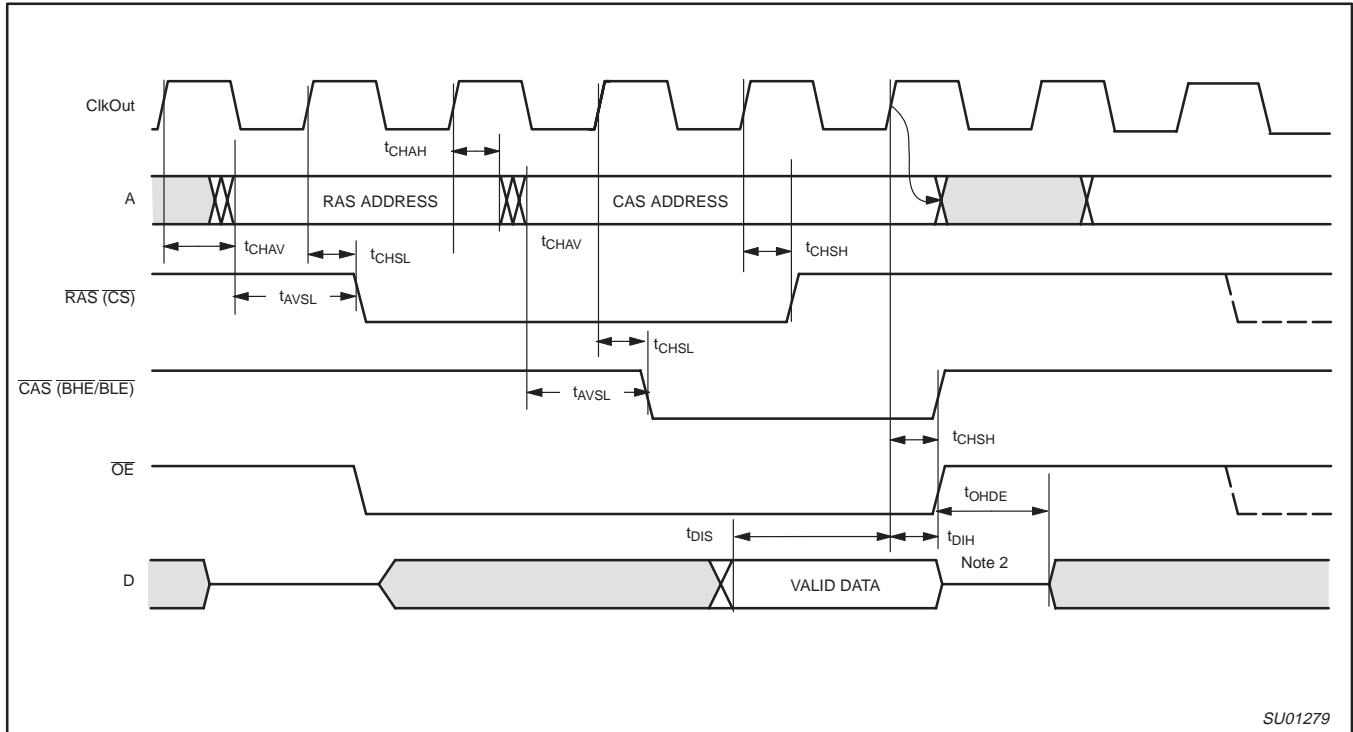
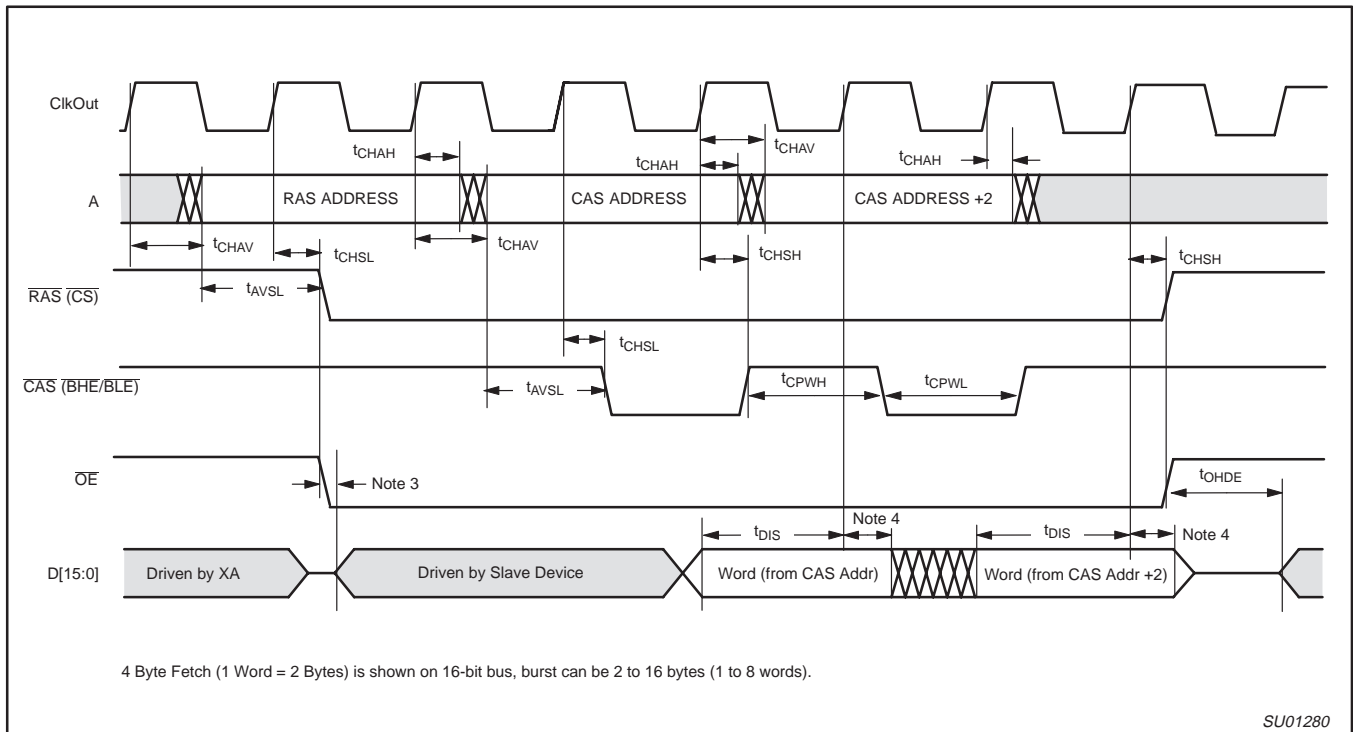


Figure 10. DRAM Single Read Cycle



4 Byte Fetch (1 Word = 2 Bytes) is shown on 16-bit bus, burst can be 2 to 16 bytes (1 to 8 words).

Figure 11. DRAM EDO Burst Code Fetch on 16-Bit Bus

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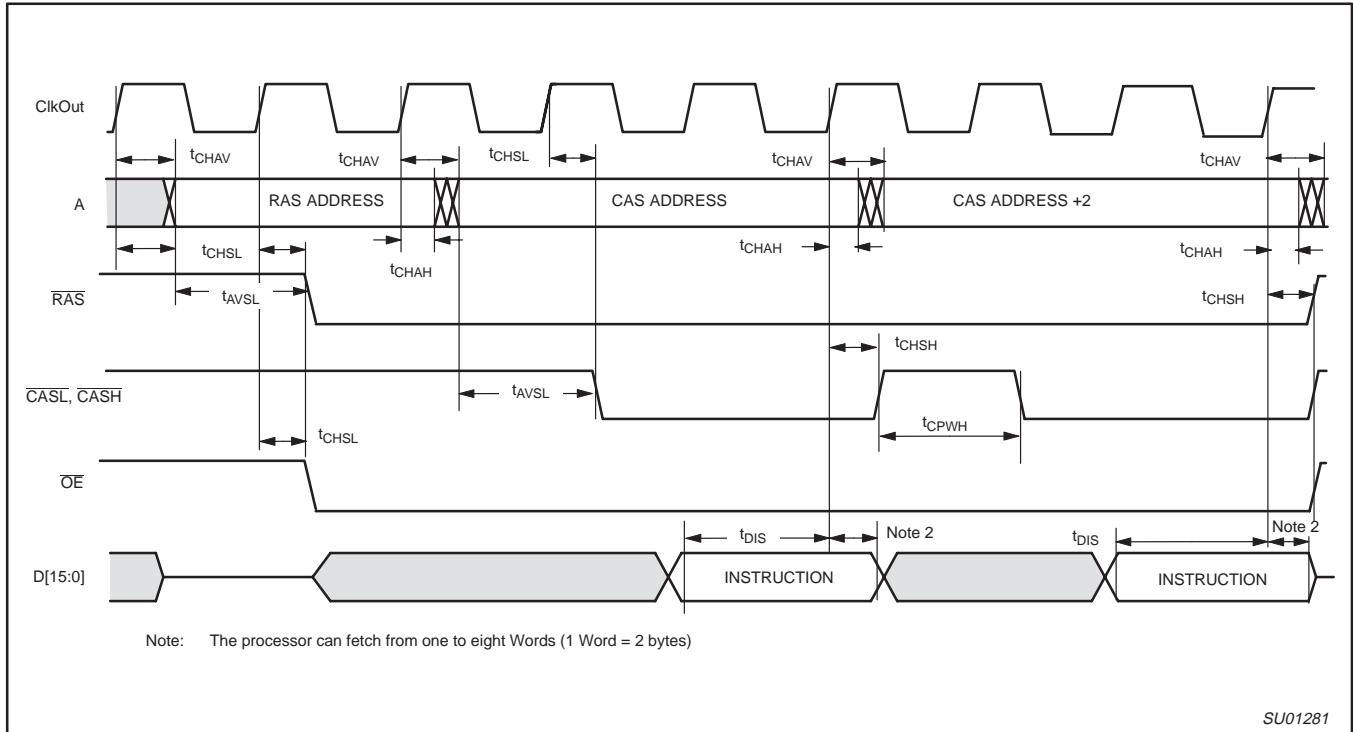


Figure 12. DRAM FPM (Fast Page Mode) Burst Code Fetch

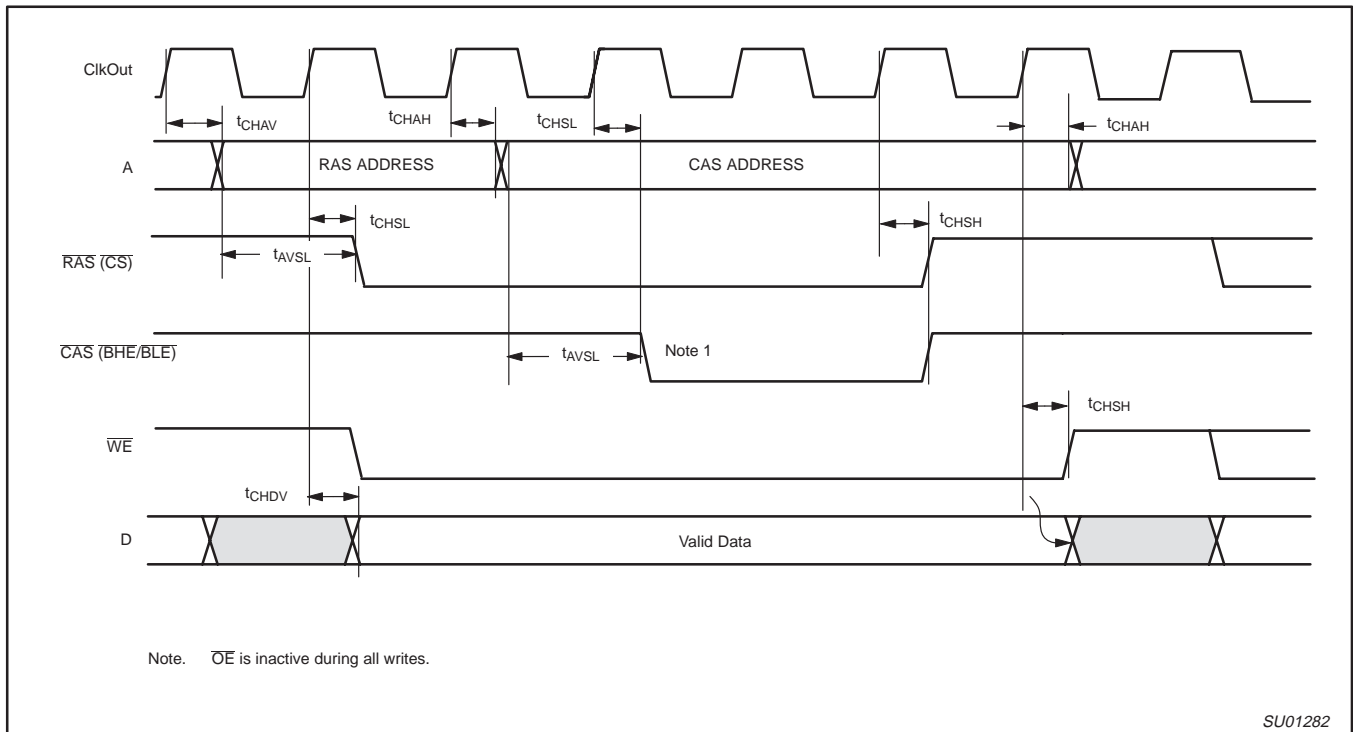


Figure 13. DRAM Write (on 16-Bit Bus, also 8-Bit Write on 8-Bit Bus)

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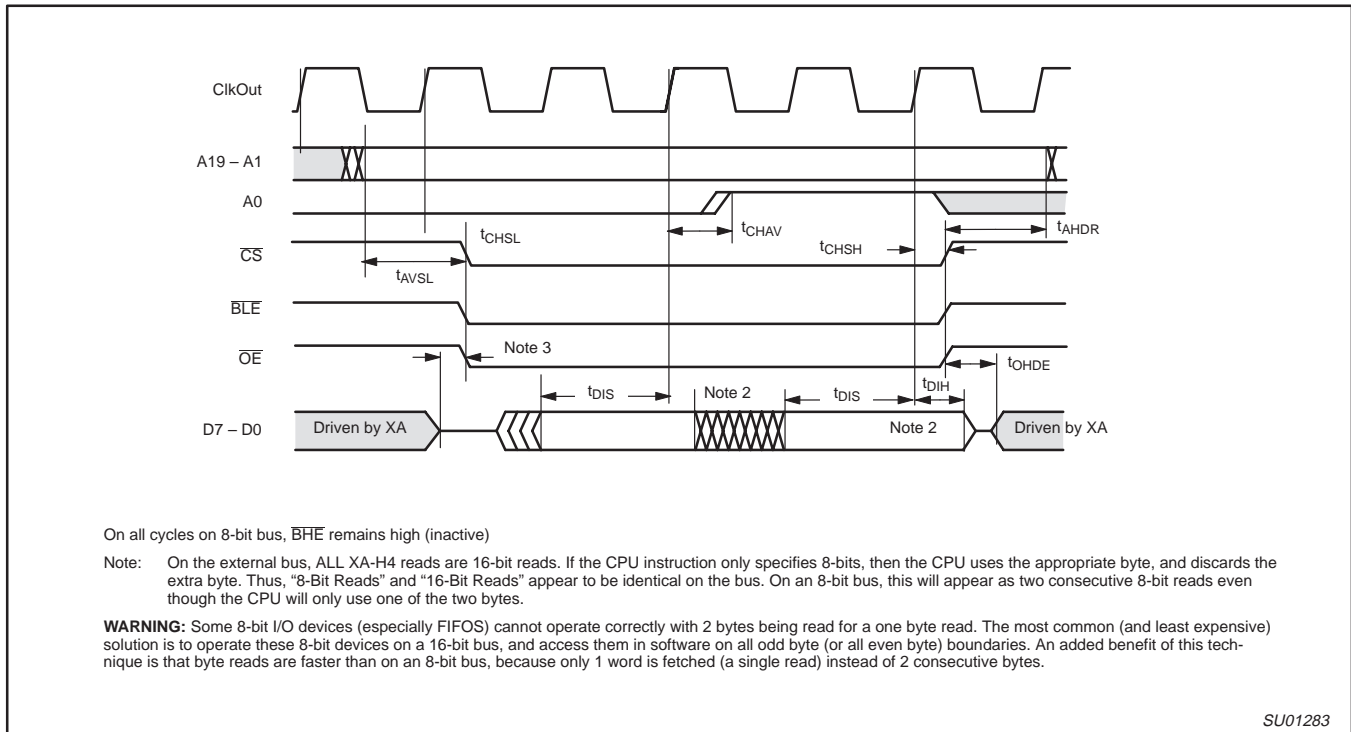


Figure 14. Generic (SRAM, Flash, I/O Device, etc.) Read (16-Bit or 8-Bit) on 8-Bit Bus

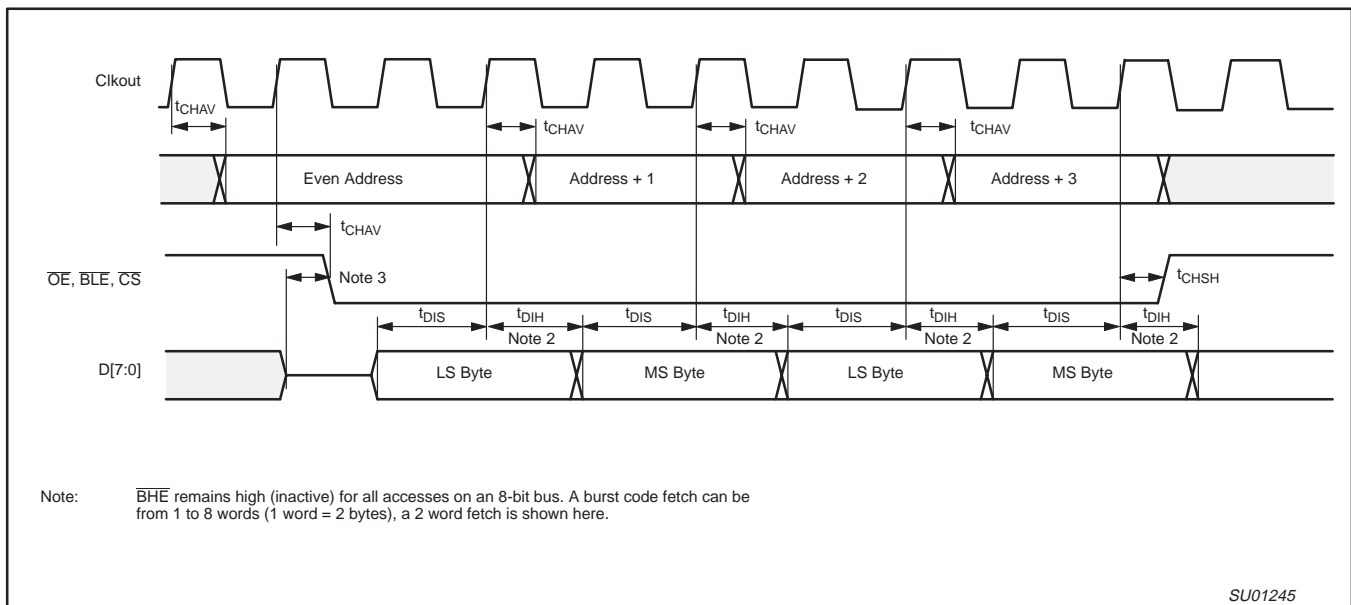


Figure 15. Burst Code Fetch on 8-Bit Bus, Generic Memory

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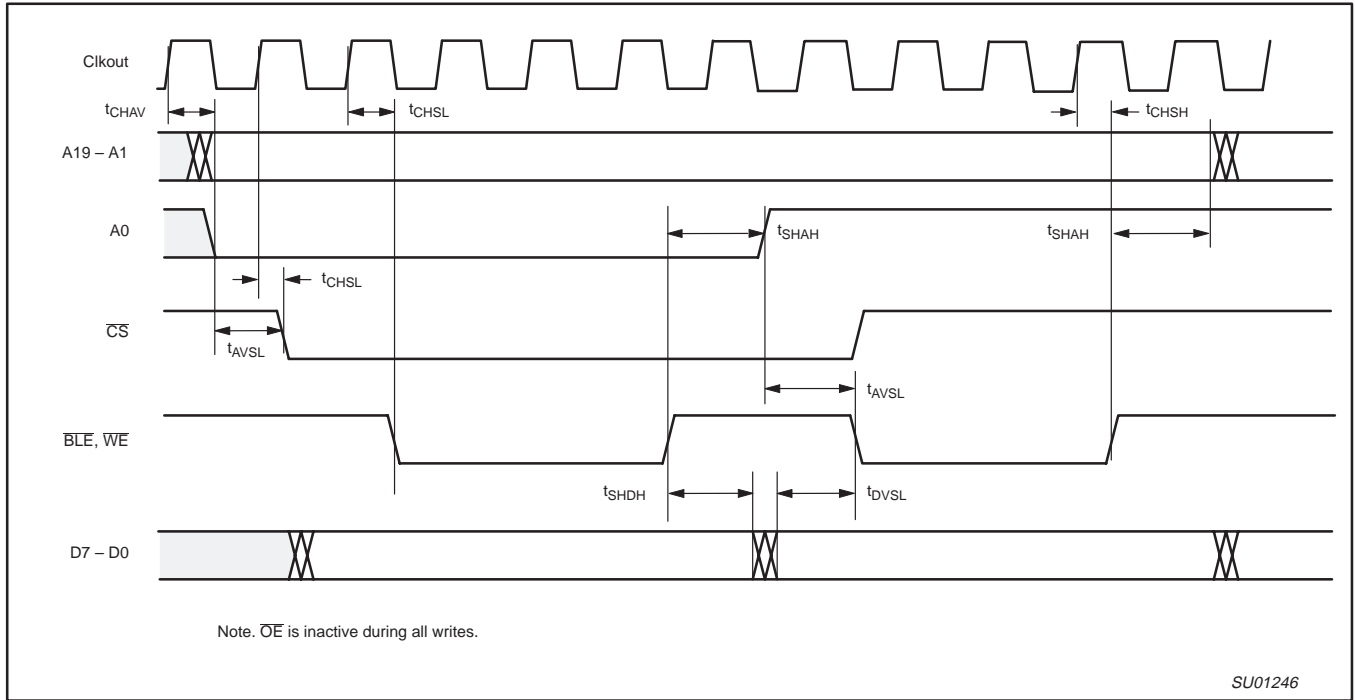


Figure 16. Generic 16-Bit Write on 8-Bit Bus

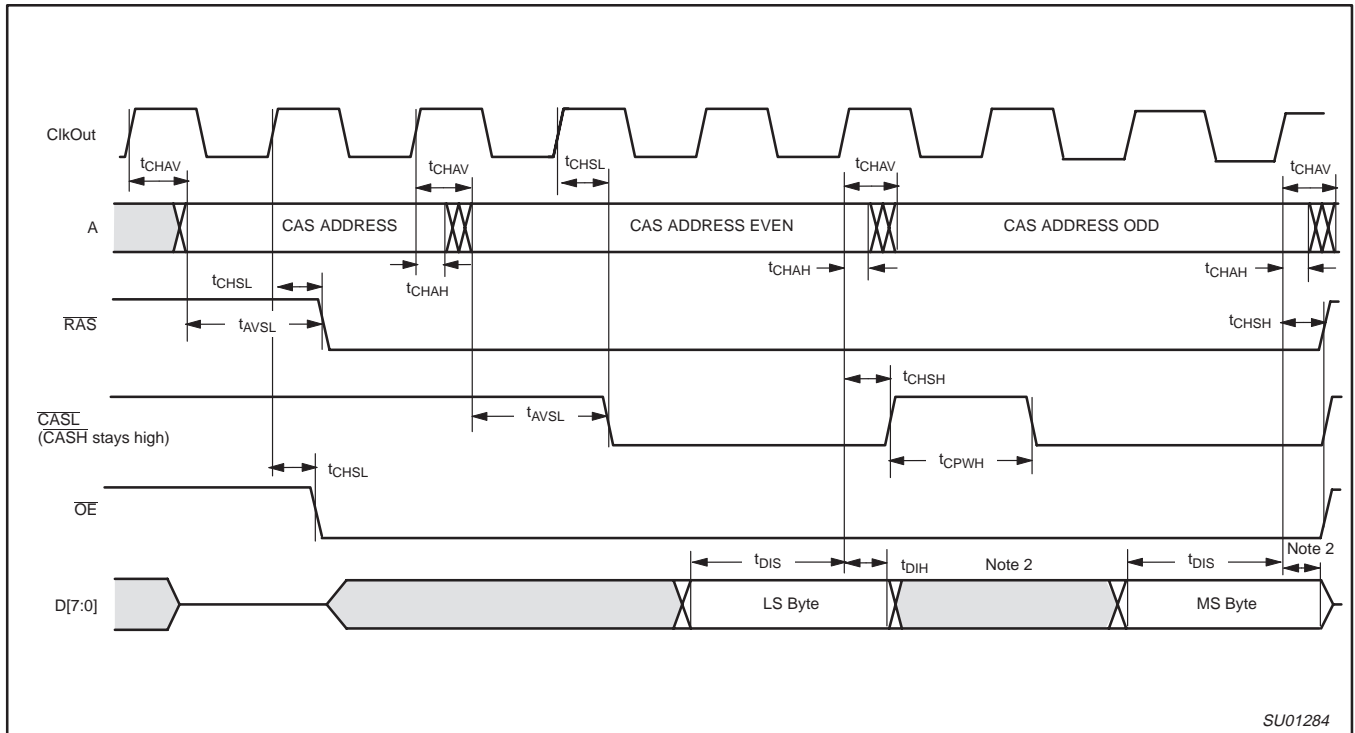


Figure 17. 16-Bit Read on 8-Bit Bus, DRAM (both FPM and EDO)

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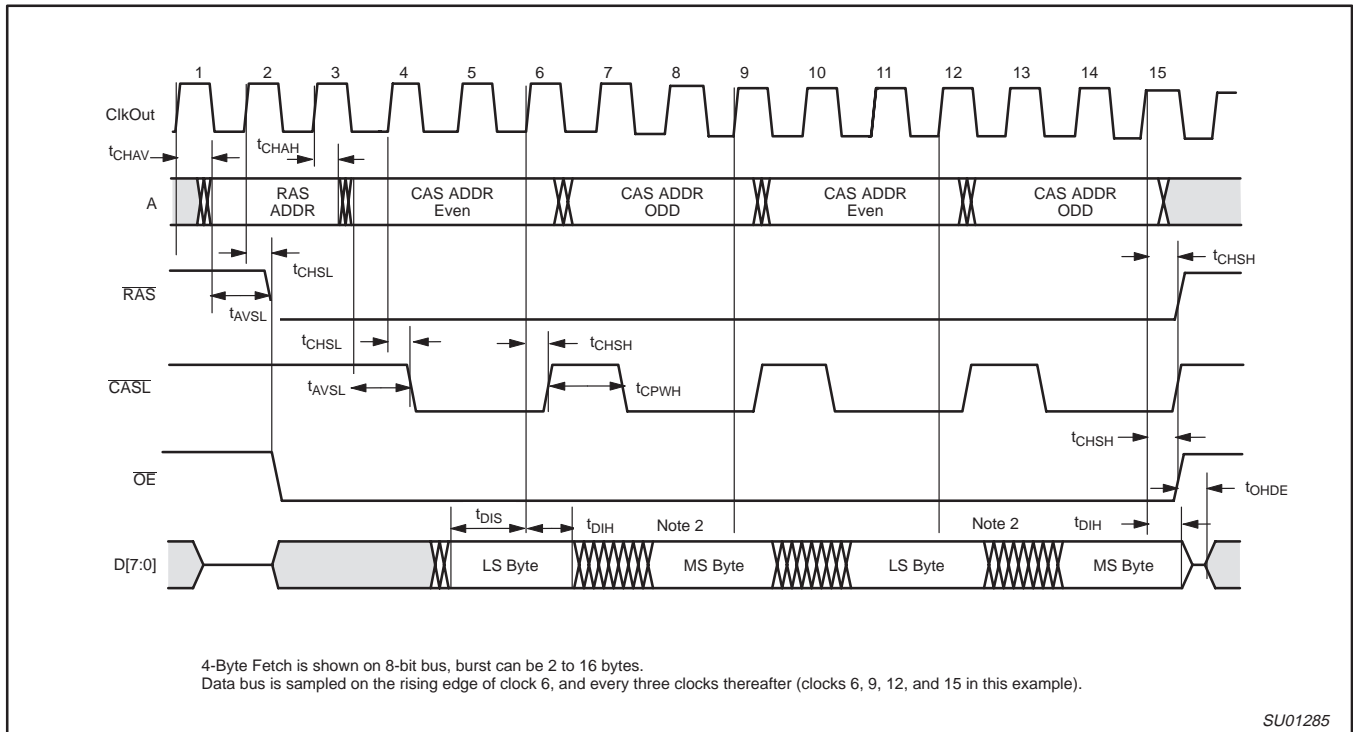


Figure 18. DRAM FPM (Fast Page Mode) Burst Code Fetch on 8-Bit Bus

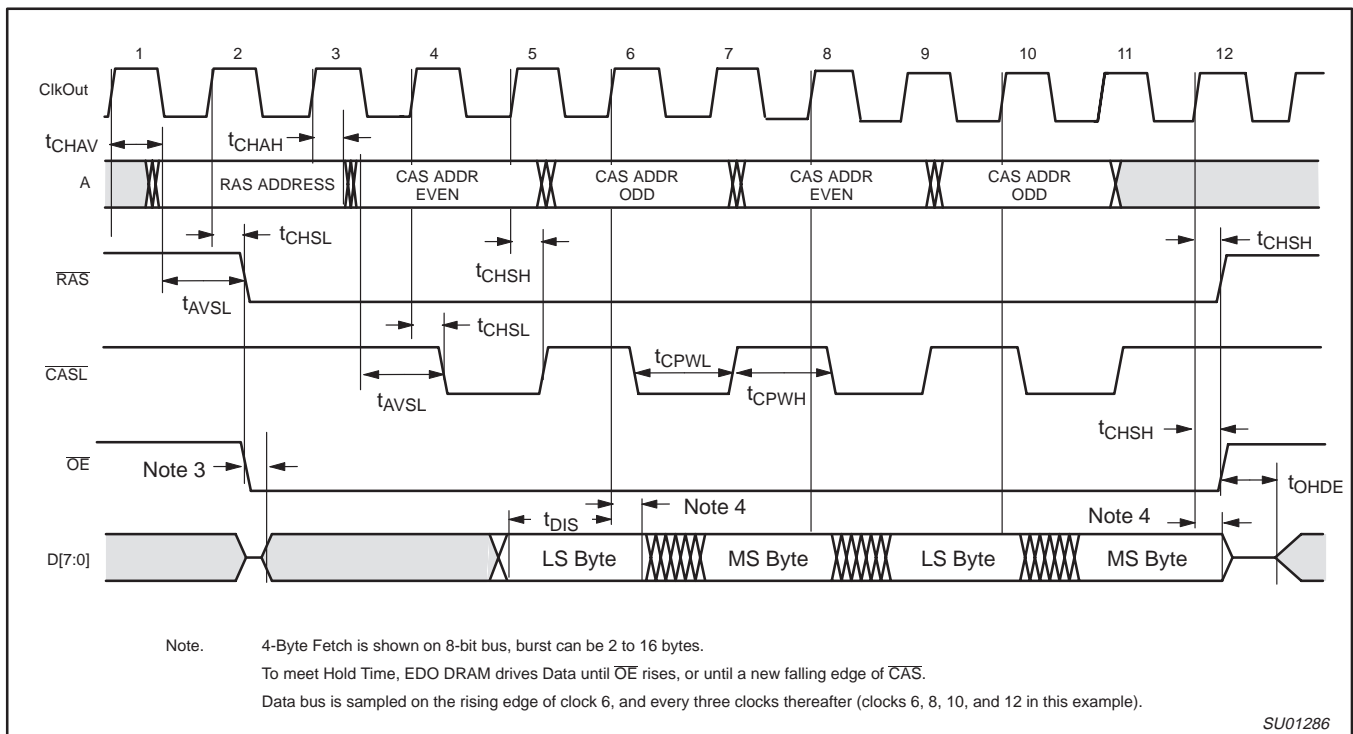


Figure 19. EDO DRAM Burst Code Fetch on 8-Bit Bus

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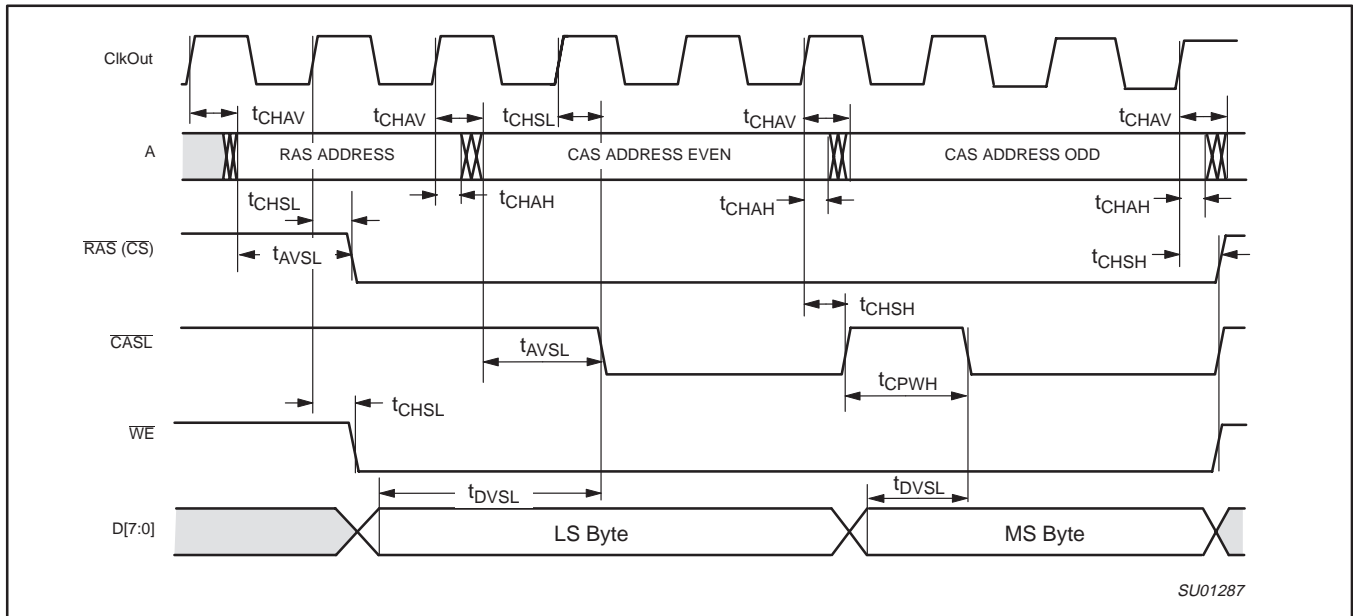
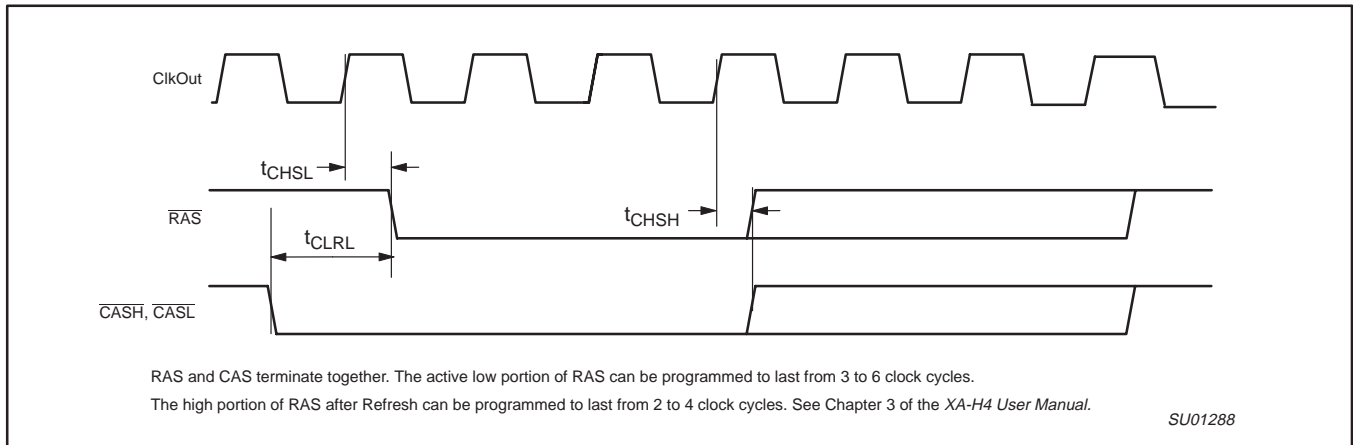


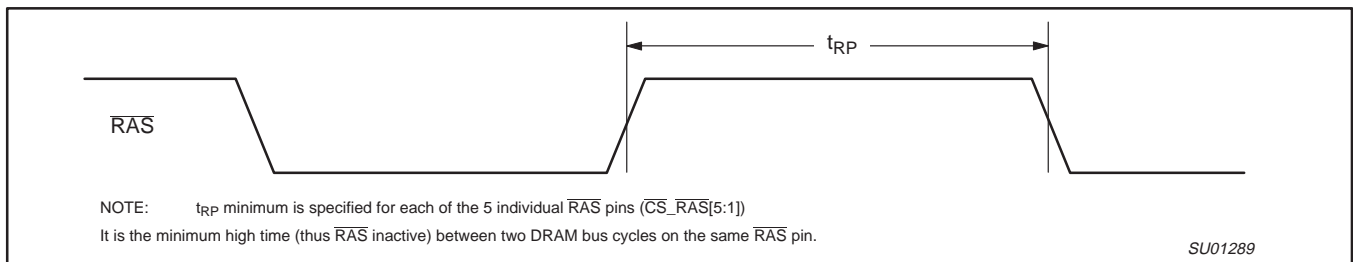
Figure 20. DRAM 16-Bit Write on 8-Bit Bus (FPM or EDO DRAMs)



RAS and CAS terminate together. The active low portion of RAS can be programmed to last from 3 to 6 clock cycles. The high portion of RAS after Refresh can be programmed to last from 2 to 4 clock cycles. See Chapter 3 of the XA-H4 User Manual.

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Figure 21. REFRESH



NOTE: t_{RP} minimum is specified for each of the 5 individual \overline{RAS} pins ($\overline{CS_RAS}[5:1]$). It is the minimum high time (thus \overline{RAS} inactive) between two DRAM bus cycles on the same \overline{RAS} pin.

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Figure 22. \overline{RAS} Precharge Time

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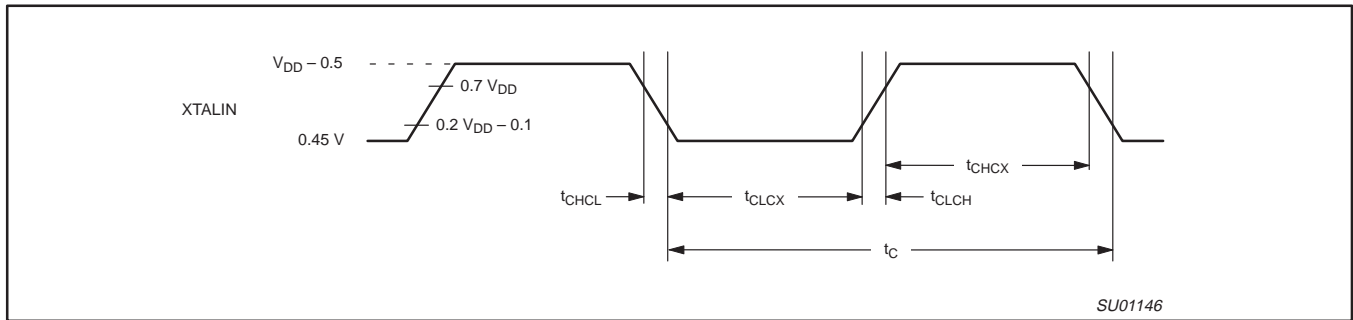


Figure 23. External Clock Input Drive

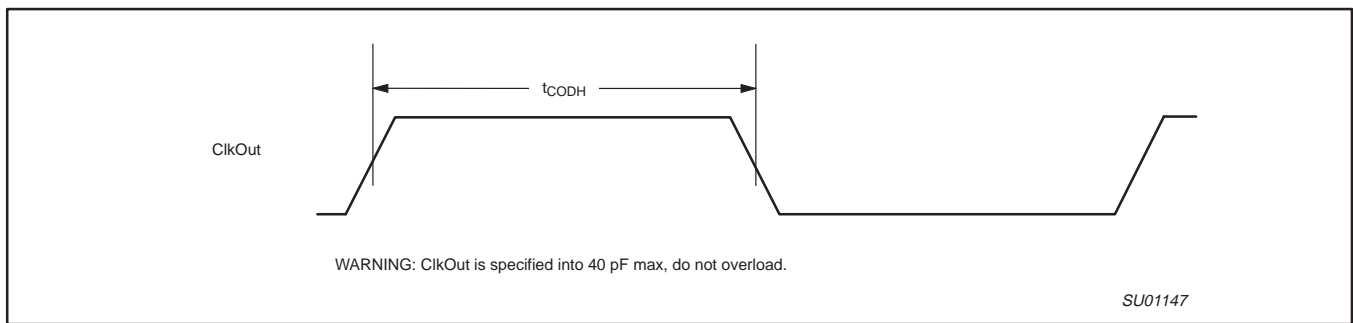


Figure 24. ClkOut Duty Cycle

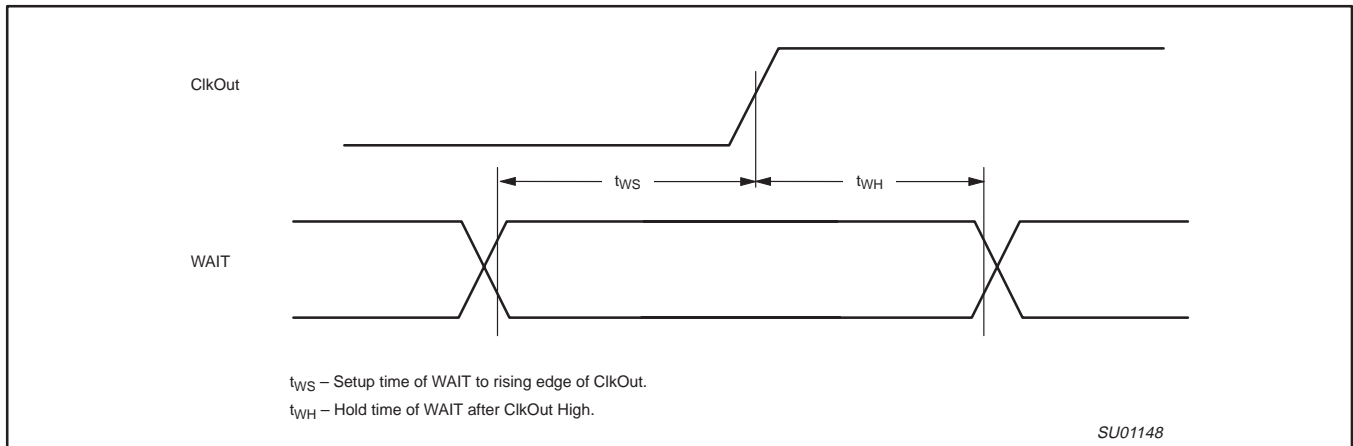


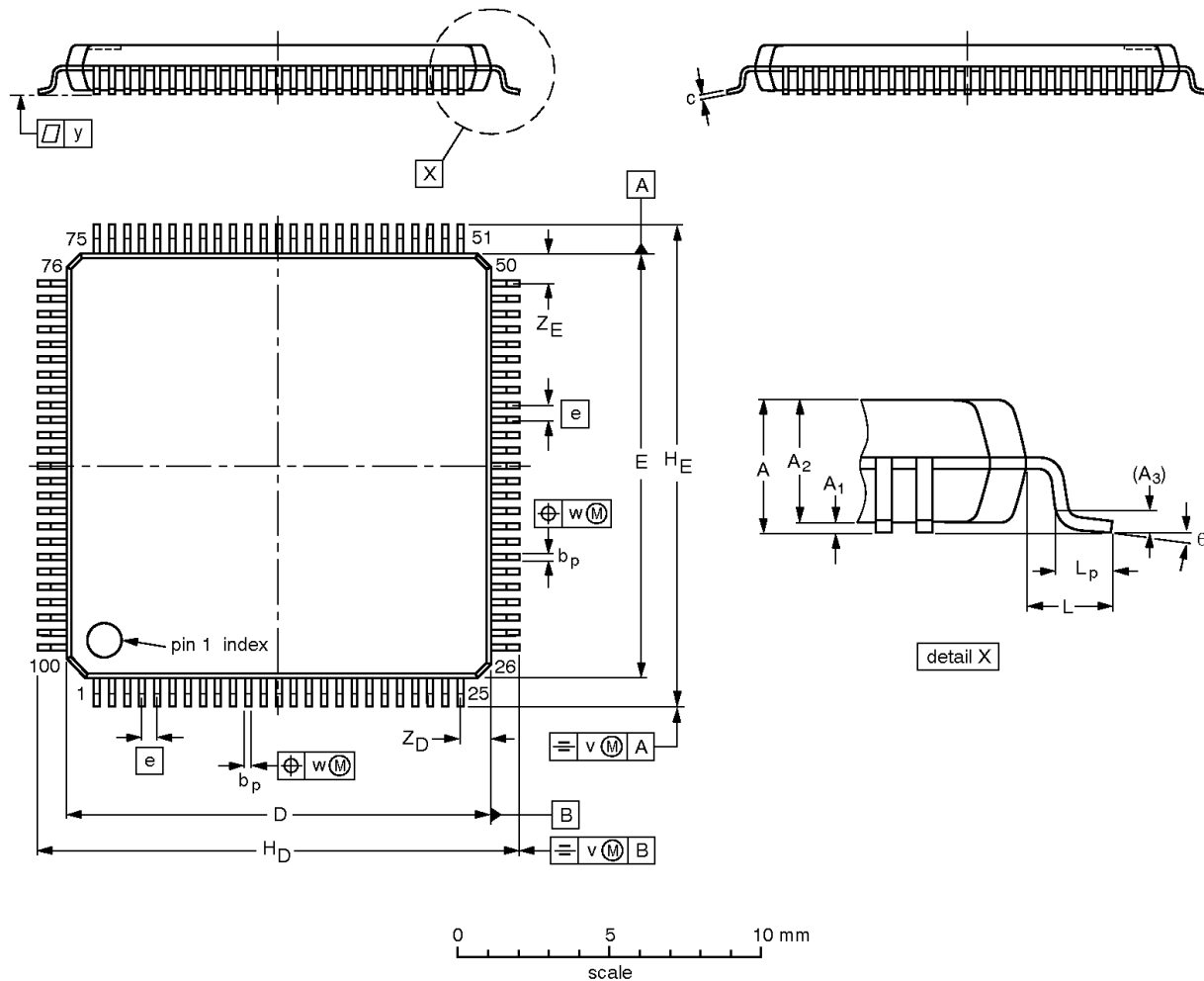
Figure 25. External WAIT Pin Timing

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LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm

SOT407-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _D | H _E | L | L _p | v | w | y | Z _D ⁽¹⁾ | Z _E ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-----|----------------|----------------|-----|----------------|-----|------|-----|-------------------------------|-------------------------------|----------|
| mm | 1.6 | 0.20 0.05 | 1.5 1.3 | 0.25 | 0.28 0.16 | 0.18 0.12 | 14.1 13.9 | 14.1 13.9 | 0.5 | 16.25 15.75 | 16.25 15.75 | 1.0 | 0.75 0.45 | 0.2 | 0.12 | 0.1 | 1.15 0.85 | 1.15 0.85 | 7° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT407-1 | | | | | | 95-12-19 97-08-04 |

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NOTES

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Data sheet status

| Data sheet status | Product status | Definition [1] |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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