ATSC 8-VSB Demodulator and Decoder TDA8960

1 FEATURES

General features

- One chip ATSC compliant 8-VSB demodulator and concatenated Trellis (Viterbi)/Reed-Solomon decoder with deinterleaver and de-randomizer
- 3.3V device
- 64 lead QFP64 package
- Boundary Scan Test
- Output format: 8-bit wide MPEG-2 transport stream

8-VSB demodulator

- On-chip digital circuitry for tuner AGC control
- Square-Root Raised-Cosine filter with 11.5% roll-off factor
- Fully internal carrier recovery loop with programmable loop filter
- Mostly internal clock recovery and AGC loops with programmable loop filters
- External indication of demodulator lock

Adaptive Equalizer

- Feed forward including a decision feedback structure (DFE)
- Range of -2.3 µs to +10.5 µs
- Adaptation based on ATSC field sync (trained) and/or 8-VSB data (blind)
- Capability to read and write taps via I²C-bus

Trellis (Viterbi) decoder

- Rate 2/3 (Rate 1/2 Ungerboeck code based)

Reed-Solomon decoder

- Internal convolutional de-interleaving
- External indication of uncorrectable error (Transport Error Indicator bit in MPEG packet header is also set)
- Followed by de-randomizer based on ATSC standard

I²C interface

- I²C-bus interface to initialize and monitor the demodulator and FEC decoder. An operation without I²C (default) is possible.

Applications

- Digital ATSC compliant TV receivers
- Personal computers with digital television capabilities
- Set top boxes

2 PINNING

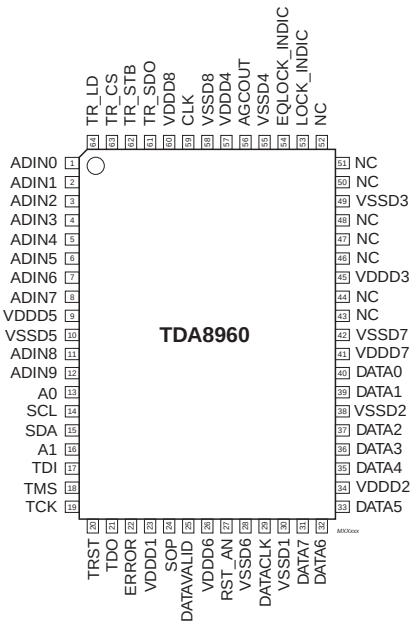

Fig.1 Pin configuration.

3 GENERAL DESCRIPTION

The TDA8960 is an ATSC compliant demodulator and forward error correction decoder for reception of 8-VSB modulated signals for terrestrial and cable applications:

Most of the loop components needed to recover the data from the received symbols are internal. The only required external loop components are a low-speed serial D/A converter and VCXO for the symbol timing recovery and an OPAMP integrator for the AGC. Loop parameters of the clock and carrier recovery can be controlled by I²C.

A tuner converts the incoming RF frequency to a fixed IF frequency centred at 44 MHz. The output of the tuner is filtered, followed by a down conversion in an IF block to a low IF centred at 1/2 the VSB symbol rate or approximately 5.38 MHz. The low IF signal is connected to the A/D converter.

The A/D converter is located within what is typically a fine AGC loop that includes a variable gain stage at the output of the IF block. However, it is also possible to apply the VSB IC AGC control output directly to the tuner. The detector for the VSB IC AGC output is located just after the A/D and determines the peak level of the incoming signals. After gain control, the low IF signal is sampled at a nominal rate of twice the VSB symbol frequency, or approximately 21.5 MHz.

The carrier recovery is performed completely internally. This function consists of a digital frequency and frequency and phase-locked loop (FPLL).

Data shaping is performed with a square root raised cosine (half Nyquist) filter with roll-off factor of 11.5%.

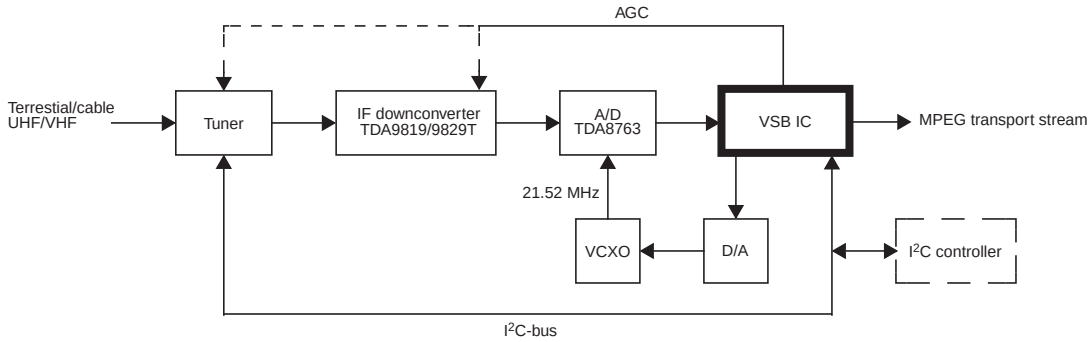

Fig.2 Front end unit for reception of 8-VSB signals.

Symbol timing recovery is performed mostly within the VSB IC, except that a low cost D/A converter and VCXO are required externally to generate the nominal 21.52 MHz clock for the A/D converter and VSB IC.

After carrier recovery, half Nyquist filtering, and symbol timing recovery, adaptive equalization is performed based on the use of the ATSC field sync (trained equalization) and/or the 8-VSB data itself (blind equalization). The adaptive equalizer uses a decision feedback equalizer (DFE) structure.

After trellis decoding, the stream is de-interleaved with a convolutional de-interleaver (interleaving depth 52). The memory for de-interleaving is on-chip. The Reed-Solomon decoder is ATSC-compliant, has a length 207 and can correct up to 10 bytes. Next the decoded stream is de-randomized using a pseudo-random binary sequence (PRBS).. Finally the data is passed to a FIFO that prevents the appearance of irregular gaps in the output data.

The output of the VSB IC is an ATSC compliant MPEG-2 transport stream together with a clock. Furthermore some signal flags are provided to indicate the sync bytes and the valid data bytes. Uncorrected blocks are also indicated.

The 8-bit wide MPEG-2 stream can be provided to an MPEG-2 transport stream demultiplexer.

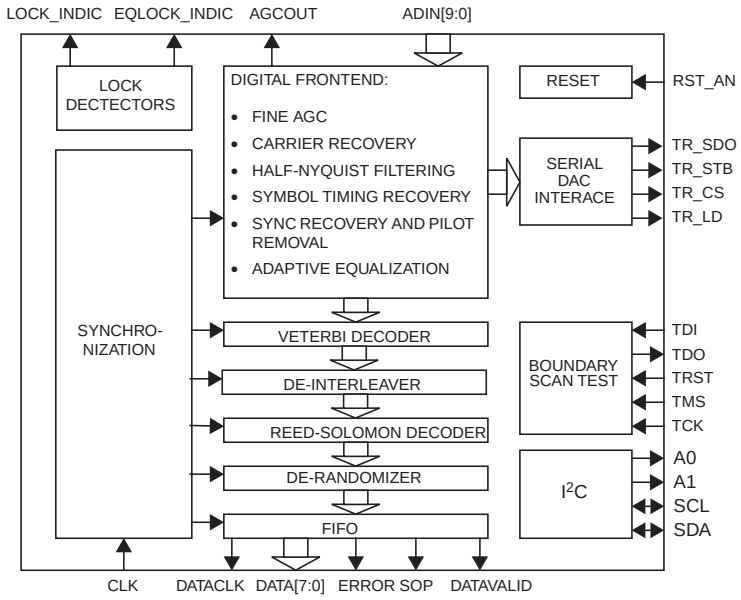

Fig.3 Block diagram of the TDA8960.

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