SiliconMAX™: Advances in On-State & Switching Performance for DC-DC Power Converters.

Chris Hill, Ed Huang, Stephen Oliver
Philips Semiconductors Ltd.
Hazel Grove, Stockport, SK7 5BJ, United Kingdom.
Tel.: +44 161 483 0011, Fax.:+44 161 957 5398

First presented on 22 June 1999 at PCIM Technical Conference, Nuernberg, Germany.

Abstract
The use of TrenchMOS structure allows much better utilisation of silicon area than conventional DMOS technology. This technology has now been extended to the voltage range 100-200V, and gives rise to significant benefits in both on-state and switching losses. By employing TrenchMOS technology and the use of maximum silicon chip sizes in popular power packages to give SiliconMAX devices, it is possible to offer the designer lower total "cost of ownership" in reduced component count, smaller board space and improved conversion efficiency.

Introduction:
Power regulation and control in Telecoms switching system is rapidly moving towards decentralized, on-board DC-DC power conversion. Distributed system architecture allows for unisolated Safety Extra Low Voltage (SELV) (24V/ 48V) bus distribution, increased system reliability due to power-per-shelf or power-per-board redundancy and easier system diagnostics & service.
DC-DC power converter modules contain one or more Power MOSFETs depending on the system topology.
SiliconMAX devices are primarily designed for Telecoms DC-DC converters due to their inherent physical structure and enhanced on-state and switching performance.

TrenchMOS structure: The effects of $R_{DS(on)}$ and Q_{GD} on 'On State' and 'Switching' efficiency
Power MOSFETs are most commonly made with what is conventionally called DMOS technology. In these structures thousands of tiny "cellular" MOSFETs operate in parallel to give the power handling capability of the full device. The on-resistance of these devices depends on the total conducting channel area. Since the channels are formed around the periphery of each "cell", the challenge for designers is to maximise the sum total of these peripheries. For the past 15 years advances in Power MOSFET performance have therefore been driven in the direction of making the cells ever-smaller and putting them closer together.

The move towards higher and higher cell packing density, however, eventually reaches a limit, not only for technological reasons but also because of a fundamental physics limitation known as the "Junction-FET" effect, where neighbouring cells packed too close together constrict the vertical current flow path down to the drain. To achieve further improvements in performance, a radical change in direction was necessary.

For a number of years development has continued on the refinement of a new MOSFET technology called "TrenchMOS". In these TrenchMOS devices a narrow trench is produced by ionic etching around each MOSFET cell, and the gate structure (including oxide and polysilicon) is formed inside these trenches (see figure on next page).

The fact that the gate structure is located at the bottom of the trench has the effect of alleviating the "Junction-FET" effect and allowing much closer packing of cells. In addition, the conducting channels are now formed on the vertical walls of the trenches, giving a more direct path for electrons flowing from source to drain, as shown in Fig. 1.

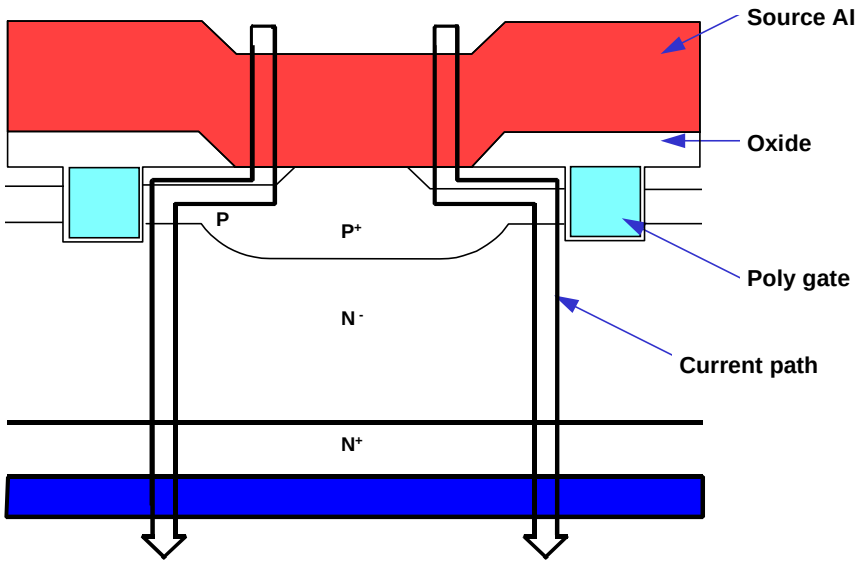

Fig. 1. TrenchMOS Cell Structure

The principle of TrenchMOS has been known for many years, but the full realisation of its advantages depended on the perfecting of the technology to make these devices in volume production with good control of the Trench structure, as well as optimal designs of the cell and Trench dimensions. This has now been achieved in volume production.

At the inception of the TrenchMOS concept it was generally assumed that the greatest advantages of this technology would be with low voltage devices, for example those with BVdss < 30V used in low voltage DC to DC converters. With these low voltage MOSFETs the largest contribution to the on-resistance comes from the channels themselves, so a new technology that gives a higher channel packing density and more direct current flow through these channels would naturally gives the biggest benefit to this voltage range. The early development work on TrenchMOS therefore concentrated on optimising structures to suit low voltage devices.

More recently, by a careful refinement of the Trench network, the edge termination structure and the choice of epi silicon doping and thickness, the TrenchMOS technology has been extended to higher voltage devices in the 100-200V range. Experimental results show that the advantage over conventional DMOS technology in this voltage range is significant.

SiliconMAX: 'on-state' benefits

SiliconMAX is the next step in applying TrenchMOS technology to the power conversion application. The capability of each power discrete package is enhanced by utilising the latest generation TrenchMOS technology in the 100V, 150V and 200V range and putting the maximum size silicon chip into each of these packages (hence "SiliconMAX"). One example of this is that it is now possible to have a 100V MOSFET in standard D-pak with an $R_{DS(on)}$ of 25 mΩ, equal to the benchmark

performance of a D²pak device using conventional DMOS technology. The much smaller size of the D-pak means a large saving in the board space while maintaining the same performance.
In applications such as low voltage, high power Full 'H' Bridge DC-DC converters, large package, large chip MOSFETs are often used in parallel to achieve the desired low on-state resistance required to handle the high current. With the progressive development of TrenchMOS into the 100/150/200V range, smaller, surface mount packages and/or component count reductions are possible.

SiliconMAX: switching benefits

Another advantage of TrenchMOS over conventional DMOS is in switching behaviour, which is of vital importance as power supply designers strive to achieve ever-higher frequency of operation. All Power MOSFETs dissipate energy when switching from a conducting to non-conducting state (and vice versa). This energy loss from the MOSFET takes the form of increased heat inside the application, thus leading to even lower efficiencies as wider design safety margins must be considered. The amount of energy dissipated during switching is directly related to the time taken to change state (parameters 't_{on}' and 't_{off}'). Switching time is dependent on the size of the capacitances within the Power MOSFET structure, in particular the component contributing to Q_{GD} (gate-drain charge). Figures 2 and 3 show schematically the built-in capacitor structures in TrenchMOS and DMOS devices giving rise to Q_{GD}.

This diagram shows the boundary between two adjacent DMOS cells.

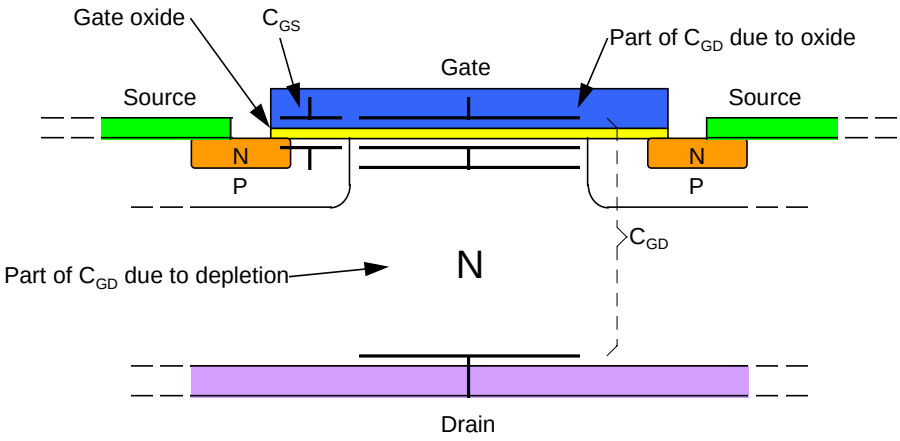

Fig. 2. Capacitances within a conventional DMOS structure

This diagram shows the boundary between two adjacent TrenchMOS cells.

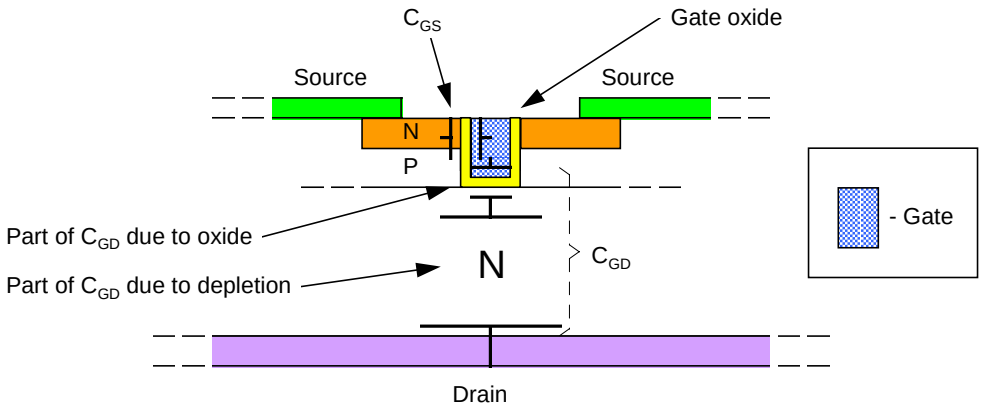

Fig. 3. Capacitances within a TrenchMOS structure

It can be seen that the gate-drain capacitor in a conventional DMOS is located in the area between neighbouring cells, and a simple way to reduce C_{GD} is therefore to bring the cells closer together. As explained earlier, however, there is a limit to how close we can pack the cells together because of the physical limitation of the “Junction-FET” effect, which can undesirably increase on-resistance. The above diagram also shows how in a TrenchMOS structure the gate-drain capacitor is formed within the narrow confines of the trenches. By a careful optimisation of the trench width and depth, as well as the doping of the silicon underneath, it is possible to minimise C_{GD} in a TrenchMOS structure.

In addition, because TrenchMOS allows much better utilisation of silicon in that it gives the same on-resistance with a smaller chip active area, the total capacitances and gate charges are also correspondingly reduced.

Laboratory switching measurements have been carried out on comparable TrenchMOS and DMOS devices in a typical forward converter circuit. A simplified drawing of the circuit is shown in Fig. 4a. The turn-on behaviour of the MOSFET is schematically shown in the waveforms sketched in Fig, 4b.

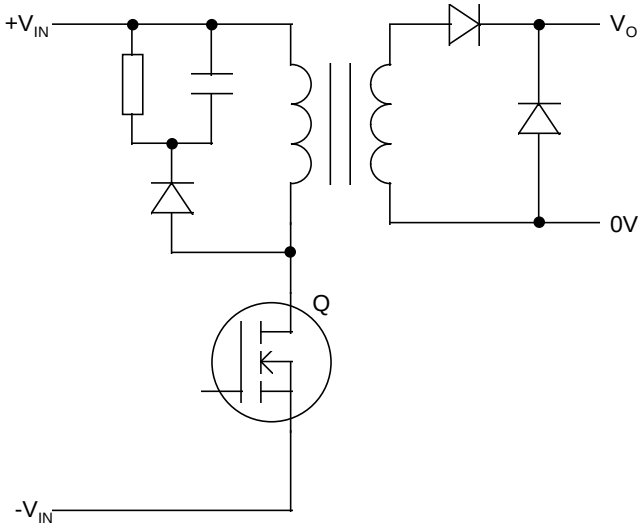

Fig. 4a. Simplified forward converter

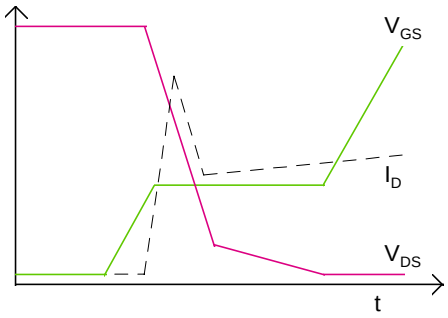

Fig. 4b. V_{DS}, V_{GS} and I_D waveforms associated with MOSFET "Q"

As the gate drive is applied, the device V_{GS} increases, but then reaches a plateau region during which the drain voltage on the device falls. The source of this plateau is the gate-drain capacitor effect mentioned earlier, which means that over this period the gate drive current is used to discharge C_{GD} to allow V_{DS} to fall. As can be seen from the waveforms, at the start of this plateau region the MOSFET is already conducting the full current, while the voltage is still in the process of falling to the low on-state value. This period therefore constitutes significant dissipation in the switching component and limits efficiency.

The results of the comparison we made between TrenchMOS and DMOS devices in the forward converter circuit are shown in the 'V_{DS} vs time' plots of Fig. 5a,. which were taken in the plateau period during turn-on.

The two devices have the same specification in terms of BVdss and $R_{DS(on)}$, both being 200V, 180mΩ types. As can be seen, the TrenchMOS device has a much faster Vds fall rate by virtue of its lower C_{GD}. The difference is even more striking when we compare the energy dissipation plot (integrating I and V) shown in Fig 5b., which demonstrates how TrenchMOS more than halves the switching losses.

Further trials were carried out on a range of 100V / TO220 devices of different Rds(on) values to determine an overall comparison between existing 100V DMOS technology and 100V TrenchMOS. The results are shown in Fig. 6. The dotted line in the plot indicates where two DMOS devices were tested in parallel to achieve the low 15mΩ $R_{DS(on)}$ value.

As can be seen, over the entire $R_{DS(on)}$ range, the TrenchMOS technology has half the Q_{GD} and therefore half the switching loss in the application for a given $R_{DS(on)}$.

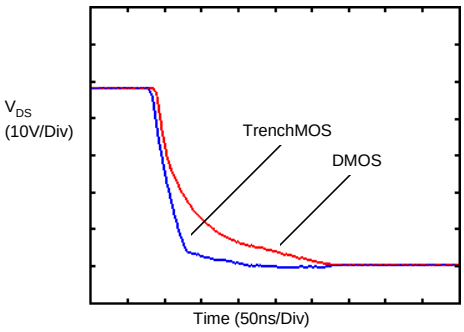

Fig. 5a. V_{DS} fall time for DMOS and TrenchMOS at turn-on

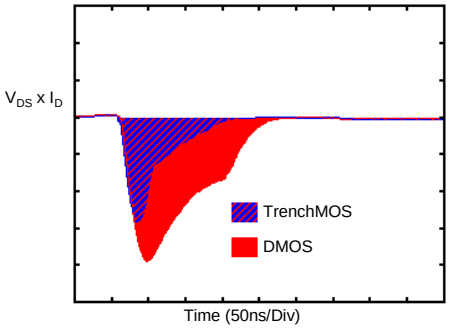

Fig. 5b. Energy dissipation in a DMOS and TrenchMOS MOSFET at turn-on

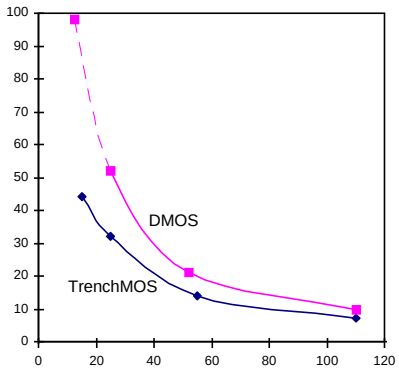

Fig. 6. Q_{GD} comparison: 100V DMOS and 100V TrenchMOS

SiliconMAX: Exploiting its benefits

The principal application for 100V, 150V and 200V SiliconMAX TrenchMOS devices is as primary side switches in Telecoms DC-DC converters having input voltages in the range 24V - 48VDC. The benefits in these applications include:

- Improved switching efficiency when replacing conventional DMOS devices with SiliconMAX devices of similar $R_{DS(on)}$.
- The ability to reduce package size for a given $_{RDS(on)}$ (e.g. replacing D²pak with Dpak) and hence reduce overall system size (and weight) and thus improve the converter's power per unit volume (W/mm^3) rating
- Reduce overall component count by substituting two or more paralleled conventional devices with one SiliconMAX device.
- The possibility of using 150V devices where previously 200V types were used, as most 48V converters only require the switching device to withstand 150V. The use of 150V devices would further enhance the $R_{DS(on)}$ and switching benefits described above.
- The option to provide surface mount solutions for $R_{DS(on)}$s previously available only in pin-through-hole packages (e.g. a change from a through-hole TO247 to a surface mount D^2pak).

These advantages allow smaller, more efficient converters, leading to higher density racking for the final application circuit boards (typically telecom Subscriber Line Interface Cards (SLICs)).

SUNSTAR 商斯达实业集团是集研发、生产、工程、销售、代理经销 、技术咨询、信息服务等为一体的高科技企业，是专业高科技电子产品生产厂家，是具有 10 多年历史的专业电子元器件供应商，是中国最早和最大的仓储式连锁规模经营大型综合电子零部件代理分销商之一,是一家专业代理和分銷世界各大品牌 IC 芯片和電子元器件的连锁经营綜合性国际公司，专业经营进口、国产名厂名牌电子元件，型号、种类齐全。在香港、北京、深圳、上海、西安、成都等全国主要电子市场设有直属分公司和产品展示展销窗口门市部专卖店及代理分销商,已在全国范围内建成强大统一的供货和代理分销网络。 我们专业代理经销、开发生产电子元器件、集成电路、传感器、微波光电元器件、工控机/DOC/DOM 电子盘、专用电路、单片机开发、MCU/DSP/ARM/FPGA 软件硬件、二极管、三极管、模块等，是您可靠的一站式现货配套供应商、方案提供商、部件功能模块开发配套商。商斯达实业公司拥有庞大的资料库，有数位毕业于著名高校——有中国电子工业摇篮之称的西安电子科技大学（西军电）并长期从事国防尖端科技研究的高级工程师为您精挑细选、量身订做各种高科技电子元器件，并解决各种技术问题。

微波光电部专业代理经销高频、微波、光纤、光电元器件、组件、部件、模块、整机；电磁兼容元器件、材料、设备；微波 CAD、EDA 软件、开发测试仿真工具；微波、光纤仪器仪表。欢迎国外高科技微波、光纤厂商将优秀产品介绍到中国、共同开拓市场。长期大量现货专业批发高频、微波、卫星、光纤、电视、CATV 器件： 晶振、VCO、连接器、PIN 开关、变容二极管、开关二极管、低噪晶体管、功率电阻及电容、放大器、功率管、MMIC、混频器、耦合器、功分器、振荡器、合成器、衰减器、滤波器、隔离器、环行器、移相器、调制解调器；光电子元器件和组件：红外发射管、红外接收管、光电开关、光敏管、发光二极管和发光二极管组件、半导体激光二极管和激光器组件、光电探测器和光接收组件、光发射接收模块、光纤激光器和光放大器、光调制器、光开关、DWDM 用光发射和接收器件、用户接入系统光光收发器件与模块、光纤连接器、光纤跳线/尾纤、光衰减器、光纤适 配器、光隔离器、光耦合器、光环行器、光复用器/转换器；无线收发芯片和模组、蓝牙芯片和模组。

更多产品请看本公司产品专用销售网站:

商斯达中国传感器科技信息网：http://www.sensor-ic.com/

商斯达工控安防网：http://www.pc-ps.net/

商斯达电子元器件网：http://www.sunstare.com/

商斯达微波光电产品网:HTTP://www.rfoe.net/

商斯达消费电子产品网://www.icasic.com/

商斯达实业科技产品网://www.sunstars.cn/ 微波元器件销售热线：

地址：深圳市福田区福华路福庆街鸿图大厦 1602 室

电话：0755-82884100 83397033 83396822 83398585

传真：0755-83376182 （0）13823648918 MSN: SUNS8888@hotmail.com

邮编：518033 E-mail:szss20@163.com QQ: 195847376

深圳赛格展销部：深圳华强北路赛格电子市场 2583 号 电话：0755-83665529 25059422

技术支持: 0755-83394033 13501568376

欢迎索取免费详细资料、设计指南和光盘 ；产品凡多，未能尽录，欢迎来电查询。

北京分公司：北京海淀区知春路 132 号中发电子大厦 3097 号

TEL：010-81159046 82615020 13501189838 FAX：010-62543996

上海分公司：上海市北京东路 668 号上海赛格电子市场 D125 号

TEL：021-28311762 56703037 13701955389 FAX：021-56703037

西安分公司：西安高新开发区 20 所(中国电子科技集团导航技术研究所)

西安劳动南路 88 号电子商城二楼 D23 号

TEL：029-81022619 13072977981 FAX:029-88789382