NEW PRODUCTS

Philips Semiconductors are working intensively on bringing new products to the market to meet the requirements of existing and new developing applications areas. These are the new products and technologies that appear for the first time in this data handbook.

HIGH COMMUTATION TRIACS

Philips range of high commutation triacs now include two new devices rated at 8 A and 25 A. These devices have high off-state dV/dt and commutation capability, and are ideal for use in motor control circuits and other inductive switching applications. (Types: BTA208, BTA225).

ISOLATED THYRISTORS AND TRIACS

The Industry Standard - BT151 thyristor plus a wide range of standard and high-commutation triacs are now available in the SOT186A isolated package, featuring isolation voltage up to 2500 Vrms. The SOT186A package allows two or more power devices to share a common heatsink, without the need for insulating bushes and spacers, or alternatively allows the heatsink to be grounded. (Types: BT151X, BT136X, BT137X, BT138X, BT139X, BTA208X, BTA212X, BTA216X).

SURFACE MOUNTING BT169

The popular BT169D, sensitive gate thyristor, used in a wide variety of consumer applications is now available in a SOT223 envelope, suitable for surface mounting (Type: BT169DW).

NEW 5 A RATED THYRISTOR

The BT300 series is a range of 5 A rated thyristors with similar characteristics to the BT151, available in 500 V, 600 V and 800 V grades. It is intended for lower power applications where the 7.5 A rating of the BT151 is not required (Types: BT300-500R, BT300-600R, BT300-800R).

NEW 5 A RATED, LOGIC LEVEL THYRISTOR

The BT258 series is a range of 5 A rated, sensitive gate thyristors available in 500 V, 600 V and 800 V grades. The BT258 may be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits. This device is particularly suitable for microprocessor controlled domestic appliances and low power consumer products. (Types: BT258-500R, BT258-600R, BT258-800R)

ADDITIONAL VOLTAGE GRADES FOR BT150

Up to now, the BT150 has only been available in the 500 V grade. Additional voltage grades of 600 V and 800 V are now available. (Types: BT150-600R, BT150-800R)

UNENCAPSULATED, PASSIVATED, SILICON POWER CHIPS

All the devices in this data handbook are available as unencapsulated dice complete with passivation and metallised contact pads, but without bond wires or any other connections or encapsulation. Contact your Regional or National Sales Office for details.

APPLICATIONS

For further information on applications which use thyristors and triacs, refer to the new handbook "Triacs and thyristors - an application guide" (Order code: 9397-750-00372).

For further information on other power semiconductor applications, refer to the "Power Semiconductor Applications Handbook" (Order code:9398-652-85011).

PHILIPS THYRISTORS AND TRIACS

The Phase 2 Process

The basic principle of using a PNPN structure to produce a thyristor, and a NPNPN structure (with two PNPN's in antiparallel) to produce a triac has been known for decades. The factors controlling various important parameters, such as blocking voltages, on-state voltage drop, trigger current, latching and holding current, off-state dV/dt, triac commutation and surge capability are also well known.

The modern challenge of making good thyristors and triacs lies not so much in innovative design concepts as in perfection of manufacturing technology.

Philips products are characterised by the use of well established, stable processes in both diffusion and assembly, giving devices of high quality and reliability. The strengths and special features of these products are outlined below.

Except for those designed for specialist applications such as GTO's and ASCR's, most common thyristors and triacs are specified to have voltage blocking capability in both directions. This means that in the PNPN or NPNPN structures, two opposing PN junctions need to be designed to withstand the rated voltage.

This is normally achieved by starting with a suitably low doped N type silicon wafer into which two P regions are diffused simultaneously from opposite sides, resulting in a symmetric PNP structure where both PN junctions have high voltage blocking capability. Further N-type diffusions are then put into both sides of the structure, (for a triac). The result is a NPNPN structure with a symmetrical blocking voltage. Both of these blocking PN junctions now need to be passivated at the point where they intersect the silicon surface, and there are two common methods for doing this, shown in the diagrams below.

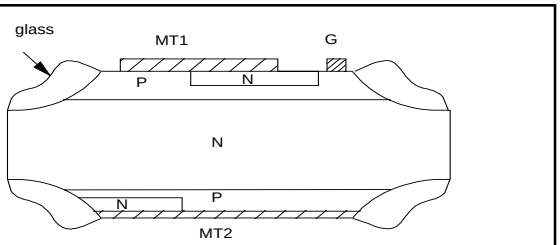

Fig.1. Phase 1 structure and Passivation.

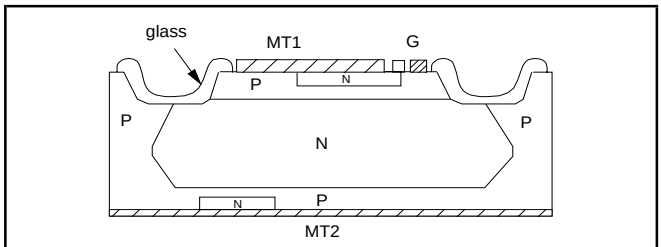

Fig.2. Phase 2 structure and Passivation.

In Philips terminology we call these "Phase 1" and "Phase 2" technologies respectively.

As can be seen, Phase 1 passivation requires a simultaneous etching of mesa troughs from both sides followed by the deposition of passivants such as negatively charged glass. The advantages of this technique are small chip size and fewer processing stages. No aluminium isolation diffusion or photolith are required, hence the overall chip cost is lower.

By contrast, the Phase 2 technology requires an aluminium isolation diffusion prior to the fabrication of the PNPN or NPNPN structure, which has the effect of bringing both blocking PN junctions to the top surface. These can then be passivated with trough etching and glass deposition on the top side only.

The main advantage of the Phase 2 technology is a much more mechanically robust structure, due to the fact that the edge of the chip is not reduced in thickness. Minor damage to the edges does not intrude into the active region. A further advantage is that the flat bottom surface is compatible with automatic die bonding in assembly.

The main disadvantage is increased cost in comparison with the Phase 1 process.

Philips has progressed from Phase 1 to Phase 2 passivation technology, despite its higher cost, because of the advantages of mechanical ruggedness and lower vulnerability to handling damage.

It is our belief that Philips thyristors and triacs produced using Phase 2 technology have fewer manufacturing defects, and are more reliable than devices produced by competitors who are still using the Phase 1 structure.

Passivation

The use of the Phase 2 passivation structure coupled with the well developed glass mesa passivation technology at Philips results in devices with high voltage blocking capability and extremely stable characteristics. The structure is also less vulnerable to edge damage compared to the alternative Phase 1 passivation.

The typical off-state breakdown voltage of our thyristors and triacs is in excess of 1000V, with a very tight distribution, so much so that we normally consider any devices with blocking voltages less than 500V to be defective. For example, our 200V and 400V grade devices are tested to withstand 500V.

In contrast, competitors using Phase 1 passivation who deliver true 200V and 400V devices, i.e. devices whose breakdown voltages are just above 200V or 400V, are likely to suffer from glass cracks or chipped corners which can progress to the extent that they cause quality and reliability problems.

Assembly

The absence of troughs and glass on the bottom surface of our chips allows us to use automated assembly. We use die bonding technology which involves scrubbing the chips onto heated leadframes that are precoated with solder. This technique gives an excellent, void free contact with low thermal resistance and avoids having to subject the chips to long duration, high temperature furnacing. Compared to our main competitors, our devices have superior die bonds and lower thermal resistance, which means that they operate at a lower junction temperature for the same dissipation, and thus have higher reliability.

Another feature of this assembly method is that, along with the ultrasonic wire bonding used to connect to the top of the chip, it gives our devices a high thermal fatigue capability. Thus they have excellent on-state reliability as well as extremely stable off-state characteristics.

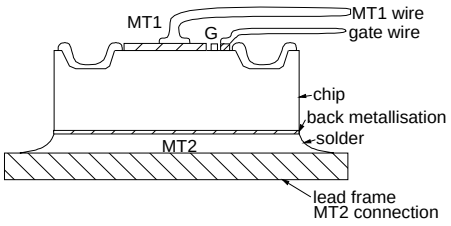

Fig.3. Die bonding onto leadframes, wire bonding.

Unencapsulated Dice

Because of the advantages of the Philips process and assembly techniques outlined above, our family of triacs and thyristors are ideal for use in unencapsulated form, in applications where space and height are at a premium. The glass passivation protects the, otherwise exposed surface regions giving highly stable device characteristics. The silicon wafers are 100% electrically tested and are normally supplied sawn, on blue film frame carriers. Unsawn wafers can be supplied where necessary.

Philips Semiconductors have a wealth of experience of supplying devices in this form and are able to provide expert advice on the subject of mounting, soldering and attaching bond wires to unpackaged dice.

Thyristor and Triac Ratings

A rating is a value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

All limiting values quoted in this data handbook are Absolute Maximum Ratings - limiting values of operating and environmental conditions applicable to any device of a specified type, as defined by its published data.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value is exceeded with any device, under the worst probable operating conditions.

VOLTAGE RATINGS

V_{DRM}, V_{RRM} Repetitive peak off-state voltage. The maximum allowable instantaneous forward or reverse voltage including transients. The rated values of $V_{DRM(max)}$ and $V_{RRM(max)}$ may be applied continuously over the entire operating junction temperature range, provided that the thermal resistance between junction and ambient is kept low enough to avoid the possibility of thermal runaway.

CURRENT RATINGS

$I_{T(AV)}$ Average on-state current. The average rated current is that value which under steady state conditions will result in the rated temperature T_{jmax} being reached when the mounting base or heatsink is at a given temperature. Graphs of on-state dissipation versus $I_{T(AV)}$ or $I_{T(RMS)}$ are provided in the data sheets. The right hand scale of each graph shows the maximum allowable mounting base or heatsink temperature for a given dissipation.

$I_{T(RMS)}$ RMS on-state current. For a given average current, the power dissipated at small conduction angles is much higher than at large conduction angles. This is a result of the higher rms currents at small conduction angles. Operating the device at rms currents above the rated value is likely to result in rapid thermal cycling of the chip and the bond wires which can lead to reliability problems.

I_{TSM} Non-repetitive peak on-state current. The maximum allowable peak, on-state surge current which may be applied no more than 100 times in the life of the device. The data sheet condition assumes a starting junction temperature equal to T_{jmax}, and a sinusoidal surge current at a mains frequency of 50/ 60 Hz. For a triac, a full sine wave of current is applied.

Immediately after the surge, the mains voltage is reapplied with a peak value equal to the full rated off-state voltage, V_{DRM}. Graphs in the data sheet show the variation of I_{TSM} with surge duration.

I^2t Device fuse rating. For correct circuit protection, the I^2t of a protective fuse must be less than the I^2t of the device. In the data sheets, the device rating is numerically equal to $I_{TSM}{}^2/200$ and assumes a 10ms fusing time.

dI_T/dt The maximum allowable rate of rise of on-state current after gate triggering. The theory underlying this rating is that, where the rate of rise of main current is very rapid immediately after triggering, local 'hot spot' heating will occur in a small part of the device active area close to the gate, leading to device degradation or complete failure. In practise, true dI_T/dt failures of this kind are very rare. The only conditions where dI_T/dt has been observed to cause failures is in triacs operated in the T2-, G+ quadrant where a combination of high dI_T/dt and high peak current (in excess of the data sheet ratings), can cause damage to the gate structure. For this reason, operation of our triacs in the T2-, G+ quadrant should be avoided wherever possible.

dI_T/dt V_{BO} or dV_D/dt triggered. Where a device is triggered by exceeding the breakdown voltage, or by a high rate of rise of off-state voltage, as opposed to injecting current into the gate, it is necessary to limit the dI_T/dt. A note in the data sheet specifies the maximum allowable dI_T/dt for this mode of triggering.

THERMAL RATINGS

$R_{th\ j\text{-}mb}$ $R_{th\ j\text{-}hs}$ $R_{th\ j\text{-}sp}$ $R_{th\ j\text{-}lead}$ Steady state thermal resistances. Junction to mounting base is used for TO220AB envelope. Junction to heatsink for devices in full pack, isolated envelopes, SOT186 and SOT186A. Junction to solder point is used for devices in SOT223 surface mounting envelope. Junction to lead is used for devices in SOT54 (TO92) small signal outline. The maximum value of the thermal resistance is given in the data sheet, and is used to specify the device rating. The average junction temperature rise for a given dissipation is given by multiplying the average dissipation by the thermal resistance.

Note that for triacs, two values of thermal resistance are quoted; one for half cycle operation and one for full cycle operation. This is because only half of the chip carries current in each half cycle allowing the non-conducting half to cool down between conduction periods. The net effect is to reduce the average thermal resistance for full cycle conduction.

$R_{th\ j\text{-}a}$ Typical values of junction to ambient thermal resistance are given in the data sheet assuming that the device is mounted vertically on a printed circuit board, in free air.

$Z_{th\ j\text{-}mb}$, $Z_{th\ j\text{-}hs}$ Whilst the average junction temperature rise may be found from the thermal resistance figure, the peak junction temperature requires knowledge of the current waveform and the transient thermal impedance. The thermal impedance curves in the data sheets are based on rectangular power pulses. The junction temperature rise due to a rectangular power pulse, is given by multiplying the peak dissipation during the pulse by the thermal impedance $Z_{th\ j\text{-}mb}$ for the given pulse width. Analysis methods for non-rectangular pulses are covered in the Power Semiconductor Applications handbook.

T_{jmax} The maximum operating junction temperature range for all our thyristors and triacs is 125˚C. This applies in either the on-state or off-state, and for either half cycle or full cycle conduction. It is permissible for the junction temperature to exceed $T_{j\ max}$ for short periods during non-repetitive surges, but for repetitive operation the peak junction temperature must remain below $T_{j\ max}$.

T_{stg} The limiting storage temperature range for all our thyristors and triacs is -40˚C to 150˚C.

$P_{G(AV)}$, P_{GM}, I_{GM}, V_{GM} The average and peak gate power dissipation, and the maximum gate voltage and gate current. Exceeding the gate ratings can cause the device to degrade gradually, or fail completely.

Thyristor and Triac Characteristics

A characteristic is an inherent and measurable property of a device. Such a property may be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

STATIC CHARACTERISTICS

V_T On-state voltage. The tabulated value in the data sheet is the maximum, instantaneous on-state voltage measured under pulse conditions to avoid excessive dissipation, at a junction temperature of 25˚C. The data sheet also contains a graph showing the maximum and typical characteristics at 125˚C and the maximum characteristic at 25˚C. The maximum characteristic at 125˚C is used to calculate the dissipation for a given average or rms current, and hence the graph of on-state dissipation versus average or rms current in the data sheet.

The on-state voltage/ current characteristic of a diode, thyristor or triac may be approximated by a piecewise linear model as shown in the figure below; where R_S is the slope of the tangent to the curve at the rated current, and V_O is the voltage axis intercept. The on-state voltage is then $V_T = V_O + I_T.R_S$, and the instantaneous dissipation is $P_T = V_O.I_T + I_T^2.R_S$. where I_T is the instantaneous on-state current.

It can be shown that the average on-state dissipation for any current waveform is: $P_{T(AV)} = V_O.I_{T(AV)} + I_{T(RMS)}^2.R_S$, where $I_{T(AV)}$ is the average on-state current and $I_{T(RMS)}$ is the rms value of the on-state current. Graphs in the published data show on-state dissipation as a function of average current for thyristors and versus rms current for triacs. Sinusoidal current waveforms are assumed and the graphs show dissipation over a range of conduction angles

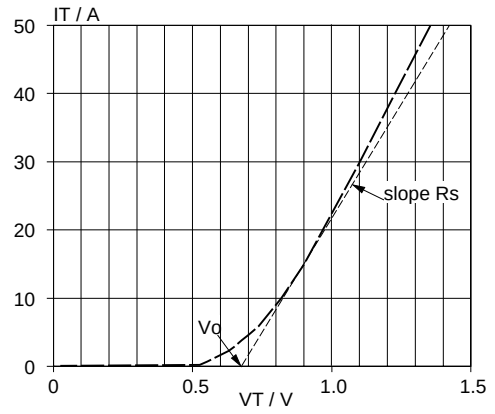

Fig.4. Piecewise linear approximation to thyristor and triac on-state characteristic.

I_{GT} Gate trigger current. The data sheet shows the typical and maximum gate trigger current at a junction temperature of 25˚C. A graph in the data sheet shows the variation of normalised I_{GT} with temperature.

When designing a triac gate trigger circuit, triggering in the T2-, G+ quadrant should be avoided if possible. The gate trigger current in this quadrant is much higher than in the other three quadrants and the device is more susceptible to turn-on dI_T/dt failure.

V_{GT} Gate trigger voltage. The data sheet shows the typical and maximum gate trigger voltage at a gate current equal to I_{GT}, at a junction temperature of 25˚C. A graph in the data sheet shows the variation of normalised V_{GT} with temperature.

To ensure that a device will not trigger, the gate voltage must be held below the minimum gate trigger voltage. The data sheet quotes $V_{GT(min)}$ at the maximum junction temperature (125˚C), and the maximum off-state voltage ($V_{DRM(max)}$).

I_L Latching current. The latching current is the value of on-state current required to maintain conduction at the instant when the gate current is removed. A graph in the data sheets shows the variation of normalised I_L with temperature.

To trigger a thyristor or triac, a gate current greater than the maximum device gate trigger current I_{GT} must be applied until the on-state current I_T rises above the maximum latching current I_L. This condition must be met at the lowest junction temperature.

I_H Holding current. The holding current is the value of on-state current required to maintain conduction once the device has fully turned on and the gate current has been removed. The on-state current must have previously exceeded the latching current I_L. A graph in the data sheet shows the variation of normalised I_H with temperature.

To turn off (commutate) a thyristor or triac, the load current must remain below I_H for sufficient time to allow a return to the off-state. This condition must be met at the highest operating junction temperature (125˚C).

I_D, I_R The maximum off-state leakage current, specified at rated $V_{DRM(max)}$, $V_{RRM(max)}$ at 125˚C.

DYNAMIC CHARACTERISTICS

dV_D/dt Critical rate of rise of off-state voltage. Displacement current caused by a high rate of rise of off-state voltage can induce a gate current sufficient to trigger the device. Devices with sensitive gates are particularly susceptible to dV_D/dt triggering, and since gate trigger current decreases as junction temperature increases, the condition is worse when the device is hot. The data sheet figure is specified at 125˚C using an exponential waveform and a maximum applied voltage of 67% $V_{DRM(max)}$. The dV_D/dt is measured to 63% of the maximum voltage.

To prevent sensitive gate devices from false triggering due to high rates of rise of off state voltage, 1 kΩ resistor in parallel with a 10nF capacitor may be fitted between gate and cathode (gate and terminal 1 for a triac). This approach is less effective for standard gate devices. In this case, the preferred option is to fit an RC snubber between anode and cathode (T2 and T1 for a triac) to reduce the dV_D/dt below the critical value.

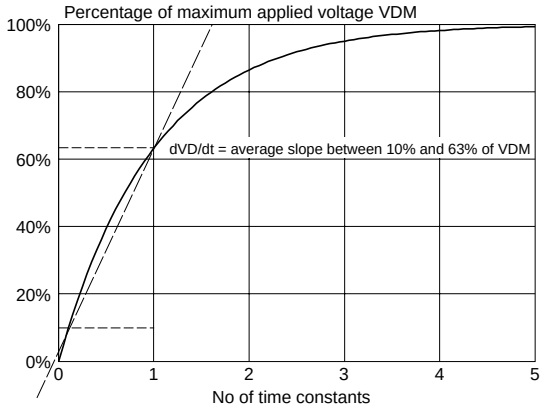

Fig.5. Exponential waveform used for measurement of critical off-state dV_D/dt. The dV_D/dt is the average slope between 10% and 63% of the maximum applied voltage V_{DM}.

t_{gt} Gate controlled turn-on time. A typical turn on time of 2 μs is specified for all our thyristors and triacs.

t_q Circuit commutated turn-off time. A typical turn off time of 70 μs is specified for standard gate thyristors and 100μs for sensitive gate thyristors.

TRIAC COMMUTATION

A triac is an AC conduction device and may be thought of as two thyristors in antiparallel, monolithically integrated onto the same silicon chip. In phase control circuits, the triac often has to be triggered into conduction part way into each half cycle. This means that at the end of each half cycle the on-state current in one direction must drop to zero and not resume in the other direction until the device is triggered again. This commutation turn-off capability is at the heart of triac power control applications. If the triac were truly two separate thyristors in antiparallel, this requirement would not present any problems. However, as the two are on the same piece of silicon there is the possibility that the unrecombined charge of one thyristor as it turns off may act as gate current to trigger the other thyristor as the voltage rises in the opposite direction. This phenomenon is called commutation failure.

There are two components of current which can act as gate current to cause commutation failure. One of these is the displacement current generated by the reapplied dV_{com}/dt. The other is the recombination current, which is mainly determined by the rate of fall of commutating current, dI_{com}/dt. Both tend to create a lateral volt drop in the emitter of the opposing thyristor which triggers the device in the opposite direction to the original current flow.

At low rates of fall of current, dI_{com}/dt, the ammount of unrecombined charge is small and commutation failure occurs mainly because of the rate of rise of off-state voltage, dV_{com}/dt. This situation is worst for inductive loads where the rate of rise of voltage can be very high when commutation occurs. The conventional remedy for this type of commutation failure is to fit a snubber across the device to limit the rate of rise of off-state voltage dV_{com}/dt.

At high values of dI_{com}/dt, the recombination current dominates and, above a critical value of dI_{com}/dt, the device will not commutate even at fairly low values of dV_{com}/dt. Under these conditions, a snubber will not prevent commutation failure, and the best option is to use a High Commutation Triac.

HIGH COMMUTATION TRIACS

Philips High Commutation Triacs attempt to separate the two antiparallel thyristor structures to prevent the unrecombined charge from the conducting half becoming gate current in the other half. This is accomplished by lateral separation of the top and bottom emitters, more extensive emitter and peripheral shorting, and by a modified gate design which prevents triggering in the T2-, G+ quadrant.

The device design, in addition to giving high immunity to commutation failure, also improves the off-state dV_D/dt capability. They will commutate the full rated current up to 125˚C without the aid of a snubber and will also withstand extremely high rates of rise of off-state voltage, in excess of 1000 V/μs. High commutation triacs can simplify circuit design by eliminating the need for RC snubbers. Typical applications include; motor starting, where the triac may be required to commutate the starting current; the switching of d.c. operated relay coils where the time constant of the coil is much greater than the mains period and static switching where it is required to turn the triac off whilst it is carrying an overload current.

dV_{com}/dt Critical rate of rise of commutating voltage. For conventional, as opposed to high commutation triacs, the data sheet conditions specify a junction temperature of 95˚C and a dI_{com}/dt given by $2.\sqrt{2}.\pi.f.I_{T(RMS)}$, where f is the mains frequency (assumed to be 50Hz). This value is the maximum rate of change of current which occurs at the zero crossing for a sine wave current equal to the rated rms value, $I_{T(RMS)}$. Graphs in the data sheet show the variation of dV_{com}/dt and with junction temperature with dI_{com}/dt as a parameter.

dI_{com}/dt Critical rate of change of commutating current. High Commutation Triacs are intended for use in circuits where high values of both dI_{com}/dt and dV_{com}/dt can occur. Commutation capability is specified in terms of dI_{com}/dt, without a snubber and at the highest junction temperature, T_{jmax} = 125˚C. A graph in the data sheet shows the variation of dI_{com}/dt with junction temperature.

Operation up to 150˚C

The maximum operating junction temperature, T_{jmax} of Philips thyristors and triacs is 125˚C. Operation above T_{jmax} for long periods, particularly in the off-state, can give rise to reliability problems due to changes in characteristics which occur as a result of mobile charge in the glass passivation.

Furthermore, as a thyristor or triac gets hot, it becomes more susceptible to false gate triggering, off-state dV_D/dt triggering, thermal runaway and commutation failure.

However, it has become apparent that some customers have applications which require operation of thyristors and triacs at higher junction temperatures.

Recent improvements in Philips glass mesa technology backed up by extensive reliability testing has shown that, for certain applications, our thyristors and triacs can be operated reliably at junction temperatures up to 150˚C.

Typical applications where 150˚C operation may be allowed include:- static switching of resistive loads, power switches for domestic appliances and electric heating applications where the device is mounted on a high temperature substrate.

Extending the upper operating junction temperature to 150˚C depends very much on the application. For this reason we recommend that customers wishing to use our thyristors and triacs at 150˚C contact the Field Applications Engineer at their Regional or National sales office.

QUALITY

Total Quality Management

Philips Semiconductors is committed to be a world class, customer driven, volume supplier of semiconductors.

To achieve this, we operate a Total Quality Management (TQM) system, based on Continuous Improvement and Quality Assurance in all our business activities, and Partnerships with our customers and suppliers.

The top priority throughout the company is Continuous Improvement.

To focus on this we will:

- Work closely with key customers, as our partners.
- Monitor progress, using customer-driven data, of our product and services.
- Benchmark against the best.

Furthermore, all parts of the organisation must always demonstrate:

- The presence of a strong, management-led improvement structure.
- Commitment and participation in all areas.
- Measurable progress towards our Quality Improvement goals.

Organisation

An organisation is in place which ensures that personnel with the necessary organisational freedom and authority can identify and solve quality problems, prevent occurrence of product non-conformity and protect the customer from non-conforming product.

Design control

A comprehensive design and development procedure is in place which ensures that the requirements of good design practice are met.

Particular emphasis is placed on ensuring that the initial specification is agreed by the Customer and the Marketing and Development functions.

There are regular formal reviews of design progress to ensure that the initial specification will be met by the design.

Detailed measurements are made on initial samples to ensure that the initial specification has been met.

Process control

All processes which directly affect quality are carried out under controlled conditions. Documented work instructions are available for all production processes and the appropriate environmental controls are in place to ensure consistent processing. Monitoring of the product, processes and the environment takes place during production.

Approval exercises are run to ensure that new processes and new equipment perform at an acceptable level.

Written, photographic or visual standards are available at the appropriate points in the production processes.

Corrective action

Non-conforming product found in process is investigated and the root causes identified. Changes to product or process are then introduced to prevent recurrence of the problem.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE. Our factories are certified to ISO 9000.

Partnerships with customers

These include: PPM co-operations, design-in agreements, ship-to-stock, just-in-time, self-qualification programmes and application support.

Partnerships with suppliers

In addition to ISO9000 audits and close monitoring of supplier delivery performance, we operate a Supplier Excellence Award scheme which requires suppliers and their sub-suppliers to use statistical process control, perform gauge studies and use failure mode and effect analysis (FMEA) techniques to identify and correct the root causes of quality and delivery problems.

Product reliability

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimizations for the highest built-in product reliability. Highly accelerated tests are applied in order to evaluate the product reliability. Rejects from reliability tests and from customer complaints are submitted to failure analysis and the results applied to improve the product or process.

Customer responses

Our quality improvement depends on joint action with our customer. We need our customers inputs and we invite constructive comment on all aspects of our performance. Please contact your local sales representative.

Recognition

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organisations.

SUNSTAR 商斯达实业集团是集研发、生产、工程、销售、代理经销 、技术咨询、信息服务等为一体的高科技企业，是专业高科技电子产品生产厂家，是具有 10 多年历史的专业电子元器件供应商，是中国最早和最大的仓储式连锁规模经营大型综合电子零部件代理分销商之一,是一家专业代理和分銷世界各大品牌 IC 芯片和電子元器件的连锁经营綜合性国际公司，专业经营进口、国产名厂名牌电子元件，型号、种类齐全。在香港、北京、深圳、上海、西安、成都等全国主要电子市场设有直属分公司和产品展示展销窗口门市部专卖店及代理分销商,已在全国范围内建成强大统一的供货和代理分销网络。 我们专业代理经销、开发生产电子元器件、集成电路、传感器、微波光电元器件、工控机/DOC/DOM 电子盘、专用电路、单片机开发、MCU/DSP/ARM/FPGA 软件硬件、二极管、三极管、模块等，是您可靠的一站式现货配套供应商、方案提供商、部件功能模块开发配套商。商斯达实业公司拥有庞大的资料库，有数位毕业于著名高校——有中国电子工业摇篮之称的西安电子科技大学（西军电）并长期从事国防尖端科技研究的高级工程师为您精挑细选、量身订做各种高科技电子元器件，并解决各种技术问题。

微波光电部专业代理经销高频、微波、光纤、光电元器件、组件、部件、模块、整机；电磁兼容元器件、材料、设备；微波 CAD、EDA 软件、开发测试仿真工具；微波、光纤仪器仪表。欢迎国外高科技微波、光纤厂商将优秀产品介绍到中国、共同开拓市场。长期大量现货专业批发高频、微波、卫星、光纤、电视、CATV 器件： 晶振、VCO、连接器、PIN 开关、变容二极管、开关二极管、低噪晶体管、功率电阻及电容、放大器、功率管、MMIC、混频器、耦合器、功分器、振荡器、合成器、衰减器、滤波器、隔离器、环行器、移相器、调制解调器；光电子元器件和组件：红外发射管、红外接收管、光电开关、光敏管、发光二极管和发光二极管组件、半导体激光二极管和激光器组件、光电探测器和光接收组件、光发射接收模块、光纤激光器和光放大器、光调制器、光开关、DWDM 用光发射和接收器件、用户接入系统光光收发器件与模块、光纤连接器、光纤跳线/尾纤、光衰减器、光纤适 配器、光隔离器、光耦合器、光环行器、光复用器/转换器；无线收发芯片和模组、蓝牙芯片和模组。

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