1 TRANSMITTING TRANSISTOR DESIGN

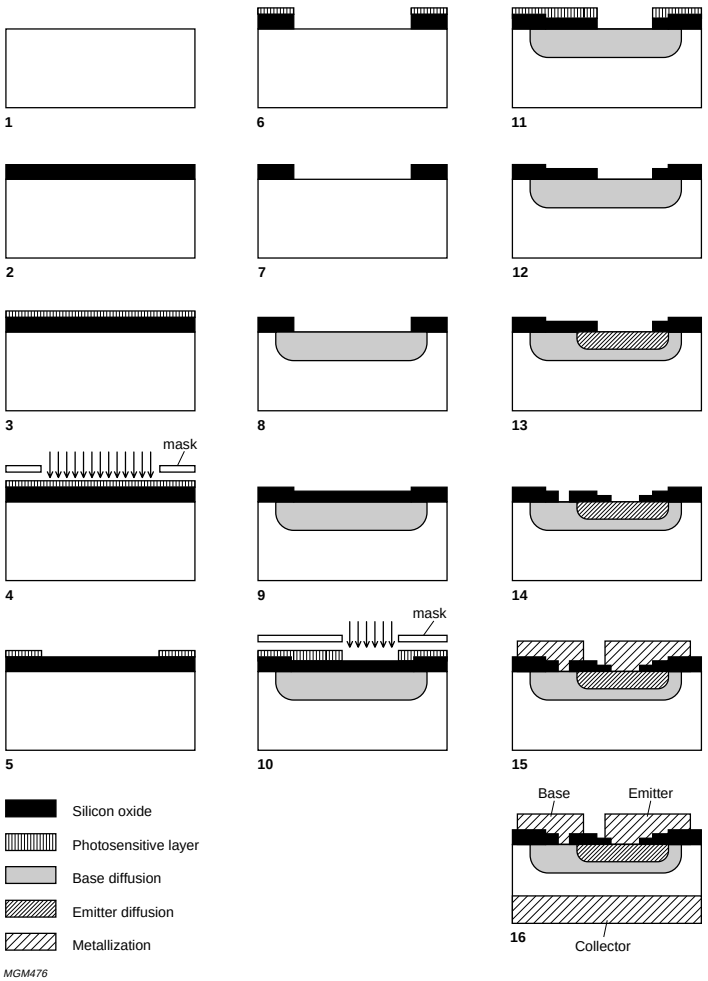
1.1 Die technology and design

A transmitting transistor has to deliver high power at high frequency (>1 MHz). This means that a large transistor die with a fine structure is required. Bipolar and MOS transistors are suitable, see panel, and Philips Semiconductors' portfolio includes both types. Their relative merits are summarized later in this section. First, however, let's look at the basic aspects of design that contribute to the reliability and high-performance of a modern RF transmitting transistor.

TRANSISTOR FABRICATION

As is well-known, most transistors are fabricated from silicon wafers (5" dia. or larger, and about 0.25 mm thick) in a multi-stage batch process that involves precise, localized doping of an epitaxial layer grown on the silicon substrate to form the different transistor regions. The main process steps for fabricating bipolar transistors are shown here as a reminder. MOS transistors are fabricated using similar techniques. Though semiconductor manufacturers have many processes available to meet different commercial and technical specifications, they all are based on the principles outlined below.

1. Silicon wafer
2. Oxidize to form oxide layer
3. Apply photosensitive layer
4. Expose through high-resolution mask
5. Develop photosensitive layer
6. Etch base window through oxide layer
7. Remove remaining photosensitive layer
8. Diffuse or ion-implant the base
9. Oxidize base window
10. Expose emitter window
11. Etch emitter window through oxide layer
12. Remove remaining photosensitive layer
13. Diffuse or ion-implant the emitter
14. Create metallization window
15. Metallize base and emitter regions
16. Polish and metallize bottom (collector).



1.1.1 Bipolar transistor dies

1.1.1.1 THE COLLECTOR (SUBSTRATE MATERIAL)

All of Philips' present bipolar types are NPN silicon planar epitaxial transistors, see Figs 1-1 and 1-2. The basic epitaxial material consists of a highly doped n-substrate (100 to 200 μm thick) with a rather high ohmic n-layer (epi-layer) deposited on top. The resistivity of this layer determines the collector-base breakdown voltage of the device ($V_{(BR)CBO}$). Most Philips transistors intended for operation at a supply voltage of 28 V have a *guaranteed* breakdown voltage of 65 V (and a typical value of about 80 V). The required resistivity of the epi-layer for this breakdown voltage is 1.6 to 2.0 Ωcm, the exact value having a very small tolerance.

A second important design parameter is the epi-layer thickness, which must be thicker than the collector depletion layer thickness at breakdown to prevent reverse second breakdown when the base current is negative. This occurs when the collector voltage is higher than the collector-emitter breakdown voltage with open base, $V_{(BR)CEO}$. Normally, this voltage is about half the collector-base breakdown voltage mentioned earlier. When the collector voltage is between these two collector breakdown voltages ($V_{(BR)CBO}$ and $V_{(BR)CEO}$), the situation is as shown in Fig.1-3.

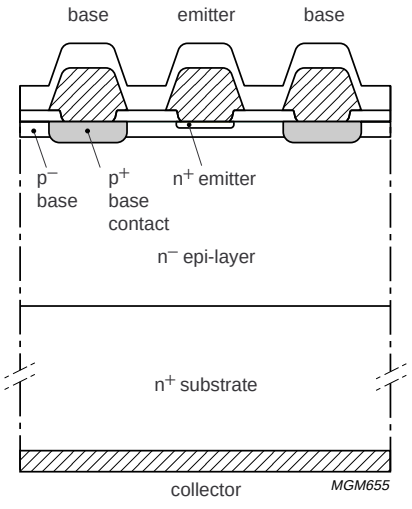


Fig.1-1 Cross-section of a bipolar transmitting transistor.

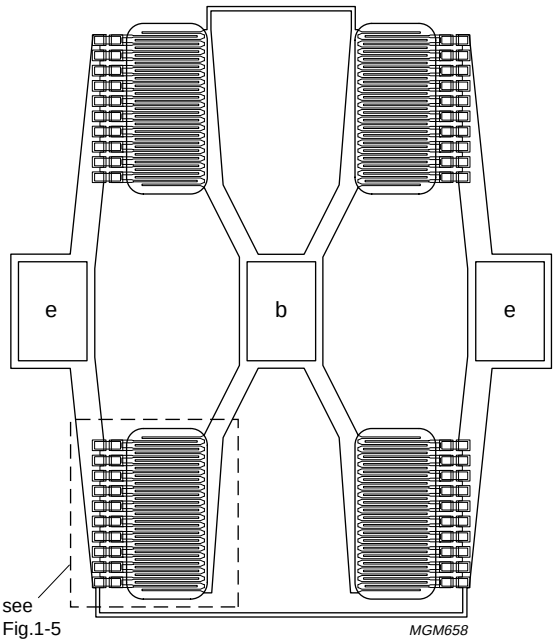


Fig.1-2 Layout of a typical bipolar transmitting transistor die.

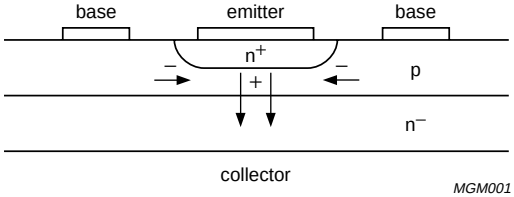


Fig.1-3 When the collector voltage is between $V_{(BR)CBO}$ and $V_{(BR)CEO}$, very high current densities are formed under the emitter. The arrows indicate the direction of electron current.

As Fig.1-3 shows, the collector current is concentrated in the middle of the emitter which can lead to very high current densities. The base is negative along the edge of the emitter and positive beneath it. If this situation continues for a long time, it will eventually destroy the transistor. This effect can be reduced by making the epi-layer somewhat thicker than strictly necessary, the chosen thickness being a compromise between the transistor's RF performance and its ability to withstand certain forms of output mismatching.

1.1.1.2 THE EMITTER AND BASE

The emitter of an RF power transistor must be dimensioned such that the transistor can deliver the required output power with all performance-degrading effects such as capacitances minimized. To achieve this, both the emitter area and periphery are important parameters, because of 'emitter-crowding', see Fig.1-4.

The base (electron) current makes the base positive along the edge of the emitter but negative in the middle. This means that collector current only flows at the edge of the emitter, so the potential output power is mainly determined by the emitter periphery. Under normal operating conditions, only 1 to 2 μm of the edge of the emitter is active; the rest of the emitter merely introduces parasitic capacitance. A practical choice for emitter width is 2 to 4 μm.

For a 2 to 4 μm wide emitter, a good design rule of thumb is that every watt of output power requires about 2 mm of emitter periphery. A narrower emitter can improve some characteristics, but requires more emitter periphery per watt.

Of course, it is not very practical to make one extremely long, narrow emitter, so transistor designers use an interdigitated structure as shown in Fig.1-5. In this structure, the emitter is split into several parallel parts ('fingers') with the base contacts in between. The finger pitch is mainly determined by the maximum frequency of operation - the higher the frequency, the smaller the pitch.

The emitter fingers are normally connected at one end by metallization. As a result, there is a voltage drop along each finger. This must not exceed 25 to 30 mV at maximum collector current otherwise part of the finger will be cut off near the other end.

Splitting the emitter into many sections is thus required for practical reasons and for good operation. This is also true to some extent for the base, but for different reasons. In fact, if the required output power is low, say 2 to 3 W, a single base area is acceptable. At higher powers, it is necessary to split the base area into several parts as this:

– Reduces the thermal resistance of the die
– Increases the base periphery, improving the distribution of dissipation at breakdown since collector breakdown occurs first along the edges of the base areas
– Allows more base and emitter bonding pads to be included, which reduces the emitter lead inductance, increasing the power gain. In addition, splitting the base area reduces the current through each bonding wire.

The preferred distance between successive base areas is approximately twice the die thickness, say about 300 μm, to obtain a low thermal resistance. A disadvantage of splitting the base is higher parasitic capacitances.

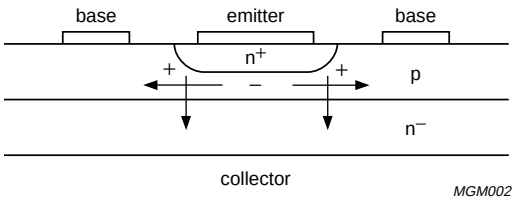


Fig.1-4 Emitter crowding effect. The arrows indicate the direction of electron current in normal operation. Note, to prevent confusion, the base current has also been drawn as an electron current.

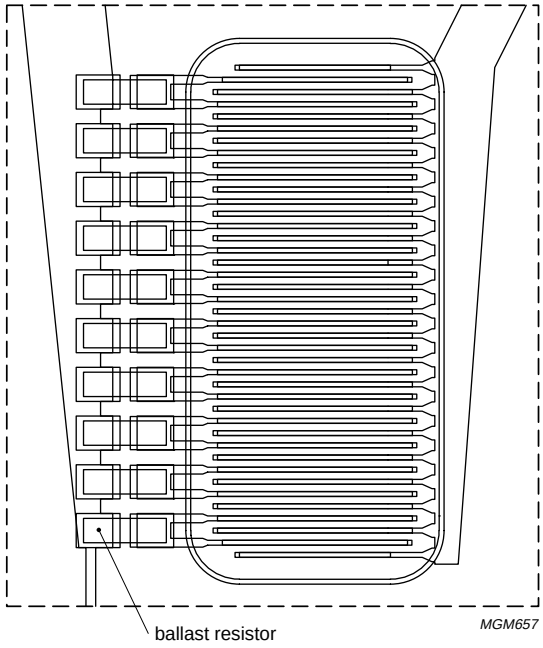


Fig.1-5 Interdigitated base-emitter structure.

1.1.1.3 EMITTER BALLAST RESISTORS

For electrical ruggedness, a built-in emitter ballast resistor is virtually a necessity. This is certainly the case when class-A or class-AB operation can be expected. In class-A for instance, without such an emitter resistor, the collector current can become restricted to a small area in the middle of the die where the temperature is highest. This causes a large increase in the thermal resistance which can destroy the transistor at a much-reduced DC power.

To prevent this effect, each emitter finger or group of two fingers, is provided with an emitter resistor. Good current distribution is obtained if the total emitter resistance is such that the voltage drop across it is approximately 200 to 300 mV at the normal DC collector current.

Emitter resistors can be made as a p^+-diffusion beside the base areas (Fig.1-6a) or as a doped polysilicon layer on top of the oxide (Fig.1-6b), the latter producing less parasitic capacitance.

The temperature coefficient (t.c.) of a diffused emitter resistance is positive, and at practical operating temperatures (~125 °C), the resistance increases by approximately 0.1%/K. The t.c. of a polysilicon resistor is much smaller.

1.1.1.4 DIFFUSION AND IMPLANTATION PROCESSES

The first transmitting transistors were made using diffusion processes. Nowadays, ion implantation followed by temperature treatment is the preferred manufacturing process as it provides superior reproducibility and sharper (i.e. better defined) doping transitions. The specific implantation process used depends primarily on the maximum frequency of operation required. For the highest frequency transistors, extremely shallow implantations are used, giving a thin base and a high f_T. The resulting h_{FE}, usually about 50, is ample for RF operation.

1.1.2 Vertical DMOS transistor dies

1.1.2.1 THE DRAIN (SUBSTRATE MATERIAL)

Philips' RF power MOS transistors are all silicon n-channel enhancement types, (see Fig.1-7). The considerations for and dimensioning of the epitaxial material are principally the same as those for bipolar transistors (Section 1.1.1.1).

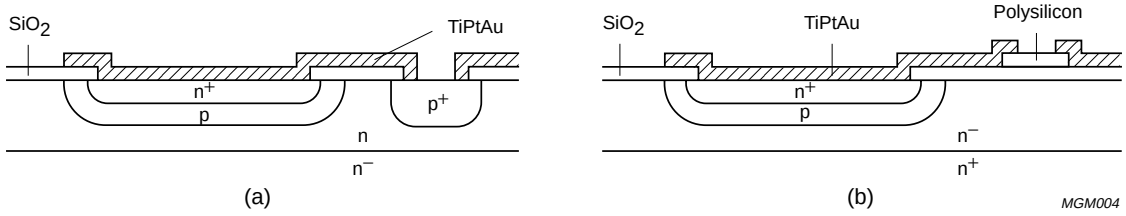


Fig.1-6 Emitter resistance formed (a) by a p^+-diffusion beside the base areas, and (b) as a doped polysilicon layer on top of the oxide.

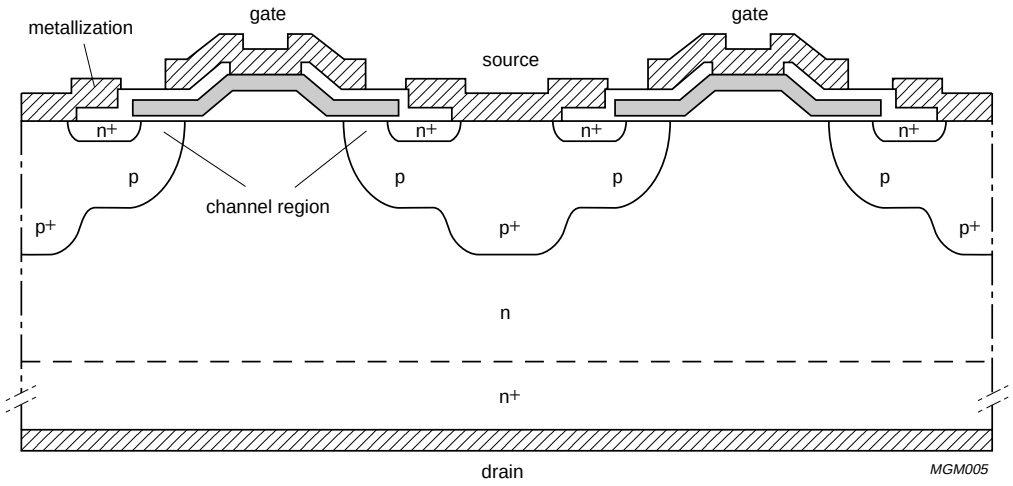


Fig.1-7 Cross-section of a vertical DMOS transmitting transistor. The *length* of the gate (the channel length) is in the plane of the paper; the channel *width* is into the plane of the paper.

1.1.2.2 THE SOURCE AND GATE

The configuration of source and gate in most MOS transmitting transistors is similar to the interdigitated emitter and base of a bipolar transistor, see Fig.1-9.

The RF output power that such a device can deliver depends of course on the maximum drain current (I_{DSX}) which, in turn, is directly proportional to the width of the gate (approximately equal to the 'channel width'). To facilitate comparison with bipolar transistors, the source periphery (virtually the same as the total channel width) is used. Dimensioning is then very similar to that of a bipolar transistor, namely 2 to 3 mm of source periphery per watt of output power.

An equivalent to the emitter ballast resistors of a bipolar transistor is not required. This is because the temperature coefficient of the drain current as a function of the gate voltage is negative at high drain currents, providing automatic protection against thermal runaway, see Fig.1-8.

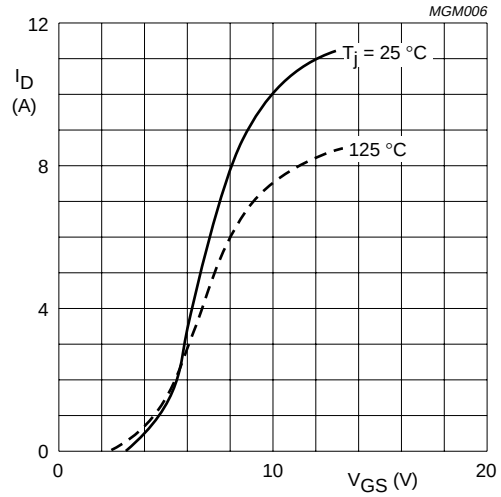


Fig.1-8 At high drain currents, the negative temperature coefficient of the drain current vs. gate voltage protects against thermal runaway.

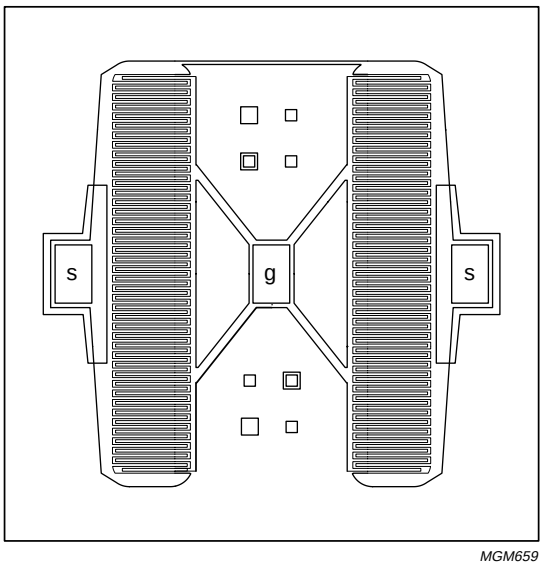


Fig.1-9 Interdigitated source and gate arrangement of a typical MOS transmitting transistor die. Die size: 1×1 mm^2.

1.1.2.3 THE CHANNEL REGION

As for bipolar devices, the process used to manufacture a MOS transistor is dependent on the intended maximum operating frequency. A key parameter is the length of the channel, l_{ch}, (gate) because it determines the cut-off frequency, f_T:

$$f_T = \frac{G_{fs}}{2\pi C_{is}} = \frac{V_{sat}}{4\pi l_{ch}}$$

where:

G_{fs} is the forward transconductance

C_{is} is the input capacitance

V_{sat} is the saturation velocity (for silicon: 10^7 cm/s)

and

l_{ch} is the channel (gate) length.

1.1.2.4 COMPARISON OF VDMOS AND BIPOLAR TRANSISTORS

Both Philips' bipolar and MOS types can provide excellent performance. At high frequencies (~1 GHz and above), bipolar transistors usually provide the best all-round performance. At lower frequencies, VDMOS devices can outperform bipolar types, e.g. on power gain, and will likely capture an increasing part of the present bipolar market as performance continues to improve.

Table 1-1 VDMOS and bipolar devices compared

ADVANTAGES OF VDMOS	DISADVANTAGES OF VDMOS
Simpler biasing circuit. This is primarily due to a MOS transistor's high input impedance, and the low and negative temperature coefficient at high drain currents.	**The gate is sensitive to electrostatic charges** so ESD protection measures must be taken.
Lower noise. This is especially important in duplex equipment and where many transceivers are operating near to each other and at similar frequencies.In one test, an improvement of 7 dB was measured at 75 MHz in similar wideband amplifiers.	**Higher output power 'slump'** (reduction of output power at high temperature). Note, this is primarily caused by decreasing transconductance.
Higher power gain (up to ~5 dB higher) than comparable bipolar types at lower frequencies. This is mainly due to the high transconductance and low feedback capacitance.	
Simple control of the output power. The output power can be controlled down to almost zero simply by reducing the DC gate-source voltage.	
Superior thermal stability owing to the negative temperature coefficient of the drain current at high levels, this is also why the current distribution over the whole active area of a VDMOS device is so good.	
Superior load mismatch tolerance - Another benefit of the superior thermal stability of a VDMOSFET.	
Lower high-order (7th and higher) intermodulation products due to the 'smoother' characteristics of MOS devices.	

1.1.3 Lateral DMOS (LDMOS) transistor dies

LDMOS technology is a relatively recent development. Unlike VDMOS which can be used up to about 1 GHz, LDMOS, like bipolar, is suitable for use at higher frequencies owing to its lower feedback capacitance and source inductance than VDMOS. However, depending on the particular performance and cost requirements, VDMOS, LDMOS or bipolar can provide the best solution.

1.1.3.1 THE SOURCE (SUBSTRATE MATERIAL)

Philips LDMOS transistors are all silicon n-channel enhancement types, (see Fig.1-11). The substrate is highly doped p-material, whereas the epitaxial layer is lightly doped p^--material.

1.1.3.2 THE DRAIN AND GATE

The configuration of drain and gate is fairly similar to the interdigitated emitter and base of a bipolar transistor, see Fig.1-10. Note however that *all regions, (gate, source and drain) are metallized on top of the die*. The gate and drain are connected to bonding pads, and the source is grounded to the substrate by means of a via-diffusion through the epi-layer. The benefit of this design is that a *single* metal interconnect can be used. Note, the top source metallization is solely for interconnecting the p^+ and n^+ regions; the transistor's source electrode is connected to the bottom (substrate) metallization.

As for a VDMOS device, the RF output power that an LDMOS device can deliver depends on the maximum drain current (I_{DSX}) which is directly proportional to the width of the gate (approximately equal to the 'channel width'). And, an equivalent to the emitter ballast resistors of a bipolar transistor is again not required, see Section 1.1.2.2.

1.1.3.3 THE CHANNEL REGION

As with VDMOS, a key parameter of an LDMOS transistor is the length of the channel, l_{ch} (gate) because it determines the cut-off frequency, f_T (defined as for VDMOS in Section 1.1.2.3).

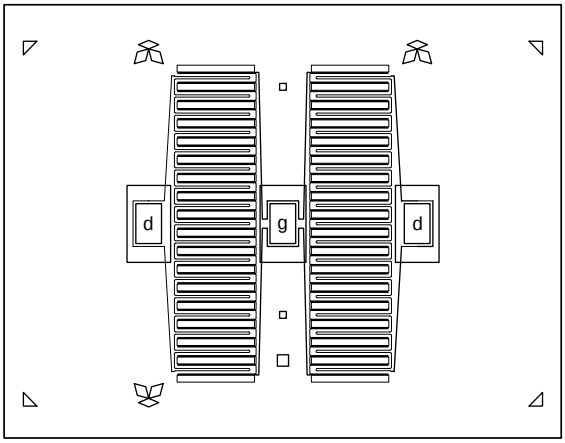


Fig.1-10 Interdigitated drain, source and gate arrangement of a typical LDMOS transmitting transistor die.
Die size: 1×0.8 mm^2.

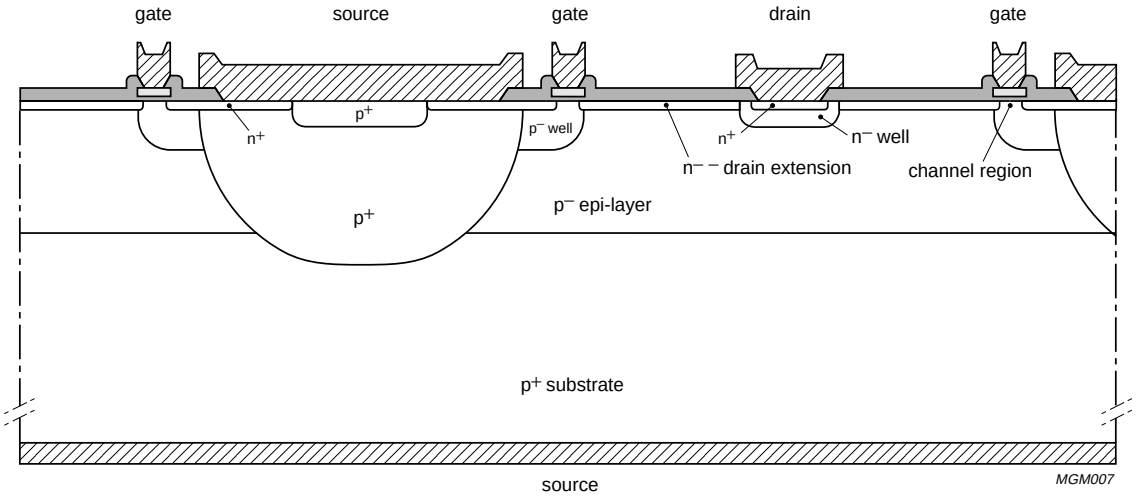


Fig.1-11 Cross-section of an LDMOS transmitting transistor. The *length* of the gate (the channel length) is in the plane of the paper; the channel *width* is into the plane of the paper.

1.1.3.4 COMPARISON OF LDMOS AND BIPOLAR TRANSISTORS

Both Philips' LDMOS and bipolar transistors can provide excellent performance in a variety of applications. Nevertheless, there are some differences. For example, the lateral structure of an LDMOS transistor means it has a very low feedback capacitance compared with a bipolar transistor. And as power gain is directly related to the feedback capacitance and source (or emitter) inductance, this means an LDMOS transistor has higher power gain. Furthermore, an LDMOS transistor has superior intermodulation distortion performance over a large dynamic range.

Table 1-2 LDMOS and bipolar devices compared

ADVANTAGES OF LDMOS	DISADVANTAGES OF LDMOS
Simpler biasing circuit. This is primarily due to a MOS transistor's high input impedance, and the low and negative temperature coefficient at high drain currents. **Higher power gain** than comparable bipolar types. This is due to the low source inductance and low feedback capacitance. **Simple control of the output power**. The output power can be controlled down to almost zero simply by reducing the DC gate-source voltage. **Superior thermal stability** owing to the negative temperature coefficient of the drain current at high levels. This is also why the current distribution over the whole active area of an LDMOS device is so good. **Superior load mismatch tolerance** - another benefit of the superior thermal stability of an LDMOSFET. **Lower high-order (7th and higher) intermodulation products** due to the 'smoother' characteristics of MOS devices.	**The gate is sensitive to electrostatic charges**, so ESD protection measures must be taken. **Higher output power 'slump'** (reduction of output power at high temperature). Note, this is primarily caused by decreasing transconductance.

1.2 Transistor equivalent circuit

At this point, it is useful to introduce a basic equivalent circuit of a bipolar RF transmitting transistor, and a few simple expressions that indicate the behaviour of power gain, input and load impedance under different conditions. This will assist the understanding of the following section on internal matching.

Figure 1-12 shows a simple equivalent circuit of an RF transistor with load circuit. Note, the emitter inductance, L_E, affects transistor performance significantly as we shall see presently.

1.2.1 Main elements

The collector-to-base feedback capacitance consists of two parts (see Fig.1-1, transistor cross-section):

– *An intrinsic part C_{BCi}:* the capacitance of the reverse biased collector-to-base junction in the regions below the emitter

– *An extrinsic part C_{BCe}:* the capacitance of the same junction beyond the emitter. C_{BCe} also includes parasitic capacitances introduced by the base metallization.

The sum of these capacitances, C_{BCt}, is published in data sheets as C_{re}:

$$C_{re} = C_{BCi} + C_{BCe}$$

R_B represents the series resistance of the base layer, and R_E is the emitter ballast resistance. C_{BE} represents the total forward biased base-emitter capacitance which is mainly determined by the diffusion capacitance, and which varies directly with the emitter current. This capacitance is normally shunted by a resistor, omitted here, since at high frequency operation, virtually all current flows into C_{BE}.

The collector is terminated by a load resistance R_L shunted by an inductance L_L which resonates with the total collector-to-base capacitance. Approximate expressions for these circuit elements are:

$$L_L = \frac{1}{\omega^2 C_{BC}} \text{ and } R_L = \frac{V_C^2}{2P_L}$$

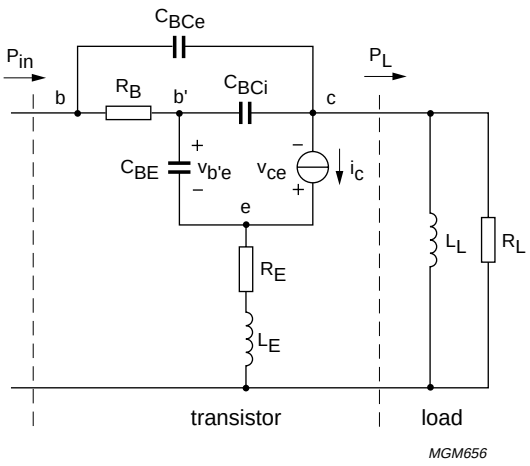
At high frequencies, the collector current, i_c, is proportional to the base-emitter current, i_{be}, and lags the latter by 90°:

$$i_c \approx i_{b'e}\left(\frac{\omega_T}{j\omega}\right)$$

Clearly, the high frequency common-emitter current gain, h_{fe}, is approximately ω_T/ω.

To simplify the following approximations, it has been assumed that:

– For maximum power, the collector circuit is in resonance, i.e. v_{ce} and i_c are in antiphase
– The base potential is very small compared to the collector voltage
– All collector parasitics are part of the load circuit.



b: Base.
c: Collector.
e: Emitter.

Fig.1-12 Simple equivalent circuit of a bipolar RF transmitting transistor.

1.2.2 Input impedance

With these assumptions, the input impedance, Z_{in}, can be approximated by:

$$Z_{in} = \left[\frac{1}{1+\omega_T C_{BCt} R_L}\right] \times$$

$$\left[(1+\omega_T C_{BCi} R_L)\, R_B + \omega_T L_E + R_E + j\omega L_E + \frac{1}{j\omega}\left(\frac{1}{C_{BE}} + R_E \omega_T\right)\right]$$

Note that emitter inductance effectively increases the total input resistance by $\omega_T L_E$. The emitter ballast resistance R_E appears as a series capacitance $1/R_E\omega_T$, decreasing the total input capacitance. Based on this expression, the total input impedance can be represented by a series RLC equivalent circuit, see Section 1.3.1.

1.2.3 Power gain

The power gain, Gp, can be approximated by:

$$G_p = \frac{P_L}{P_{in}} = \left(\frac{\omega_T}{\omega}\right)^2 \left(\frac{1}{1+\omega_T C_{BCt} R_L}\right) \times \left(\frac{R_L}{(1+\omega_T C_{BCi} R_L)\, R_B + R_E + \omega_T L_E}\right)$$

Note that emitter inductance L_E reduces power gain and is a key performance-determining factor in high-frequency transistors. It depends on bonding wire and package inductances. Other important parameters affecting power gain are R_E and these are determined by the active parts of the die design.

1.2.4 Large-signal expressions

The expressions given for Z_{in} and G_p relate to class-A amplifiers operating in the linear (i.e. small-signal) region. For large-signal operation, several elements become non-linear. The expressions can however still be used for a first-order approximation by substituting *average* values for the voltage and current dependent elements. In addition for class-B and class-C operation, the conduction angle, which affects the average value of ω_T, should be taken into account.

1.3 Internal matching

Impedance matching is required to optimize the performance of a transmitting transistor in the application for which it was designed. Internal matching raises impedances and improves wideband capability. To assist designers, many of Philips' transmitting transistors already incorporate internal matching circuitry, simplifying or reducing the external matching required.

1.3.1 Input matching

Figure 1-13 shows the equivalent circuit of the input impedance of a bipolar transmitting transistor without matching circuitry.

At high frequencies, the capacitor has very low reactance and can be neglected in most cases. In a high-power transistor, the resistor becomes very small, typically <1 Ω, as such a device can be considered as many small 'transistors' in parallel The inductor, which is normally 1 to 2 nH, has a rather high reactance in the UHF region, so the input Q becomes high, making wideband matching difficult if not impossible, while circuit losses increase significantly. To compensate for these effects, an additional capacitor is often fabricated 'inside' the transistor such that the transistor equivalent circuit is as shown in Fig.1-14.

This capacitor, together with the base and emitter inductances, forms a first matching section that raises the input impedance to a more acceptable level. The resonant frequency of the section is set to be somewhat above the maximum operating frequency for which the transistor is intended.

An additional advantage of this configuration is that it increases the power gain slightly at the high end of the frequency band, not only because of reduced circuit losses, but mainly because the capacitor is, in effect, connected to a tap on the emitter lead inductance, overcoming a major cause of reduced power gain at high frequencies (emitter lead inductance).

A MOS capacitor is used, and it can only be used in transistor packages with two emitter 'bridges': one, the normal elevated bridge; the other, an integrated bridge on the beryllia disc to which the capacitor is soldered. The maximum performance improvement is obtained with packages having *four* emitter connections (see Fig.1-15). Better still of course are packages with internal emitter grounding.

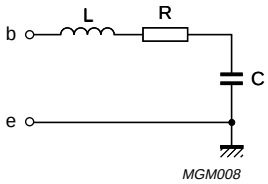


Fig.1-13 Equivalent circuit of the input impedance of a bipolar transmitting transistor. For high-frequency high-power operation, matching circuitry is required. b: base; e: emitter.

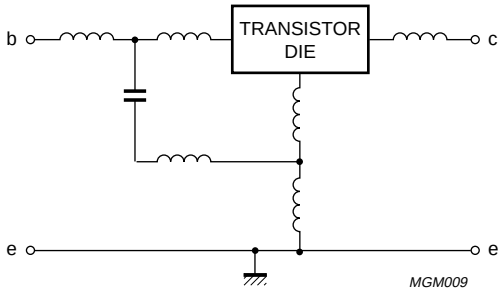


Fig.1-14 Equivalent circuit of a bipolar transmitting transistor with internal input matching. Adding an internal capacitor improves wideband matching.

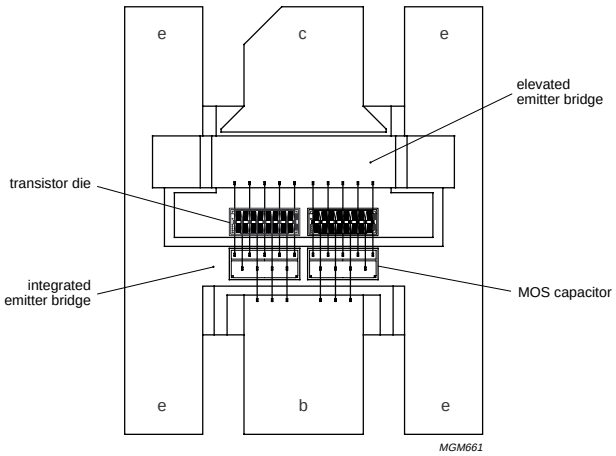


Fig.1-15 Position of the MOS input matching capacitor in a package with two emitter bridges, and four emitter connections.

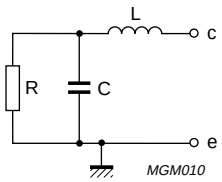


Fig.1-16 Large-signal equivalent circuit of the output of an RF power transistor.
L: collector and emitter lead inductance;
C: effective output capacitance;
R: optimum load resistance. Note, R is the load resistance that produces maximum output. It is not a physical resistor in a transistor and its value varies according to the application.

1.3.2 Output matching

At the output of a transistor, the situation is somewhat different, see Fig.1-16.

In wideband matching circuits, it is desirable to tune out (with inductive shunt) the capacitor C somewhere in the frequency band for which the transistor is intended. In practice, the best results are obtained when the resonant frequency is in the lower part of the band.

If an *external* shunt inductor were used for this purpose, the result would be a very low inductive tap, making further matching extremely difficult, especially at high powers and frequencies. A better solution would be to tune out the collector capacitance *inside the transistor package*. This is done in practice in balanced (push-pull) transistors by adding a metallized strip onto the beryllia or aluminium nitride disc. In single-ended devices, it is done by connecting one side (the other is grounded) of a MOS capacitor that provides isolation to the collector via bonding wires that form the required shunt inductance, see Fig.1-17.

A disadvantage of this approach in both cases is that such a transistor is unsuitable for use in frequency bands lower than the one for which it is intended. This limitation is outweighed however by the higher load impedance and lower Q-factor, resulting in lower losses in the matching circuit and improved wideband performance.

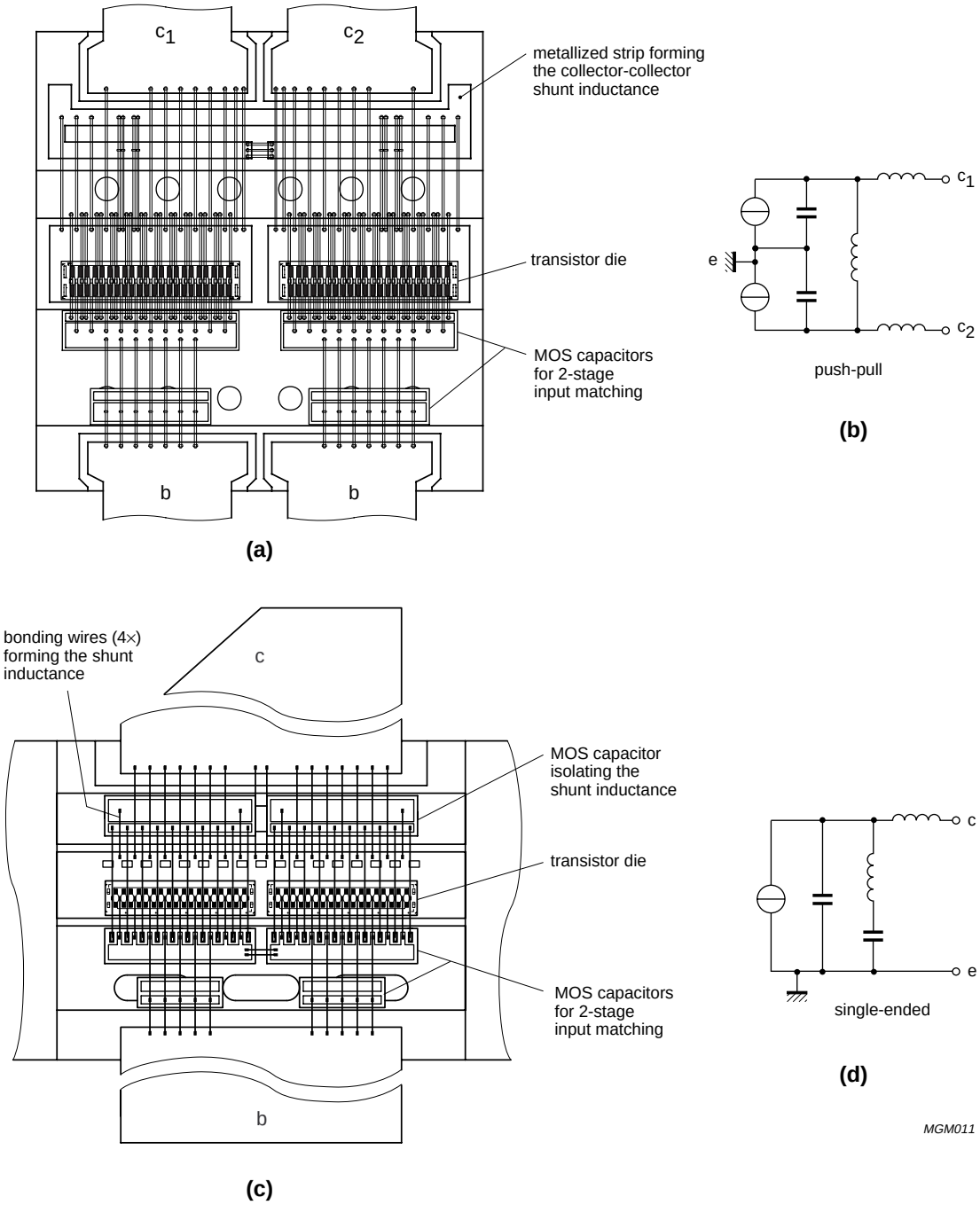


Fig.1-17 Bonding arrangement of (a) a BLV861 intended for use in push-pull configuration (b), and (c) bonding arrangement of a BLV2045 intended for single-ended configuration (d).

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