THERMAL CONSIDERATIONS - DIODES

Thermal resistance

Circuit performance and long-term reliability are affected by the temperature of the die. Normally, both are improved by keeping the die temperature (junction temperature) low.

Electrical power dissipated in any semiconductor device is a source of heat. This increases the temperature of the die about some reference point, normally an ambient temperature of 25 °C in still air. The extent of increase in temperature depends on the amount of power dissipated in the device and the net thermal resistance between the heat source and the reference point. This can be expressed with the following formula:

$\Delta T_j = P_{tot} \times R_{th(j\text{-}a)}$

where:

ΔT_j is the increase in junction temperature

P_{tot} is the total power generated in the device

$R_{th(j\text{-}a)}$ is the thermal resistance from junction to ambient.

Surface mount devices

Heat transfer can occur by radiation, conduction and convection. Surface mount devices lose most of their heat by conduction when mounted on a substrate. Referring to Fig.1, heat conducts from its source (the junction) via the package leads and soldered connections to the substrate. Some heat radiates from the package into the surrounding air, where it is dispersed by convection or by forced cooling air. Heat that radiates from the substrate is dispersed in the same way.

The thermal resistance for surface mounted devices therefore, can be expressed as:

$R_{th(j\text{-}a)} = R_{th(j\text{-}tp)} + R_{th(tp\text{-}a)}$ (see Fig.2)

where:

$R_{th(j\text{-}a)}$ is the thermal resistance from junction to ambient

$R_{th(j\text{-}tp)}$ is the thermal resistance from junction to tie-point

$R_{th(tp\text{-}a)}$ is the thermal resistance from tie-point to ambient.

The $R_{th(j\text{-}tp)}$ value is essentially independent of external mounting method and cooling air, but is sensitive to the materials used in the package construction, the die bonding method and the die area, all of which are fixed.

The $R_{th(tp\text{-}a)}$ value depends on the shape and material of the tracks and substrate. For all package types these values are given in Table 1 for mounting on (FR4) printed-circuit board with small pad area. For other pad areas and printed-circuit board configurations see Fig.3.

The maximum power handling capability ($P_{tot(max)}$) is given by:

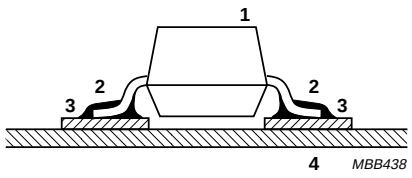
$$P_{tot(max)} = \frac{(T_{j(max)} - T_{amb})}{R_{th(j\text{-}a)}}$$

where:

$T_{j(max)}$ is the maximum junction temperature

T_{amb} is the ambient temperature.

Calculating this maximum power handling capability we have to take into account the maximum junction temperature of the particular device, the maximum temperature of the solder joints (110 °C for long time reliability) and the ambient temperature. Dependent on the ratio of the component parts of the thermal resistance, it will be possible that the junction temperature or the temperature of the solder joints (T_{tp}) will be the limiting factor. This can be shown in the following examples for SOT23 and SOD87 packages mounted on FR4 printed-circuit board.



Heat radiates from the package (1) to ambient.
Heat conducts via leads (2), solder joints (3) to the substrate (4).

Fig.1 Heat losses.

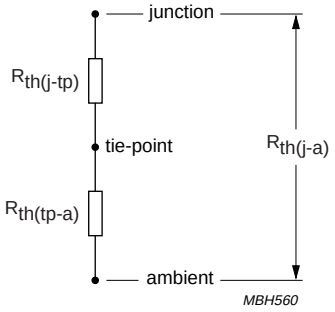


Fig.2 Representation of thermal resistance paths for a surface mounted diode.

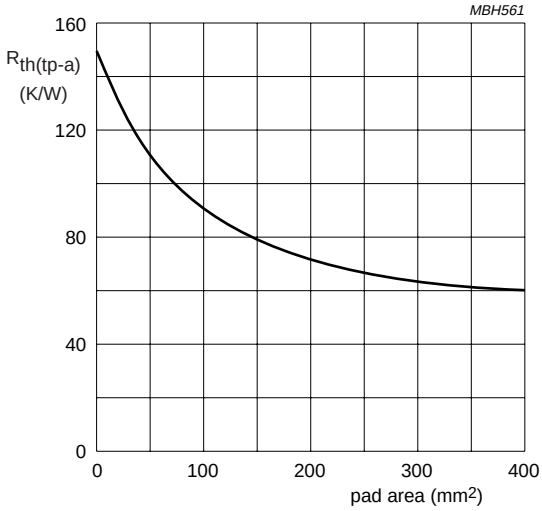


Fig.3 Thermal resistance ($R_{th(tp-a)}$) as a function of FR4 printed-circuit board pad area.

Table 1 Thermal resistance values and maximum power handling capability of surface mount packages

PACKAGE	$R_{th(j-a)}$ (K/W)	$R_{th(j-tp)}$ (K/W)	$R_{th(tp-a)}$ (K/W)	$P_{tot(max)}$ (W)
SC-59 (SOT346)	500	350	150	0.25
SC-70 (SOT323)	500	350	150	0.25
SOD80(C)	320 to 600	170 to 450	150	0.21 to 0.47
SOD87	150	30	120	0.71
SOD106	150	25	125	0.68
SOD110	315	165	150	0.40
SOD323	625	475	150	0.20
SOT23	500	350	150	0.25
SOT143	500	350	150	0.25
SOT323	625	475	150	0.20

EXAMPLE FOR THE SOT23 PACKAGE

$$P_{tot(max)} = \frac{(T_{j(max)} - T_{amb})}{R_{th(j-a)}}$$

$$= \frac{(150\,°C - 25\,°C)}{500\ K/W} = 0.25\ W$$

$$T_{tp} = T_{amb} + P_{tot(max)} \times R_{th(tp-a)}$$

$$= 25\,°C + 0.25\ W \times 150\ K/W = 62.5\,°C$$

This is below 110 °C, so $T_{j\,max}$ is the limiting factor.

EXAMPLE FOR THE SOD87 PACKAGE

$$P_{tot(max)} = \frac{(T_{j(max)} - T_{amb})}{R_{th(j-a)}}$$

$$= \frac{(175\,°C - 25\,°C)}{150\ K/W} = 1\ W$$

$$T_{tp} = T_{amb} + P_{tot(max)} \times R_{th(tp-a)}$$

$$= 25\,°C + 1\ W \times 120\ K/W = 145\,°C$$

This is above 110 °C, so the $P_{tot(max)}$ will be limited by T_{tp}, therefore:

$$P_{tot(max)} = \frac{(T_{tp} - T_{amb})}{R_{th(tp-a)}}$$

$$= \frac{(110\,°C - 25\,°C)}{120\ K/W} = 0.71\ W$$

The $P_{tot(max)}$ values given in Table 1 are based on:

T_{amb} = 25 °C; $T_j = T_{j(max)}$; $T_{tp} \leq 110$ °C.

Leaded devices

Figure 4 illustrates the various components of thermal resistance for an axial leaded diode mounted with symmetrical, equal length leads. The thermal resistance from junction to ambient ($R_{th(j-a)}$) comprises the following thermal resistances:

$R_{th(j-p)}$ is the thermal resistance from junction to package

$R_{th(p-tp)}$ is the thermal resistance from package to tie-point

$R_{th(tp-a)}$ is the thermal resistance from tie-point to ambient

$R_{th(p-a)}$ is the thermal resistance from package to ambient.

The values of the thermal components depend on the diode package type, the lead length and the mounting method used.

Using the model in Fig.4 and referring to Table 2, values for the thermal resistance from junction to ambient can be calculated using the formula:

$$R_{th(j-a)} = R_{th(j-p)} + \frac{R_{th(p-a)}(R_{th(p-tp)} + R_{th(tp-a)})}{R_{th(p-a)} + R_{th(p-tp)} + R_{th(tp-a)}}$$

The maximum power handling capability ($P_{tot(max)}$) is given by:

$$P_{tot(max)} = \frac{(T_{j(max)} - T_{(amb)})}{R_{th(j-a)}}$$

where:

$T_{j(max)}$ is the maximum junction temperature and

T_{amb} is the ambient temperature.

Calculating this maximum power handling capability we have to take into account the maximum junction temperature of the particular device, the maximum temperature of the solder joints (110 °C for long time reliability) and the ambient temperature. Dependent on the ratio of the component parts of the thermal resistance it is possible that the junction temperature or the temperature of the solder joints (T_{tp}) will be the limiting factor. This can be shown in the following examples for a SOD57 device mounted on an FR4 printed-circuit board, as shown in Fig.5.

$$R_{th(j-a)} = 14\ K/W + \frac{429\ K/W\,(38\ K/W + 70\ K/W)}{429\ K/W + 38\ K/W + 70\ K/W}$$

$$= 100\ K/W$$

and

$$P_{tot(max)} = \frac{(T_{j(max)} - T_{amb})}{R_{th(j-a)}}$$

$$= \frac{(175\,°C - 60\,°C)}{100\ K/W} = 1.15\ W$$

$$T_{tp} = T_{amb} + \frac{R_{th(p-a)} \times R_{th(tp-a)}}{R_{th(p-a)} + R_{th(p-tp)} + R_{th(tp-a)}} \times P_{tot}$$

Using values in Table 2:

$$T_{tp} = T_{amb} + \frac{429\ K/W \times 70\ K/W}{429\ K/W + 38\ K/W + 70\ K/W} \times P_{tot}$$

is simplified to:

$$T_{tp} = T_{amb} + 56\ K/W \times P_{tot}$$

Using T_{tp} = 110 °C and T_{amb} = 60 °C the equation becomes:

$$P_{tot} = \frac{(T_{tp} - T_{amb})}{56\ K/W}$$

$$= \frac{(110\,°C - 60\,°C)}{56\ K/W} = 0.89\ W$$

This is lower than $P_{tot(max)}$ = 1.15 W (for $T_{j(max)}$ = 175 °C), so in this particular case T_{tp} = 110 °C is limiting the $P_{tot(max)}$.

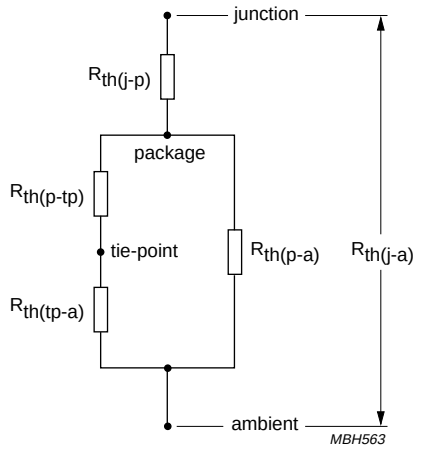


Fig.4 Representation of thermal resistance paths for a leaded device.

Table 2 Thermal resistance values for leaded packages
All values expressed in K/W, unless otherwise specified.

THERMAL RESISTANCE	CONDITIONS	SOD27	SOD57	SOD64	SOD66	SOD68	SOD81	SOD91
$R_{th(j-p)}$		125	14	10	95	150(1)	28	60
$R_{th(p-tp)}$	lead length = 5 mm	121	19	7	19	121	19	48
	lead length = 10 mm	242	38	14	38	242	38	96
	lead length = 15 mm	363	57	21	57	363	57	144
	lead length = 20 mm	484	76	28	76	484	76	192
	lead length = 25 mm	605	95	35	95	605	95	240
$R_{th(p-a)}$	lead length = 5 mm	1050	586	417	673	1343	787	1261
	lead length = 10 mm	744	429	293	473	879	527	843
	lead length = 15 mm	576	338	225	365	654	396	633
	lead length = 20 mm	469	279	183	297	520	317	507
	lead length = 25 mm	396	237	154	250	432	264	423
$R_{th(tp-a)}$	notes 2 and 3	100	–	–	–	100	–	–
	notes 2 and 4	–	70	70	70	–	70	70
	notes 2 and 5	–	55	55	55	–	55	55
	notes 2 and 6	–	45	45	45	–	45	45

Notes

1. For Schottky diodes in SOD68 package $R_{th(j-p)}$ = 125 K/W.
2. Device mounted on a 1.5 mm thick epoxy-glass printed-circuit board with a copper thickness ≥ 40 μm.
3. Mounted as in Fig.6.
4. Mounted as in Fig.5.
5. Mounted with copper laminate per lead of 1 cm^2.
6. Mounted with copper laminate per lead of 2.25 cm^2.

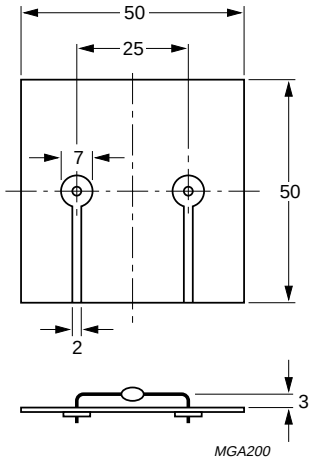


Fig.5 Leaded device mounted on printed-circuit board 50 × 50 mm.

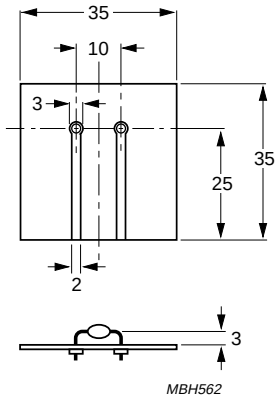


Fig.6 Leaded device mounted on printed-circuit board 35 × 35 mm.

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